OPERATORS, ORGANIZATIONAL, DIRECT SUPPORT
AND GENERAL SUPPORT MAINTENANCE MANUAL

FUNCTIONING OF EQUIPMENT

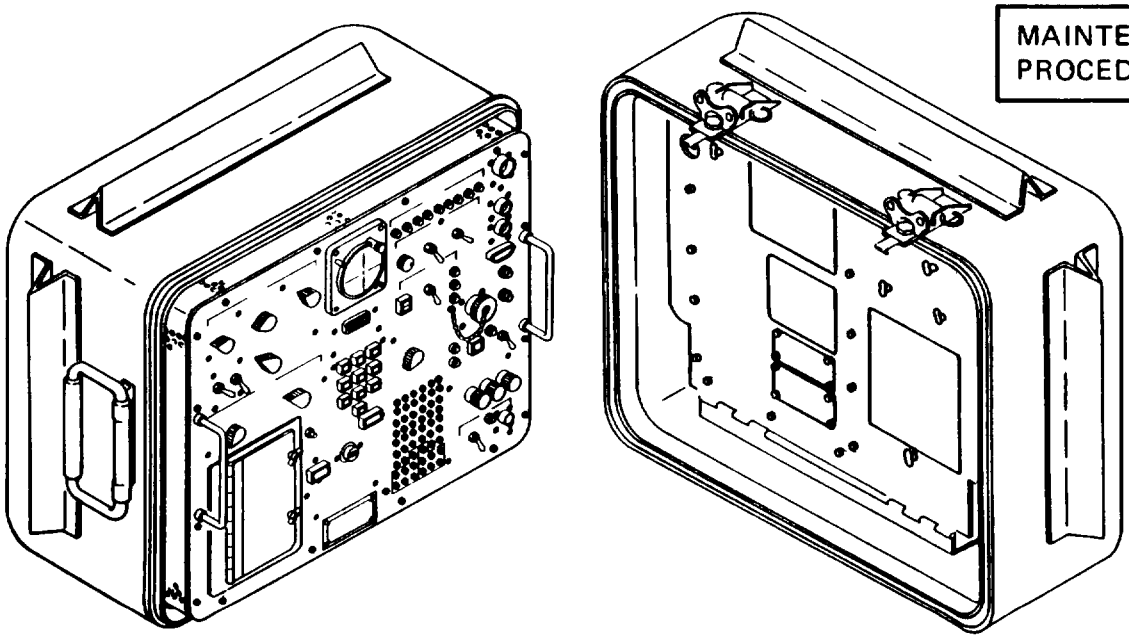
OPERATING INSTRUCTIONS

ELECTRICAL CHECK PROCEDURES

TROUBLESHOOTING PROCEDURES

MAINTENANCE PROCEDURES

PROCESSOR TEST SET AN/APM-415A (NSN 6625-01-147-4741)



HEADQUARTERS, DEPARTMENT OF THE ARMY
15 JANUARY 1986

WARNING

High voltage is used in the operation of this equipment.

DEATH ON CONTACT

may result if personnel fail to observe safety precautions. Learn the areas containing high voltage in each piece of equipment. Be careful not to contact high-voltage connections when installing or operating this equipment. Before working inside the equipment, turn power off and ground points of high potential before touching them.

WARNING

Handle CRT (indicator screen) with extreme caution; implosion may result from careless handling.

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

CAUTION

Do not use acetone, chlorinated, or aromatic hydrocarbons. These type cleaning agents will attack the adhesives used in the magnetic read/write head and plastic parts of the MTCT.

CAUTION

Do not use MTCT until cleaning solution has completely dried.

CAUTION

Do not connect both the processor unit and the control unit to the PTS at the same time. All three units can be damaged when you turn power on at the PTS.

CAUTION

Do not let the DC+ and ground wires touch during the connection of an external power supply to the PTS; damage to the power supply may result.

CAUTION

Do not clean CRT screen or TEST SELECT pushbutton keys with isopropyl alcohol.

CAUTION

Lifting of the processor test set requires two men.

CAUTION

Limit rated power of soldering iron used for soldering to a maximum of 37-1 /2 watts. Use heat sink when soldering diode leads.

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE , TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

TECHNICAL MANUAL
No. 11-6625-2940-14

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 15 January 1986

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT AND GENERAL SUPPORT PROCESSOR TEST SET AN / APM-415A (NSN 6625-01-147-4741)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

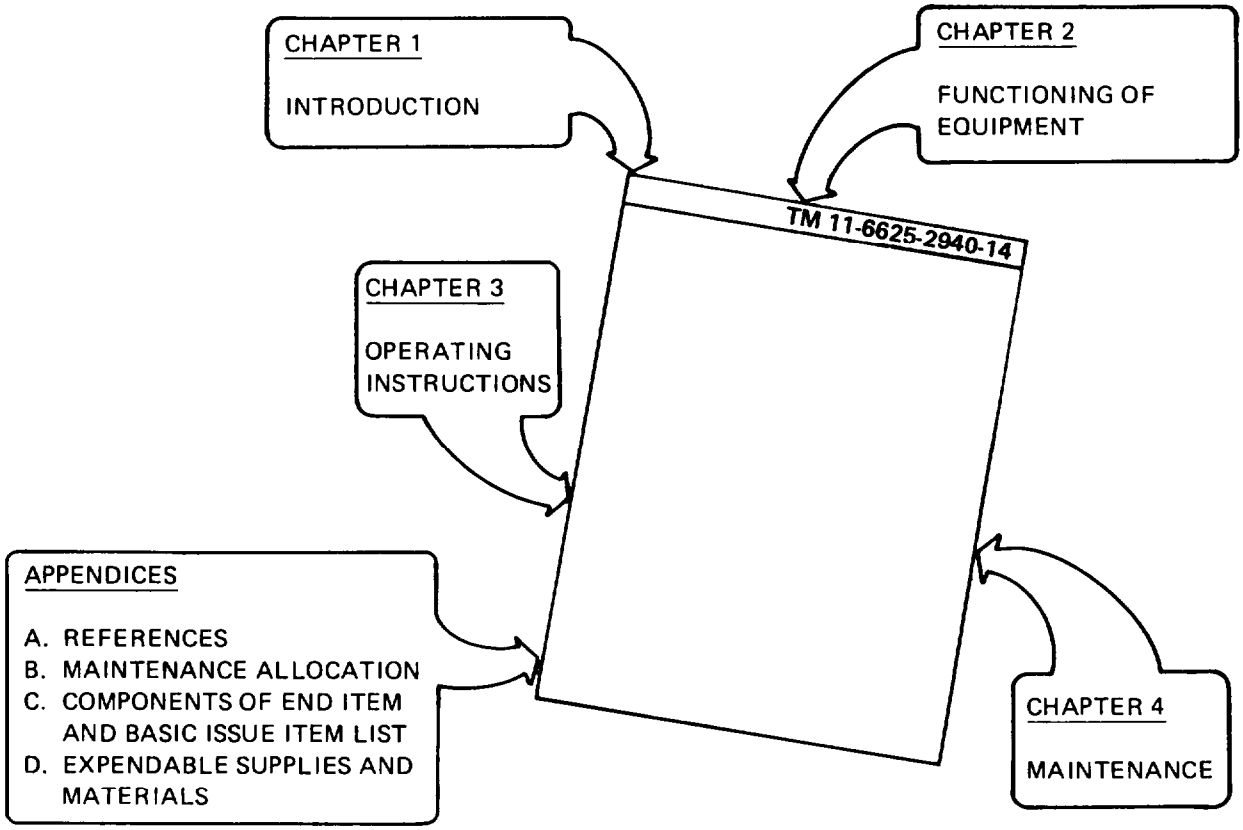
You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2, located in back of this manual, directly to: Commander, US Army Communications - Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. In either case, a reply will be furnished directly to you.

HOW TO USE THIS MANUAL

This manual tells about operating and maintaining Processor Test Set AN/APM-415A at the Aviation Intermediate and Unit Maintenance levels.

Use the front cover locators and 'marked' pages to quickly find the parts of the manual shown on the cover. These portions of the manual were chosen because they are used often. This manual has been divided into chapters, sections, and paragraphs which are numbered sequentially. Tables and figures are also numbered this way. In addition to this numbering system, you will find a system of captions in ORANGE print which will help you quickly find the information you need. These captions name the pieces of equipment and/or maintenance procedures that you will be doing. Some of the procedures may actually consist of several smaller procedures. For example, 'Removal,' 'Installation,' and 'Test after Repair' may be parts of a larger maintenance procedure. The captions for the smaller procedures appear under the captions for the larger ones. Both sets of captions appear on each page which describes the general procedure. Each large section begins with a 'Section Contents' which lists the procedures by title and page number.

Before you attempt to maintain Processor Test Set AN/APM-415A, it is important to familiarize yourself with this manual. Each of the four chapters is unique and you will save time if you know where to go for the information you need. Briefly, this is how this manual is organized:



TURN TO THE NEXT PAGE FOR EXAMPLES OF HOW YOU WILL BE USING THIS MANUAL

HOW TO USE THIS MANUAL (Continued)

PROBLEM

The equipment is “new” to you and you want to familiarize yourself with it quickly.

SOLUTION

Read “Equipment Description” - see chapter 1, section II.

PROBLEM

You have received new equipment. What do you do first?

SOLUTION

Unpack it, inspect it and check it out - see chapter 4, section II.

PROBLEM

Maintenance personnel bring you a processor test set which is defective or suspect. What do you do?

SOLUTION

Check it out, troubleshoot it, and replace defective assemblies if required - see chapter 4, section IV.

PROBLEM

You are unfamiliar with which Army forms and records are applicable to the equipment.

SOLUTION

Read chapter 1, section I.

CHAPTER 1
INTRODUCTION

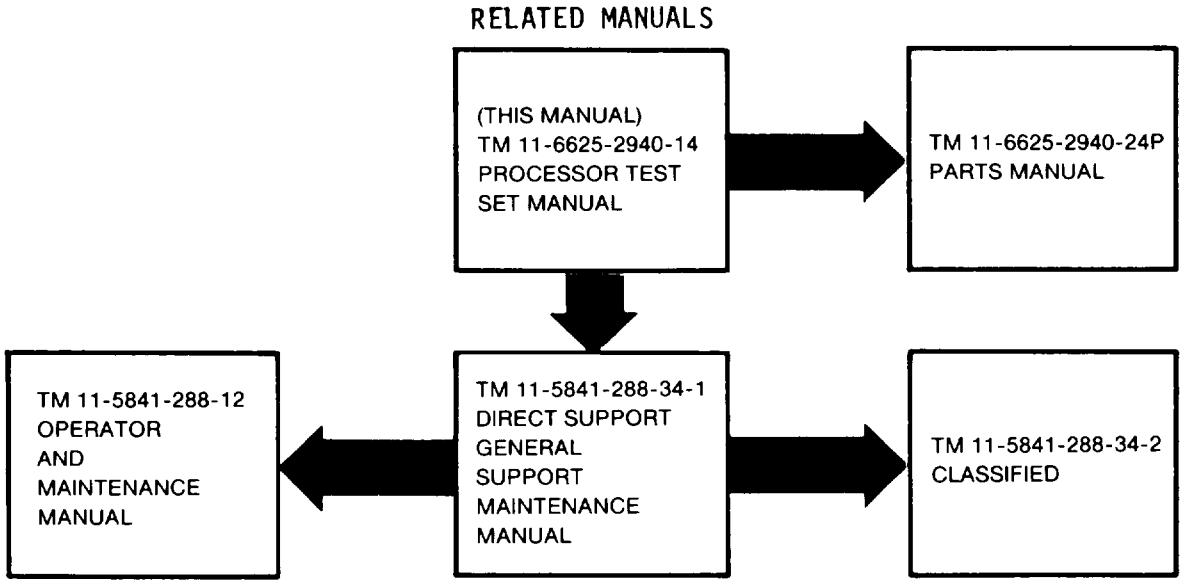
CHAPTER CONTENTS

SECTION 1
GENERAL INFORMATION

SECTION CONTENTS

SCOPE

1-1. This manual covers the operation and maintenance of Processor Test Set AN/APM-415A, at the operator, organizational, direct support and general support level. The manual contains equipment description, test, fault isolation information and repair procedures for the processor test set. Refer to TM 11-6625-2940-24P for repair parts and special tools listings. Use this manual to keep up your skills and maintain the equipment in top operating order.



1-2. Maintenance Forms, Records, and Reports

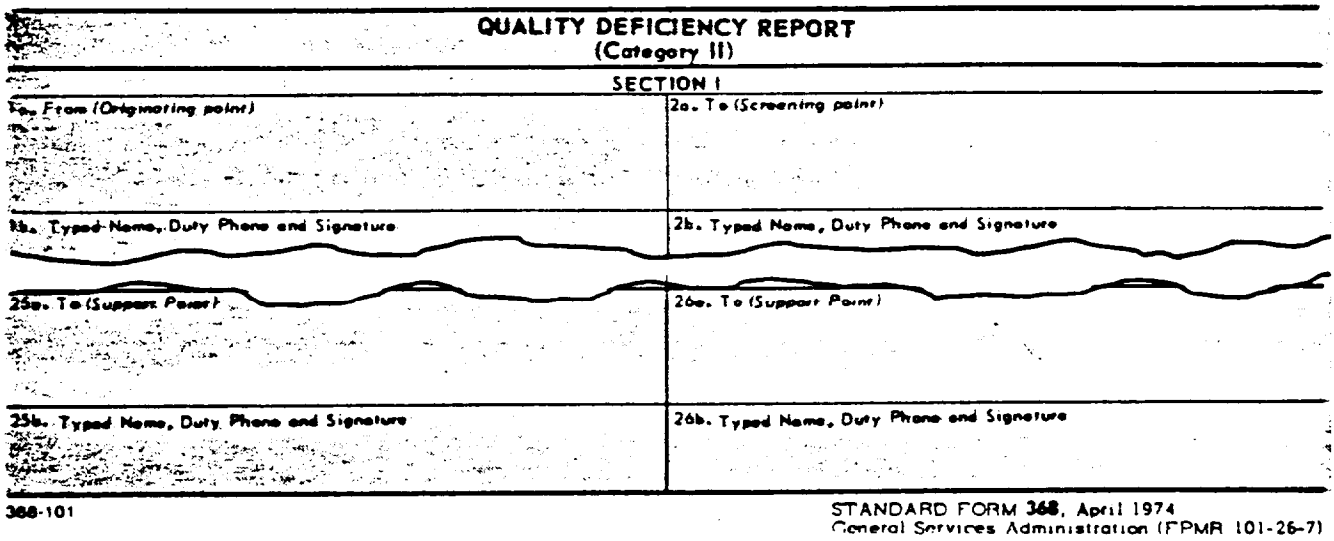
a. Reports of Maintenance and unsatisfactory Equipment. Department of the *Army* forms and procedures used for equipment maintenance will be those prescribed by DA PAM 738-750 as contained in Army Maintenance Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO *P461O. 19D/DLAR* 4500.15.

1-3. Reporting Equipment Improvement Recommendations(EIR)

If your processor Test Set AN/APM-415A needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications- Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.



QUALITY DEFICIENCY REPORT
(Category II)

SECTION I

1a. From (Originating point)

2a. To (Screening point)

1b. Typed Name, Duty Phone and Signature

2b. Typed Name, Duty Phone and Signature

25a. To (Support Point)

26a. To (Support Point)

25b. Typed Name, Duty Phone and Signature

26b. Typed Name, Duty Phone and Signature

368-101

STANDARD FORM 368, April 1974
General Services Administration (FPMR 101-26-7)

NOMENCLATURE CROSS-REFERENCE LIST

1-4. A cross reference of the official and common names of the equipment used in Processor Test Set AN/APM-415A is shown below. You will find that all references to these items are by the common names.

Official Name	Common Name
Processor Test Set AN/APM-415A	Test set
Processor Test Set TS-3706A/APM-415	PTS
Test Set Case CY-7712A/APM-415	Case
Test Adapter Assembly MX-9975/APM-415	Adapter MX
Test Cables W1 through W5	W1 through W5
Electrical Power Cable Assembly SM-C-933053	Power adapter
Magnetic Tape Cassette Transport	MTCT
Card Puller	Extractor
Programmed Tape Cassettes	Cassettes
Radar Signal Indicator IP-1150/APR-39(V)	Display

ABBREVIATIONS

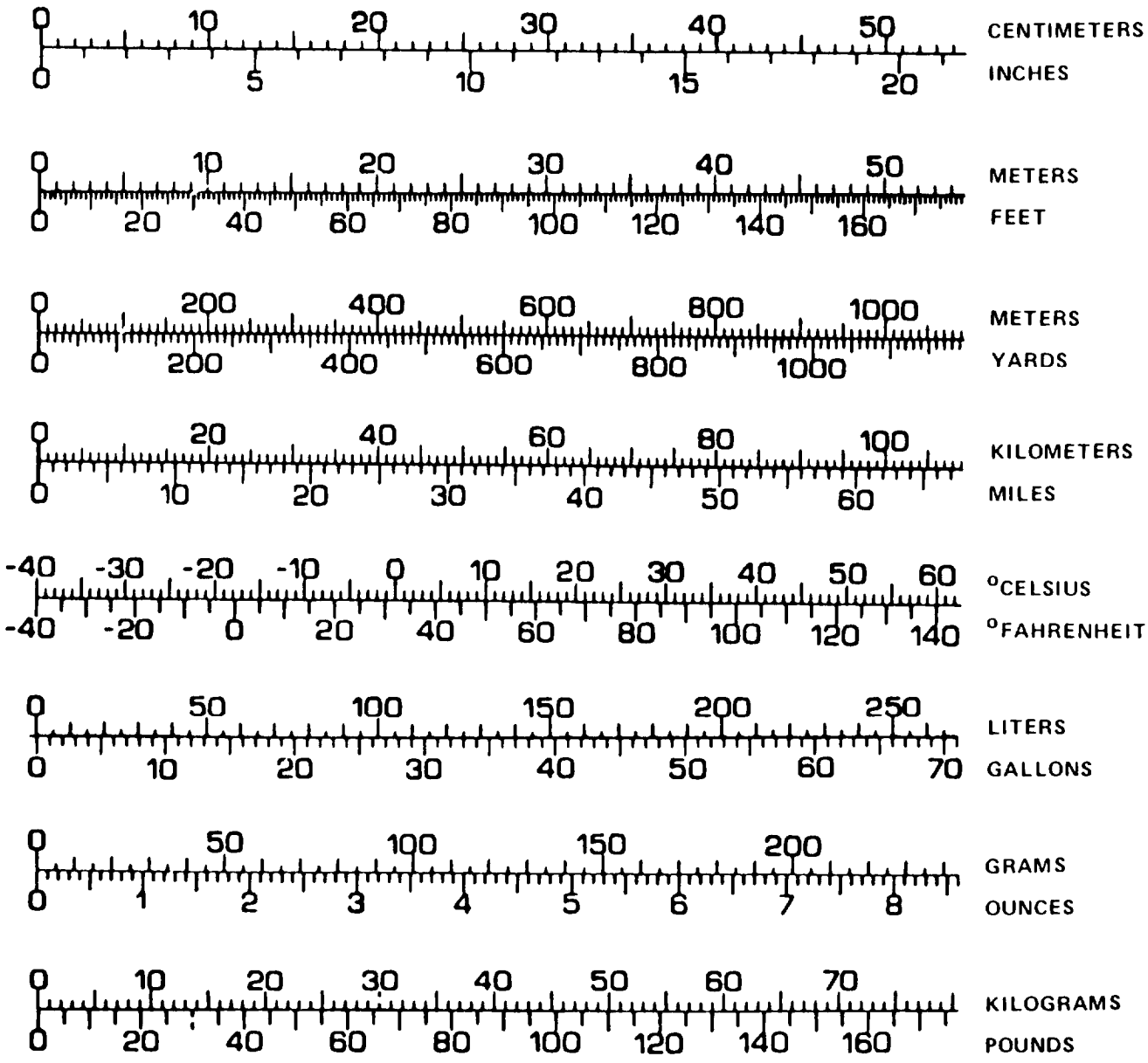
1-5. The following abbreviations are used in this manual. For definitions of terms not listed here, refer to the glossary in the back of this manual.

Abbreviation	Word or Term
ac	alternating current
aft	rear
crt	cathode ray tube
dc	direct current
fwd	forward
Hz	Hertz (cycles per second)
MA	missile alert
MAC	maintenance allocation chart
MWO	modification work order
NSN	national stock number
prf	pulse repetition frequency
pri	pulse repetition interval
PW	pulse width
rf	radio frequency
RPSTL	Repair Parts and Special Tools List
SAM	Surface-To-Air Missile
TAMMS	The Army Maintenance Management System
TMDE	test, measurement, and diagnostic equipment

USE OF METRIC MEASURING SYSTEM

1-6. In this manual, you'll find weights and measurements given in Metric units, with the same measurements in American Standard units shown in parentheses. For example: 30 cm (11.8 in).

Tools, or nuts and bolts that have been manufactured in American Standard units will be described in those units. For example: 1/2 inch hex nut, 3/4 inch bolt, 1/2 inch wrench. Use the following Metric/American Standard table as a measurement guide for any conversions you have to make.



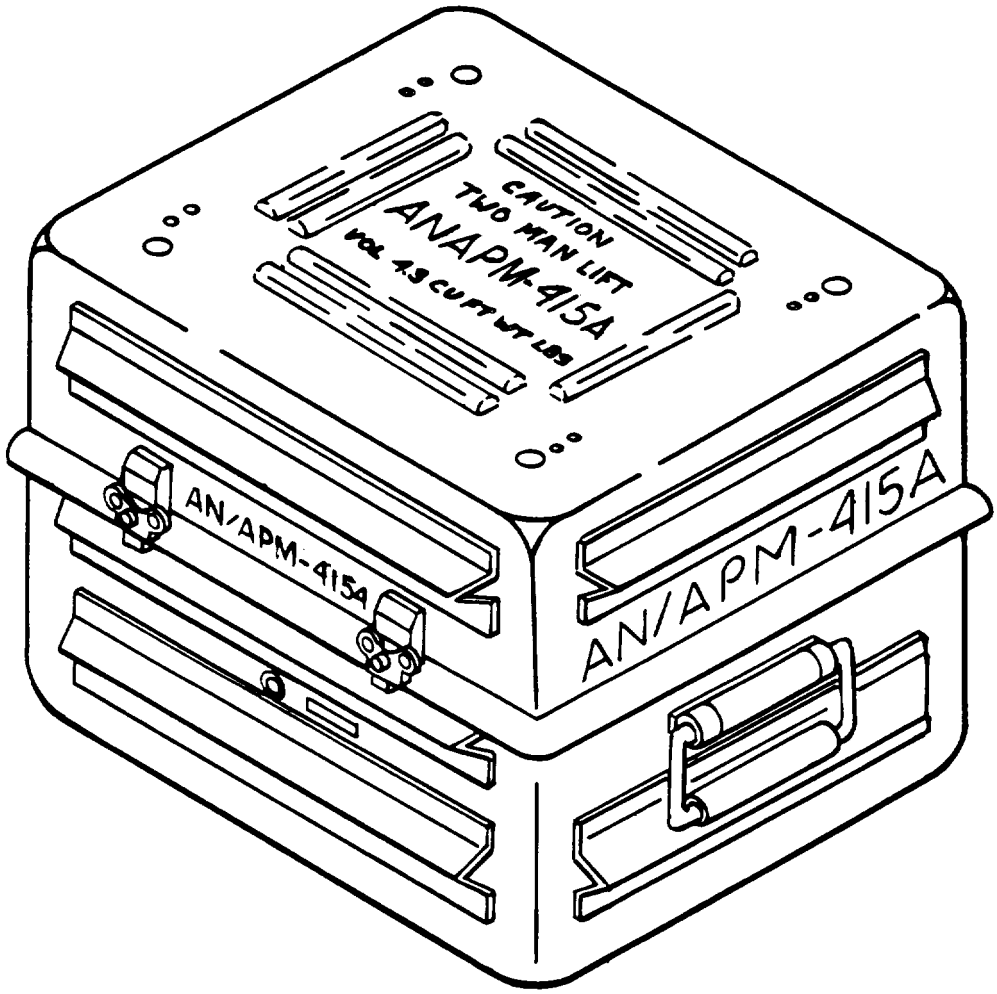
SECTION II

EQUIPMENT DESCRIPTION

SECTION CONTENTS — PAGE

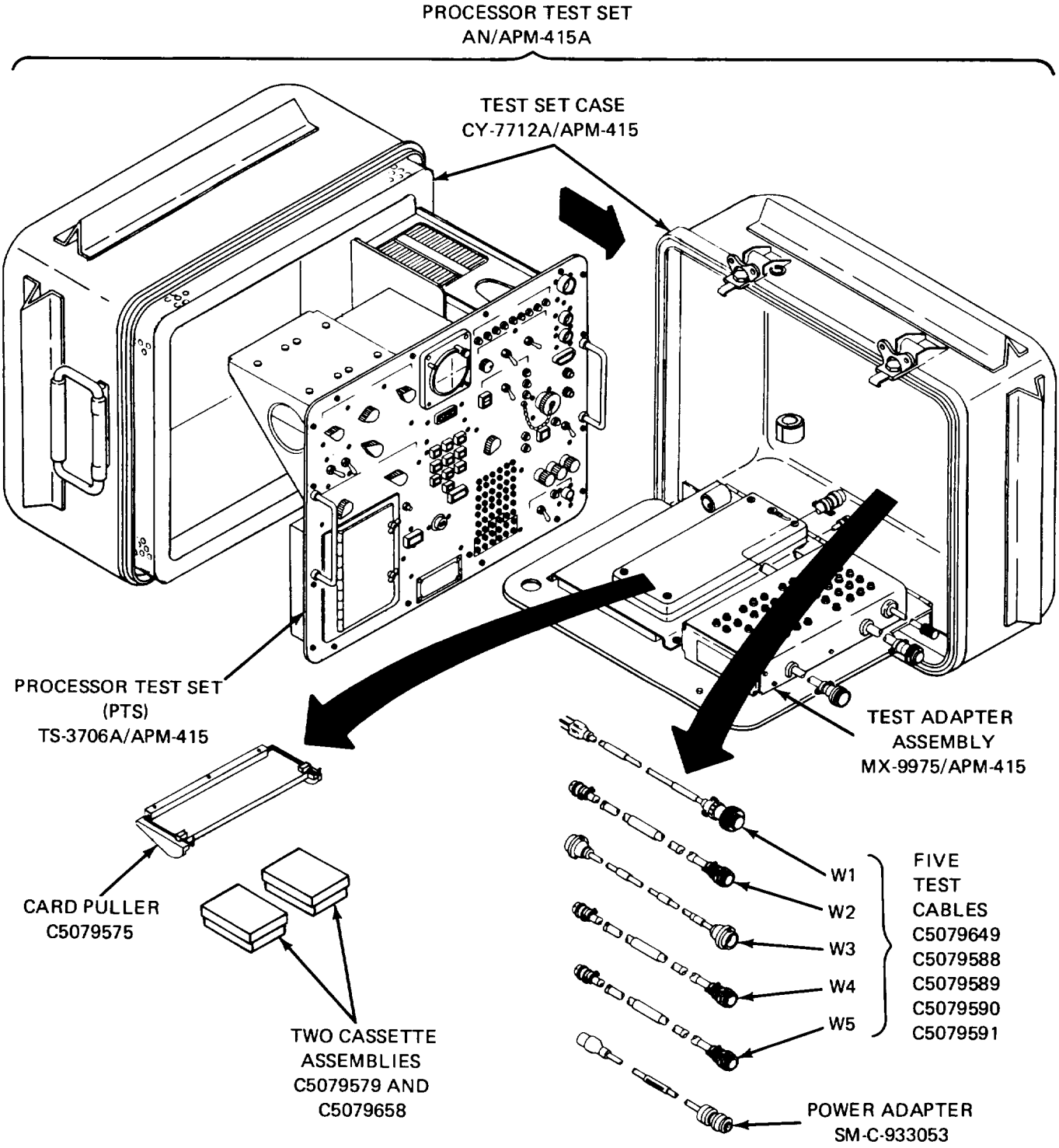
EQUIPMENT PURPOSE, CAPABILITIES, AND FEATURES

1-7. Processor Test Set AN/APM-415A is used to test and maintain Digital Processor CM-480A/APR-39(V) (processor unit) and Detecting Set Control C-10412A/APR-39(V) (control unit) of the Radar Detecting Set AN/APR-39(V)2, at the direct support and general support maintenance levels. The processor test set (test set) provides primary power and stimulus signals for testing and troubleshooting of the processor unit or control unit.



DESCRIPTION OF MAJOR ITEMS

1-8. Processor Test Set AN/APM-415A includes a processor test set TS-3706A/APM-415, a test set case CY-7712A/APM-415, a test adapter assembly MX-9975/APM-415, a power adapter SM-C-933053, five test cables, a card puller and two cassettes. Each item is described in the following paragraphs.



TEST SET CASE CY-7712A/APM-415

The test set case is a metal box that houses all major items of Processor Test Set AN/APM-415A. Four interlock latches are provided to hold the case together. A carrying handle is mounted on each side of the case. In addition, a pressure relief valve is provided on one side of the case. When closed and latched, the case provides protection for all major items of the processor test set during storage or transit.

PROCESSOR TEST SET (PTS) TS-3706A/APM-415

The PTS is housed in one side of the test set case. When the case is opened, the front panel of the PTS is fully exposed. For added protection, the PTS front panel is secured to the test set case. Components of the front panel include controls, indicators, connectors, a magnetic tape cassette transport (MTCT) and a radar signal indicator (display). The overall function of the PTS is to provide power and signal stimuli for testing and, if required, troubleshooting of a processor unit or a control unit.

TEST ADAPTER ASSEMBLY MX-9975/APM-415

The test adapter assembly is used at the depot level to provide interconnection between the processor unit and a radar signal test adapter MX-9848/APR-39(V), which is the “hot mock-up” or test bed for the AN/APR-39(V)1 system. The MX-9975/APM-415 test adapter assembly contains test points which permit monitoring of signals and voltages between the processor unit and the other units of the AN/APR-39(V)1 system by depot maintenance personnel.

TEST CABLES W1 THROUGH W5

The five test cables, W1 through W5, are secured together and are located behind the hinged plate of the test set case. Cable W1 provides a means to connect the PTS to primary power. Cables W2, W3, W4 and W5 are used to interconnect the processor unit and PTS during testing, while cable W3 is used to interconnect the control unit and PTS during testing.

POWER ADAPTER SM-C-933053

Power adapter SM-C-933053 is secured together with test cables W1 through W5. When primary power is 115 Vac, 400 Hz, instead of the normal 115 Vac 50/60 Hz type, power adapter SM-C-933053 is used along with test cable W1 to adapt primary power to the PTS.

CARD PULLER C5079575

Card puller C5079575 is located inside the metal box, which is secured to the hinged plate of the test set case. The card puller is used to extract circuit cards A1 through A5 and A7 through A9, located in the card cage of the PTS.

CASSETTE ASSEMBLIES C5079579 AND C5079658

The two cassette assemblies, C5079579 and C5079658, are located inside the metal box, which is secured to the hinged plate of the test set case. Each assembly contains a cassette tape; namely, PUT diagnostic tape MTC5079655, located inside assembly C5079579, and PTS memory verification tape MTC5079654, located inside assembly C5079658.

DIFFERENCES BETWEEN MODELS

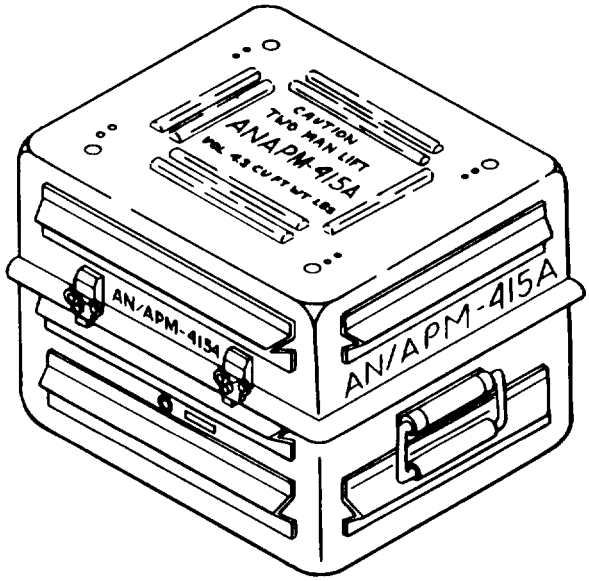
1-9. Only one model of the processor test set exists, therefore there is no difference between models.

PHYSICAL DATA

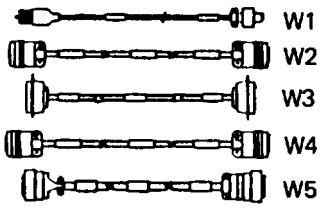
1-10. The dimensions and weights of Processor Test Set AN/APM-415A are provided below:

PROCESSOR TEST SET AN/APM-415A

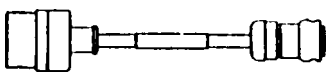
- **HEIGHT: 16 IN.**
- **WIDTH: 20.5 IN.**
- **LENGTH: 16.9 IN.**
- **WEIGHT: 82 LB.**



TEST CABLES



POWER ADAPTER



TEST CABLES	LENGTH
● W1	96 IN.
● W2	36 IN.
● W3	36 IN.
● W4	36 IN.
● W5	36 IN.

POWER ADAPTER: 9 IN. LONG

PERFORMANCE DATA

1-11. The performance data for Processor Test Set AN/APM-415A is provided below:

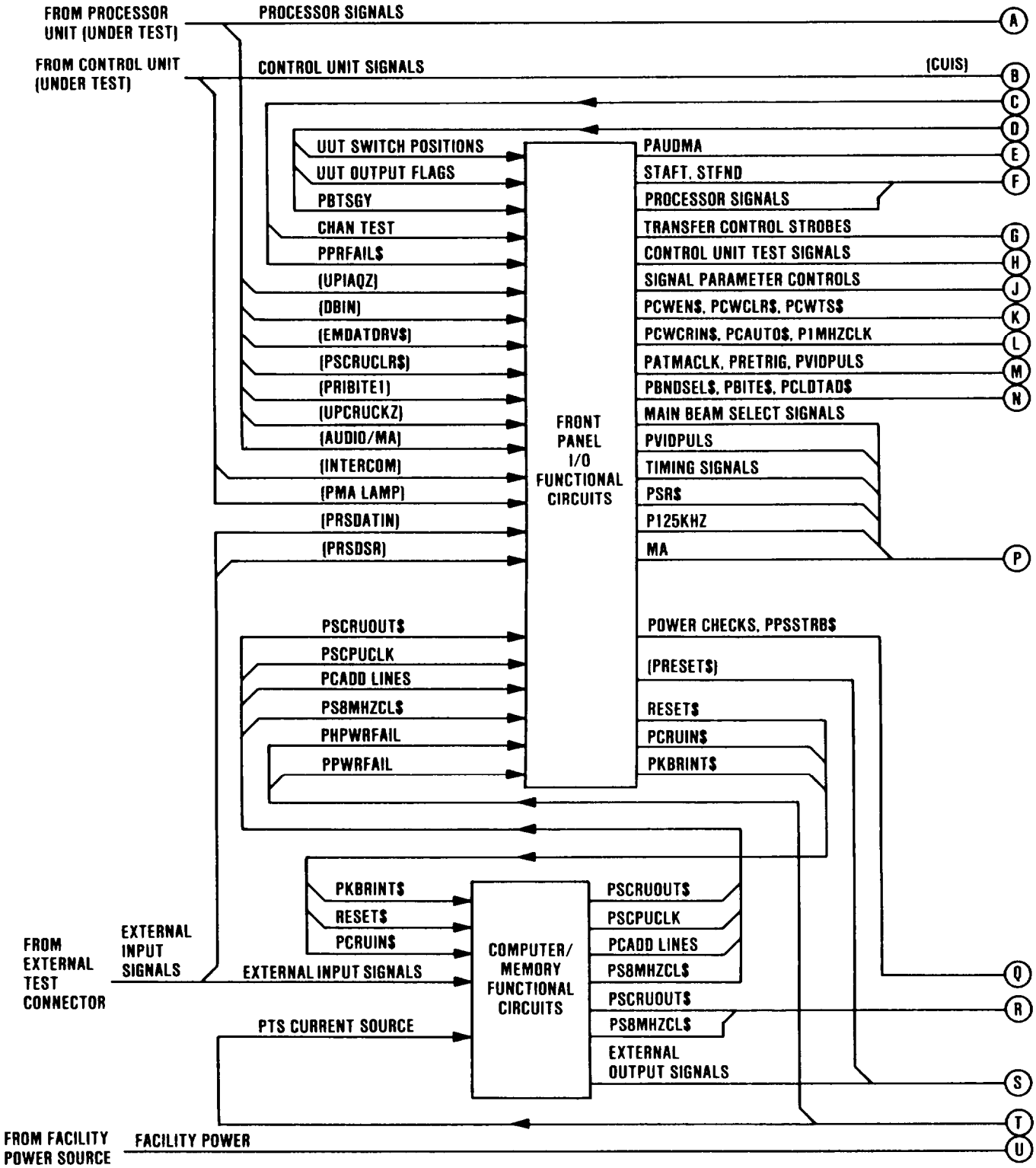
- Operates on 115 Vac 50/60 Hz single phase power or 115 Vac 400 Hz single phase power, using power adapter SM-C-933053.
- Permits operational checkout and, if required, troubleshooting of digital processor unit CM-480A/APR-39(V) or detecting set control unit C-10412A/APR-39(V) of radar detecting set AN/APR-39(V)2.
- Permits operator initiated self-test of the PTS with pass/fail and error message indications.
- Contains a radar signal indicator which is identical to aircraft radar signal indicator unit 1P-1150/APR-39(V) of radar detecting set AN/APR-39(V)2.
- Contains a magnetic tape cassette transport (MTCT) for loading cassette programs into the PTS or digital processor unit at the intermediate or depot maintenance levels.

CHAPTER 2
FUNCTIONING OF EQUIPMENT

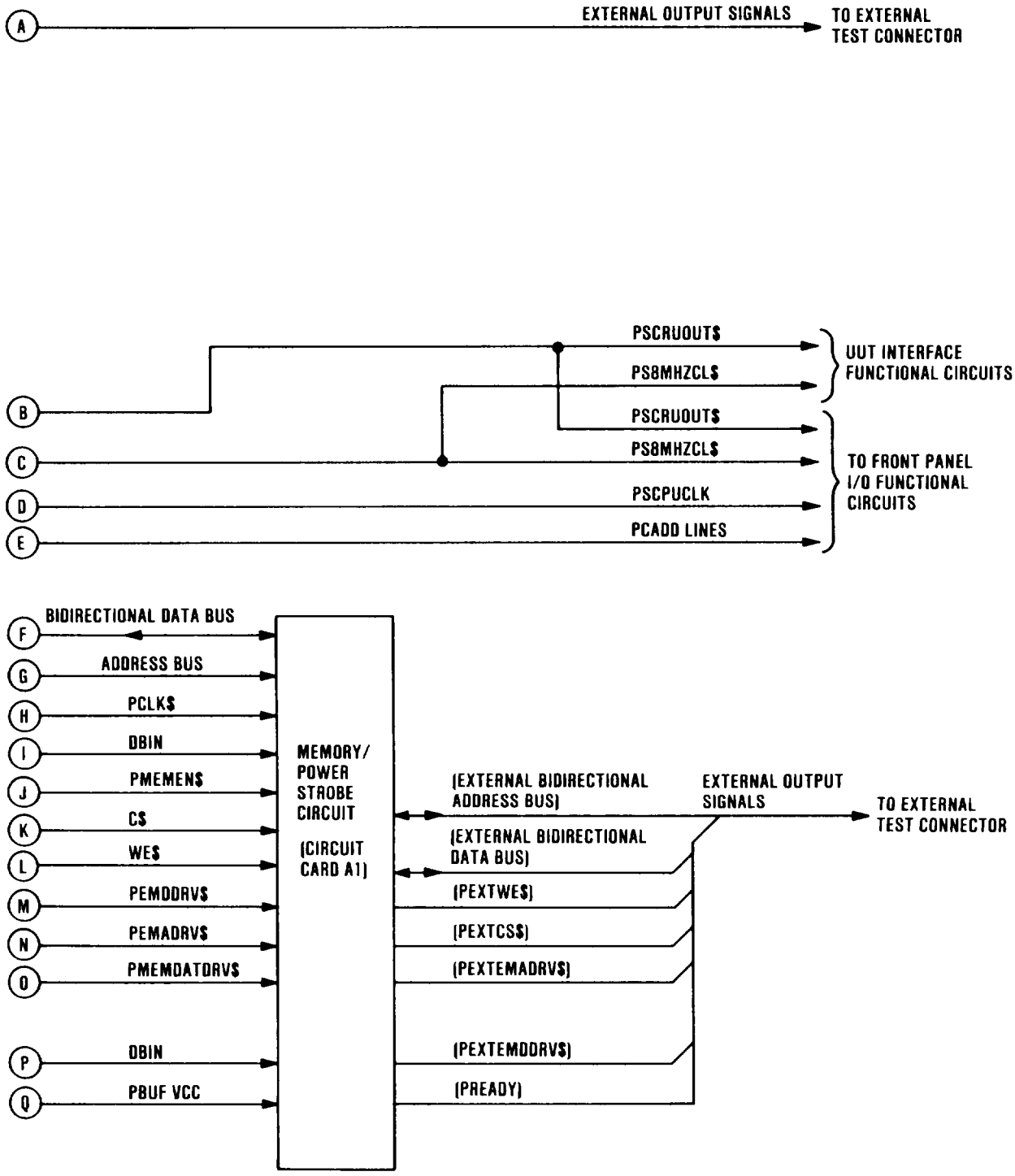
SECTION I
OVERALL FUNCTIONAL DISCUSSION

SCOPE

2-1. The principles of operation for the PTS are contained in this chapter. Section I provides the block diagram of the PTS. This diagram depicts five functional areas (which comprise the basic functions) of the PTS. Section II provides a breakdown into major circuits comprising each of the basic functions depicted in section I. Section Ill provides a detailed block diagram discussion of each of the circuits comprising the basic functions depicted in section Il.



PTS Overall Block Diagram (Sheet l of 5)



Computer/Memory Functional Circuits (Sheet 2 of 3)

COMPUTER/MEMORY FUNCTIONAL CIRCUITS

The computer/ memory functional circuits contain the operational program, and when executed, control the functional operation of the PTS. The components of the computer/memory functional circuits are the computer/DMA circuit and memory/power strobe circuit.

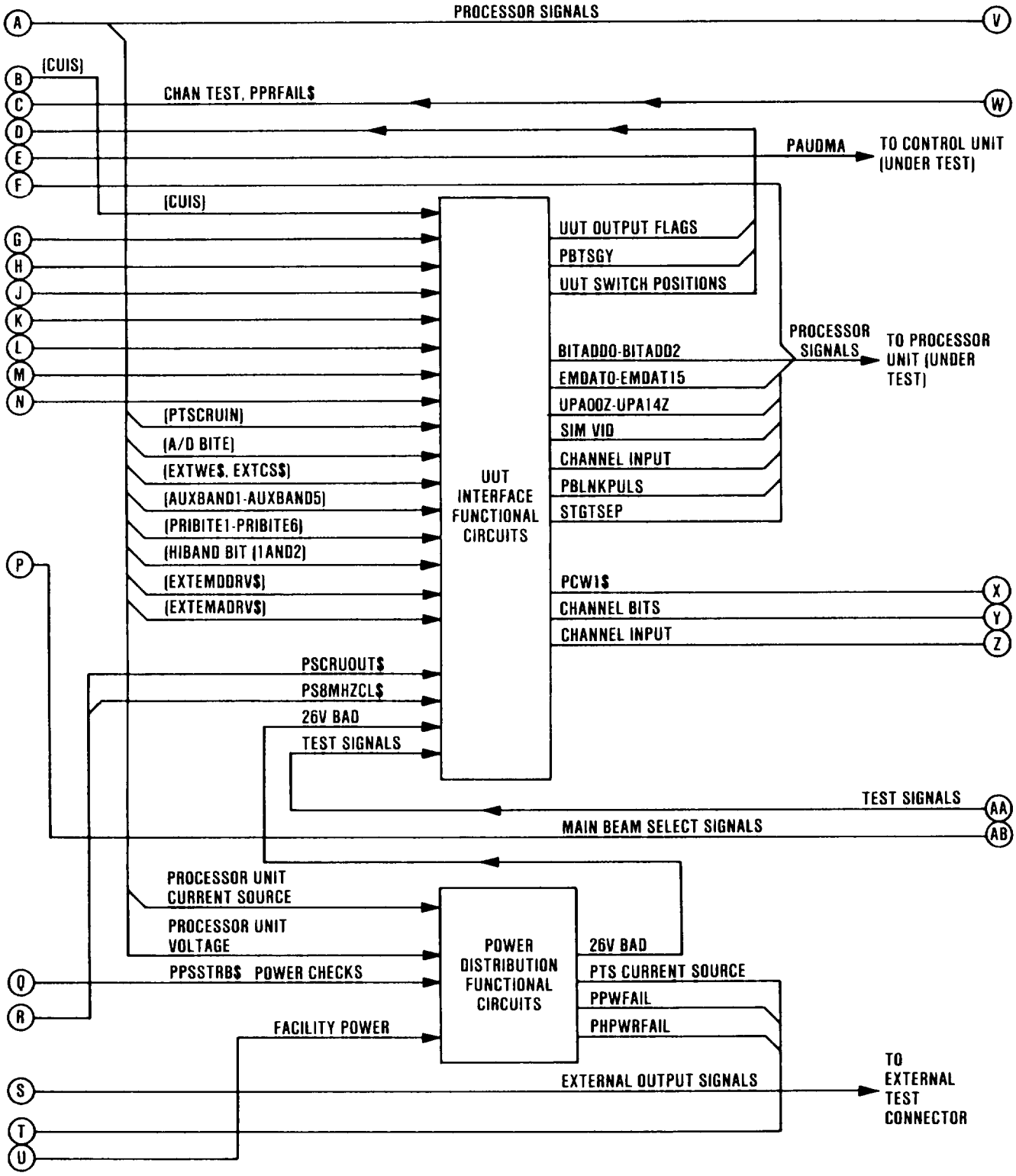
COMPUTER/DMA CIRCUIT

The computer/DMA circuit implements the instructions contained in the operational program. The computer/DMA circuit also contains several components reserved for future expansion.

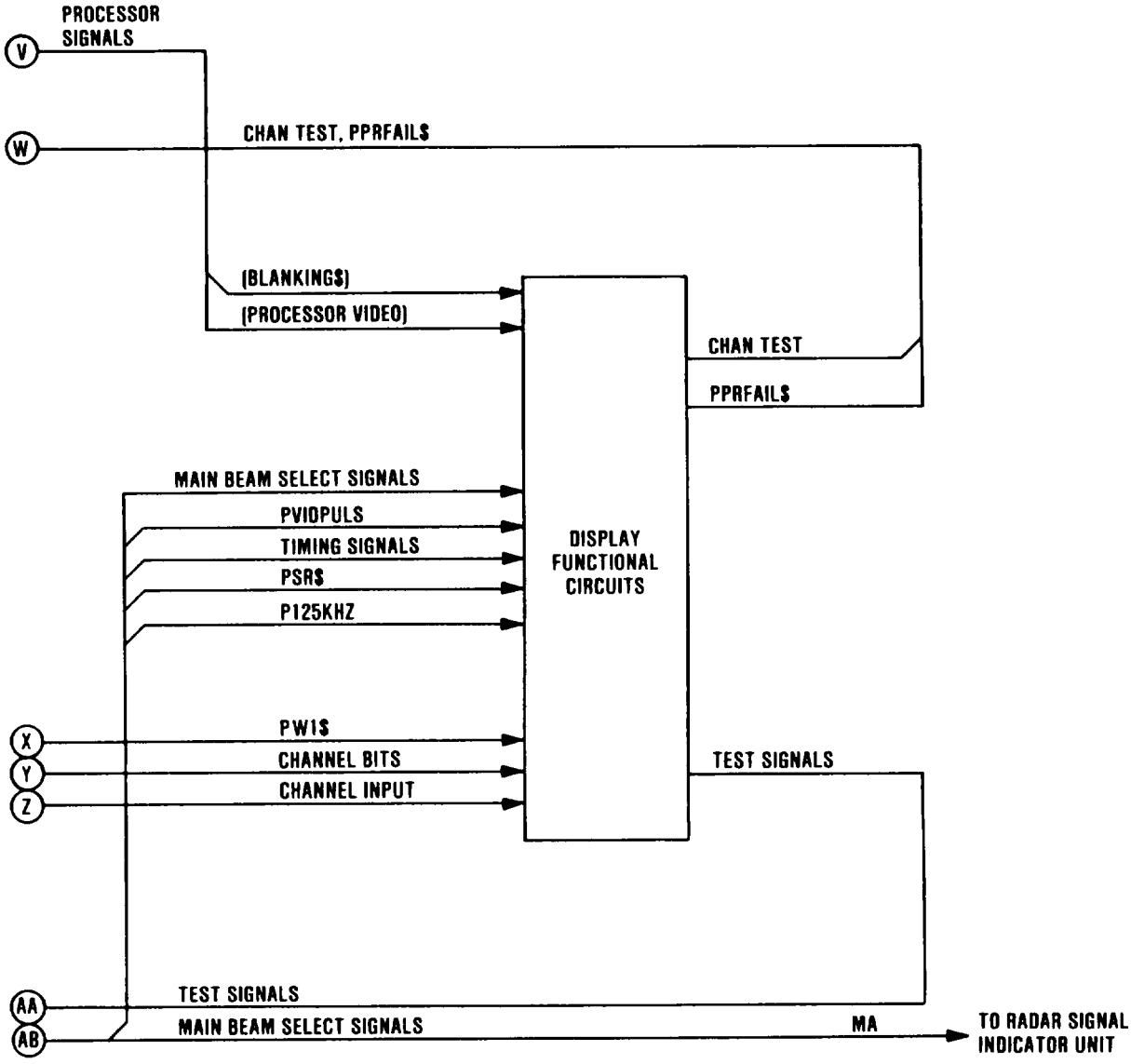
MEMORY/POWER STROBE CIRCUIT

The memory/power strobe circuit provides permanent storage of the operational program in programmable read only memory (PROM) and temporary storage for scratch pad purposes in random access memory (RAM). In addition, this circuit provides buffers which permit transfer of data, addresses and commands to and from the external equipment.

Computer/Memory Functional Circuits (Sheet 3 of 3)



PTS Overall Block Diagram (Sheet 2 of 5)



PTS Overall Block Diagram (Sheet 3 of 5)

PTS OVERALL BLOCK DIAGRAM

The PTS is comprised of five basic functional circuits; namely, computer/memory, front panel I/O, UUT interface, display and power distribution. The computer/memory functional circuits are comprised of a computer/DMA circuit (contained on circuit card A2) and memory/power strobe circuit (contained on circuit card Al). The front panel I/O functional circuits are comprised of a front panel circuit, an analog control interface circuit (contained on circuit card A4), an analog signal interface circuit (contained on a portion of circuit card A9), a computer interface circuit (contained on circuit card A5) and an MTCT circuit. The UUT interface functional circuits are comprised of a digital signal processor (contained on circuit card A3), a video generator circuit (contained on a portion of circuit card A7) and a display protect circuit (contained on a portion of circuit card A8). The display functional circuits are comprised of a video generator circuit (contained on a portion of circuit card A7), a display protect circuit (contained on a portion of circuit card A8), and a radar signal indicator unit. The power distribution functional circuits are comprised of a distribution circuit, power supply PS1, and an analog signal interface circuit (contained on a portion of circuit card A9). All of these functional areas operate together to exercise the functional components of either a processor unit or control unit.

When power is first applied, the PTS performs an initialization routine, which clears all counters, registers and latches. The computer/memory functional circuits begin to receive instructions from the operational program stored in permanent memory. These instructions sequence the computer/memory functional circuits to initiate a test of the PTS power supply voltages and current source, and check the status of the front panel switches to determine if the PTS is to function in the auto or manual mode of operation. In the auto mode of operation, test signal parameters are selected in accordance with instructions contained in the operational program. In the manual mode of operation, test signal parameters are selected by the operator through the use of front panel switches.

If the unit to be exercised is a processor unit, testing begins when the front panel UUT switch is set to ON. The computer/memory functional circuits develop the appropriate commands to direct the other functional circuits of the PTS to develop simulated radar receiver output pulses. The pulses are developed in accordance with commands from the front panel l/O functional circuits. These commands dictate the various pulse parameters (selected by either program instructions or front panel switch settings) for the simulated radar receiver output pulses generated by the UUT interface functional circuits. The simulated radar receiver output pulses, once generated, are applied to the processor unit (under test). The processor unit accepts the pulses and performs an analysis of the pulse parameters in the same manner as performed in the system environment. The analysis results in the development of video signals that are returned to the PTS. The video signals are checked to ensure that the parameters are within acceptable limits, and then, if accepted, applied to the radar signal indicator unit. Since the parameters of the original simulated radar receiver output pulse are known, the type and positioning of the response shown on the radar signal indicator unit can be anticipated.

PTS Overall Block Diagram (Sheet 4 of 5)

Determination of operational status is made by checking the actual response against the anticipated response. Through the use of preprogrammed diagnostic tapes, in conjunction with the BITE ADDRESS SELECT switch, front panel TEST POINTS and supportive test equipment, the functional status of each of the individual functional circuits of the processor unit (under test) can be accurately determined.

If the unit to be exercised is a control unit, testing begins when the PTS completes its initialization routine. The operator sets the control unit switches to their various positions, exercising the switch encoder circuit in the control unit. The output of the control unit is then decoded by the PTS, and used to turn on front panel indicators. A comparison of which indicator has turned on versus switch and switch position selected, provides an indication as to the operational status of the control unit. The aural and MA lamp outputs of the control unit are checked by software instructions under control of the computer/memory functional circuits. These checks are performed by applying a computer generated audio input to the control unit, and then checking the returned signals.

The PTS also performs a self-test of its own functional circuits to provide the operator with an indication of the functional status of the PTS. The self-test is performed by the computer/memory functional circuits in accordance with software instructions. This test first exercises the various signal control circuits through parity checks, and then checks, in sequence, the signal generating circuits and response processing circuits.

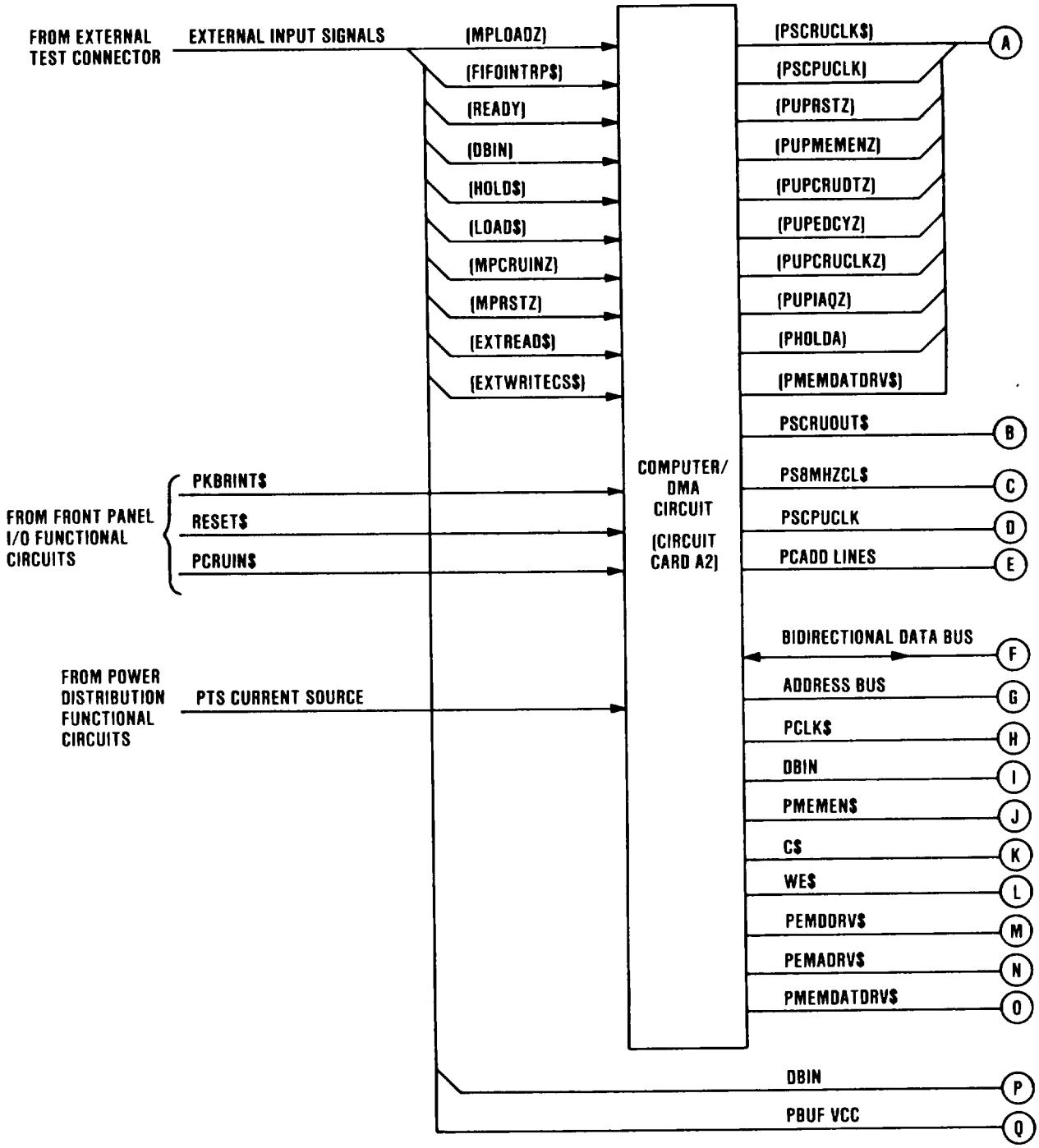
PTS Overall Block Diagram (Sheet 5 of 5)

SECTION II
BASIC FUNCTIONAL DISCUSSION

SECTION CONTENTS PAGE

INTRODUCTION

2-2. The following paragraphs describe the basic functional circuits of the PTS. Each discussion is supported by a basic functional diagram.



Computer/Memory Functional Circuits (Sheet 1 of 3)

FRONT PANEL I/0 FUNCTIONAL CIRCUITS

The front panel I/0 functional circuits provide the means by which commands and test signals are generated in response to either the front panel switches or software program to control the development of test signal parameters; and data, flags, control signals and response signals are transferred from the computer/memory functional circuits, to and from various circuits of the PTS and processor unit (under test) to allow software control of the testing sequence. These circuits also control the functional operation of the MTCT circuit to provide for the transfer of program instructions and data from a preprogrammed tape to the computer/memory functional circuits. The front panel I/0 functional circuits are comprised of the front panel circuit, analog control interface circuit (circuit card A4), analog signal interface circuit (P/O circuit card A9), computer interface circuit card (circuit card A5), and the MTCT circuit.

FRONT PANEL CIRCUIT

The front panel circuit contains the various switches and indicators that are located on the PTS front panel. The functional operations of these switches and indicators are incorporated into the block diagrams and described in subsequent discussions of the various circuits that comprise the front panel I/0 functional circuits.

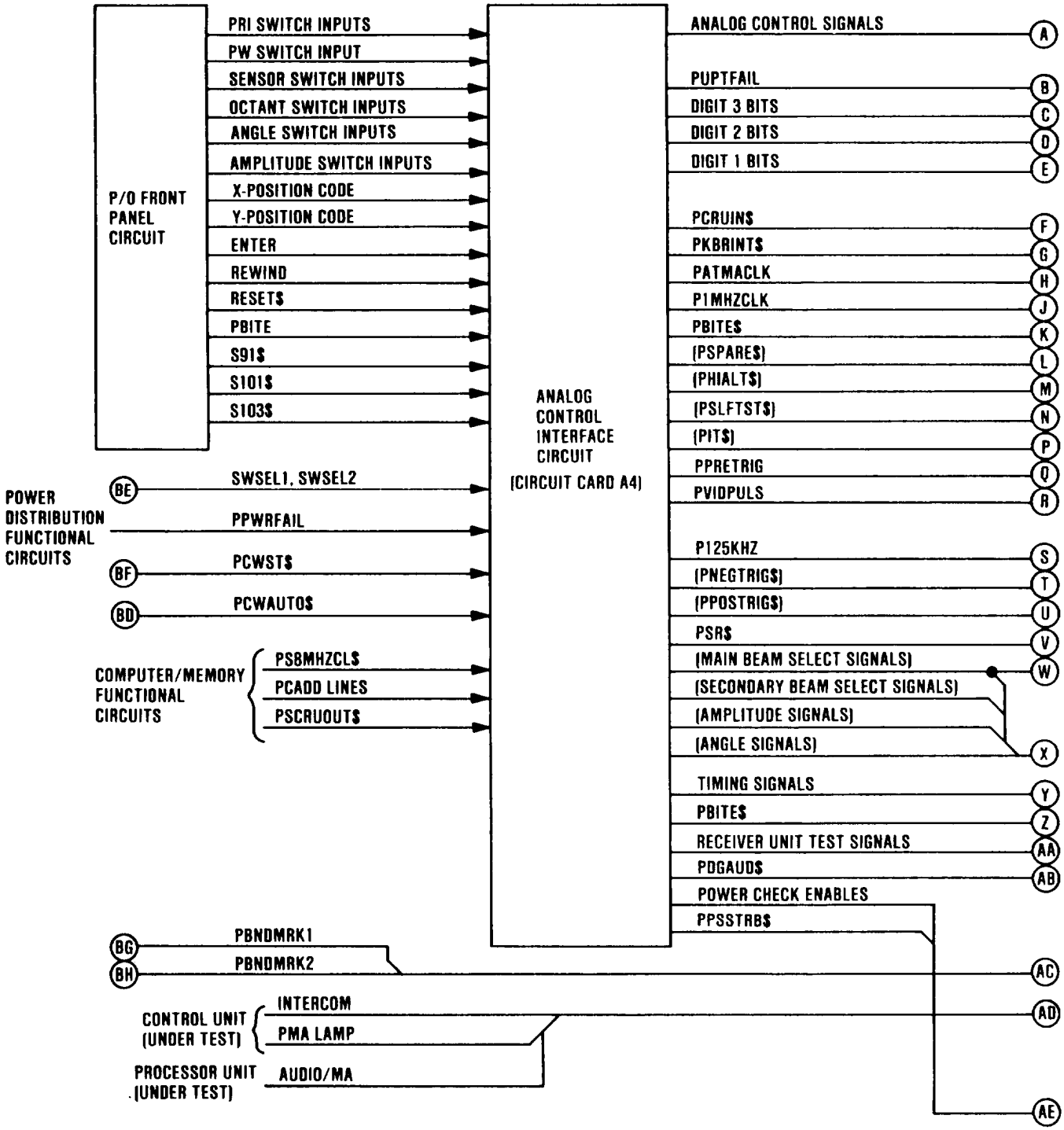
ANALOG CONTROL INTERFACE CIRCUIT

The analog control interface circuit controls the generation of commands and test signals in response to either the manual setting of front panel switches or the software program. These commands and test signals control the functional operation of the other functional circuits of the PTS. The analog control interface circuit also provides the means for inputting test instructions via the TEST SELECT keypad switches.

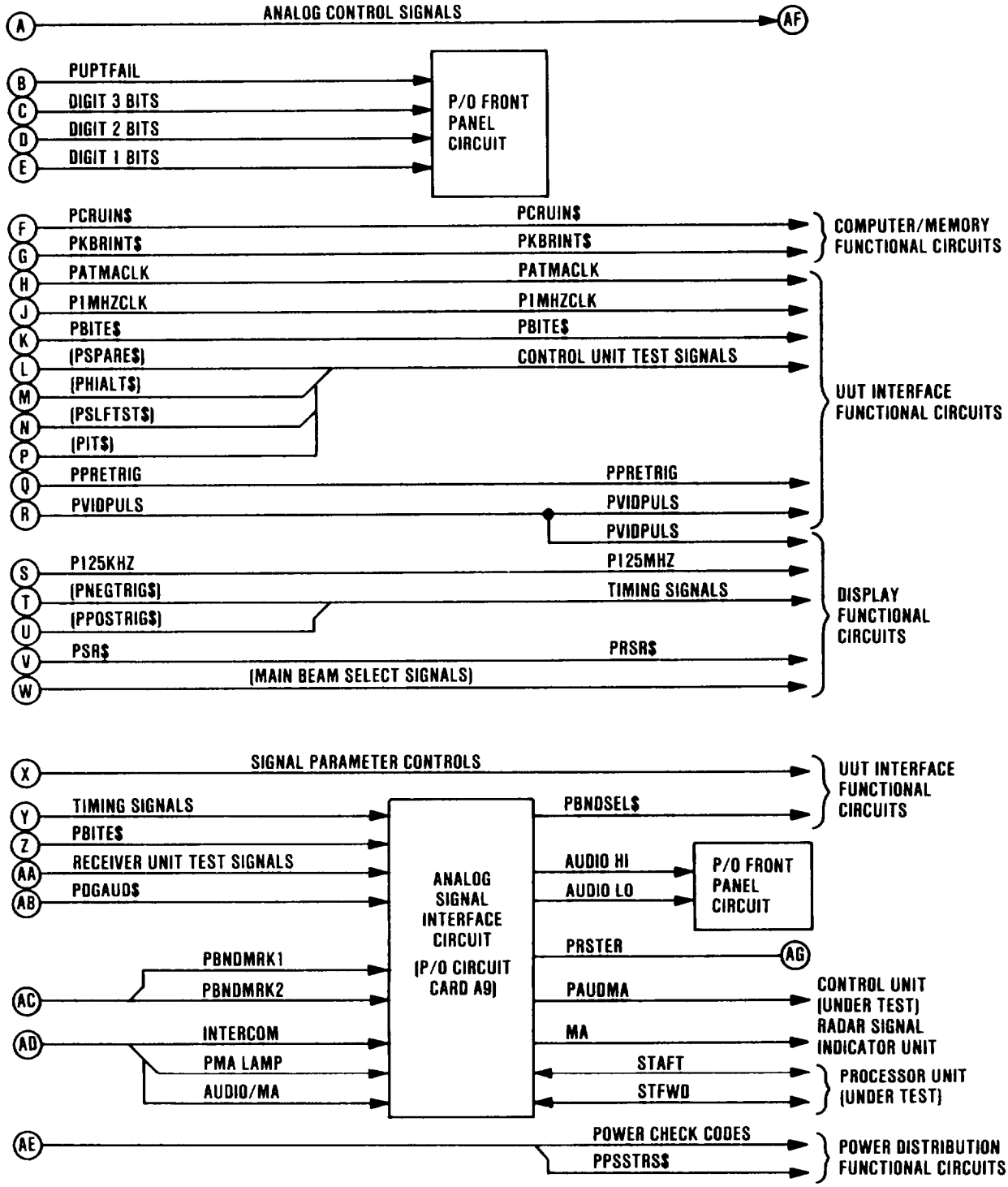
ANALOG SIGNAL INTERFACE CIRCUIT

The analog signal interface circuit controls testing of the audio circuits contained within the processor unit and control unit. This circuit also controls the testing of the STAFT and STFWD messages, both generated and received by the processor unit (under test).

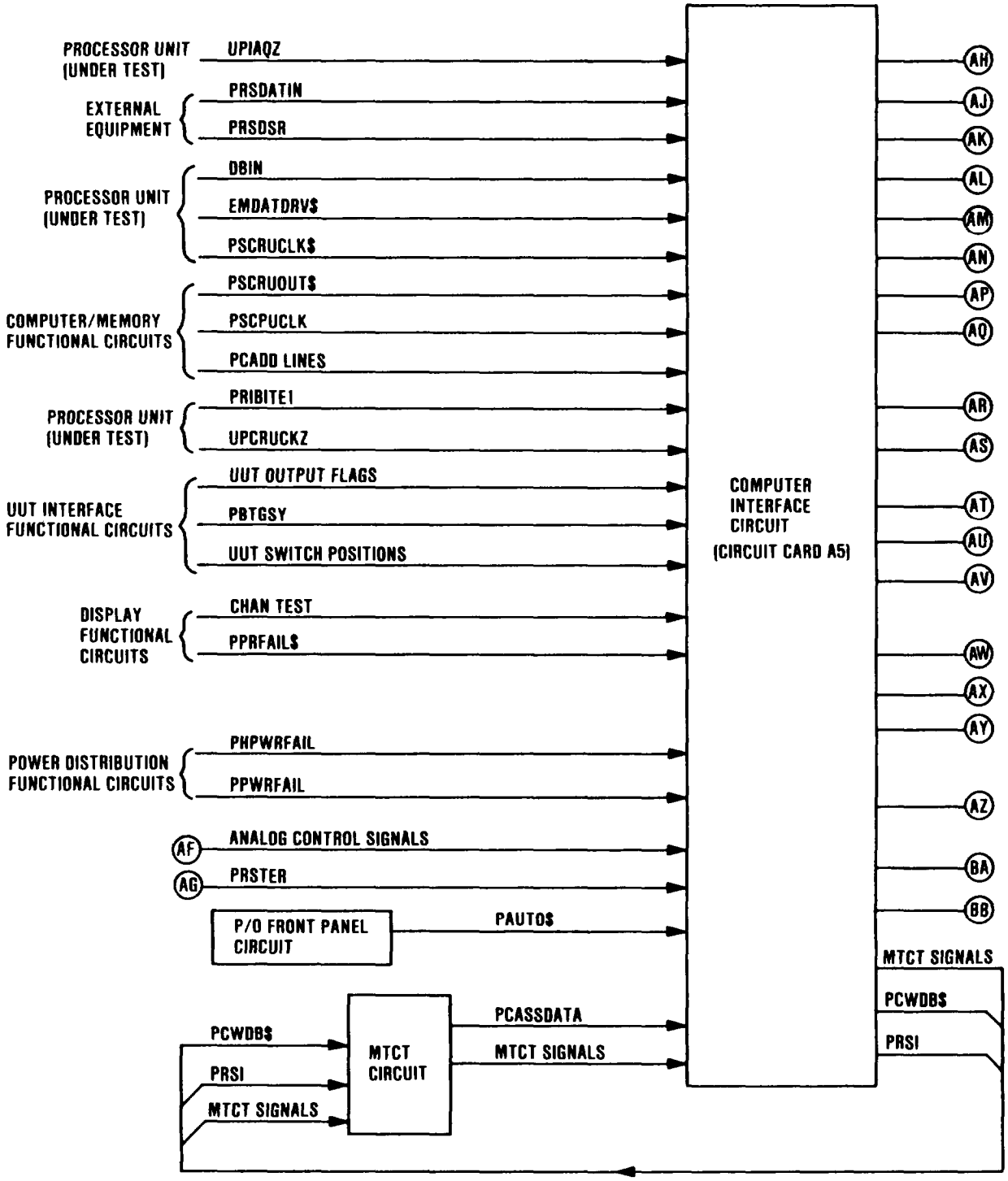
Front Panel I/0 Functional Circuits (Sheet 1 of 6)



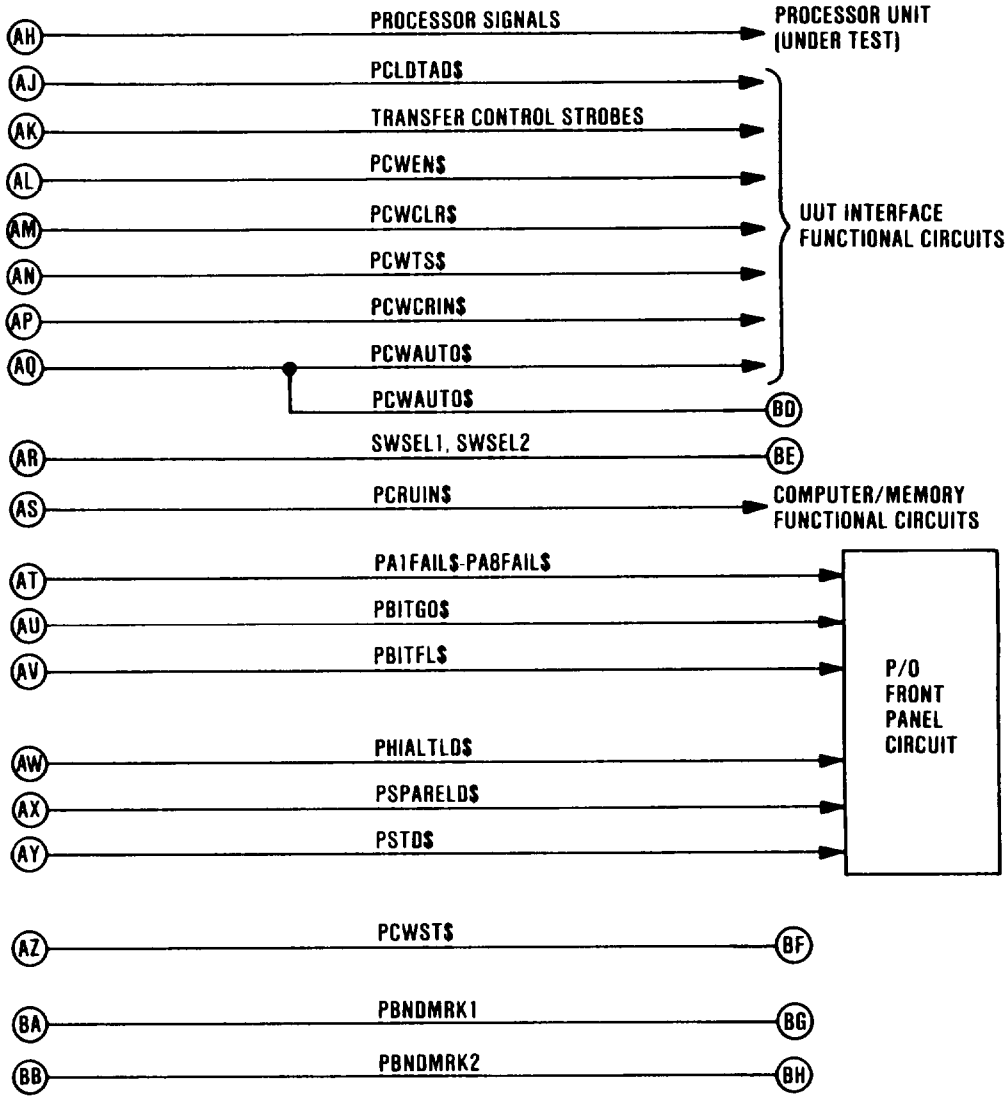
Front Panel I/0 Functional Circuits (Sheet 2 of 6)



Front Panel I/O Functional Circuits (Sheet 3 of 6)



Front Panel I/O Functional Circuits (Sheet 4 0f 6)



Front Panel I/0 Functional Circuits (Sheet 5 of 6)

COMPUTER INTERFACE CIRCUIT

The computer interface circuit, under control of the computer software program, controls the transfer of data, flags, control signals and response signals from the computer/memory functional circuits to and from the various circuits of the PTS and the processor unit (under test).

MTCT CIRCUIT

The MTCT circuit receives data and control inputs (PCWDB$, PRSI and MTCT SIGNALS) from the computer interface circuit. These signals control the functional operations of the MTCT circuit as well as data transfer from a preprogrammed (magnetic) tape. The MTCT circuit applies the data read from the tape (PCASSDATA) and response signals (MTCT SIGNALS) to the computer interface circuit.

Front Panel I/O Functional Circuits (Sheet 6 of 6)

UUT INTERFACE FUNCTIONAL CIRCUITS

The UUT interface functional circuits provide the means for controlling the testing process through test data, command and response signal transfer between the PTS and the processor unit (under test); simulation of radar receiver output pulse used for testing the input signal processing circuits of the processor unit (under test); simulation of test signals for, and testing of response signals from the control unit (under test); and generation of self-test signals for testing of the PTS circuits. The UUT interface functional circuits are comprised of the digital signal processor circuit (circuit card A3), video generator circuit (P/O circuit card A7) and display protect circuit (P/O circuit card A8).

DIGITAL SIGNAL PROCESSOR CIRCUIT

The digital signal processor circuit provides the means for transferring test control signals and test data to the processor unit (under test) to control the testing process; and transferring response signals from the processor (under test) to the front panel l/O functional circuits to monitor the testing process. The circuit also develops switch data to set up test conditions and interconnect various points within the processor unit (under test) to test points on the front panel of the PTS.

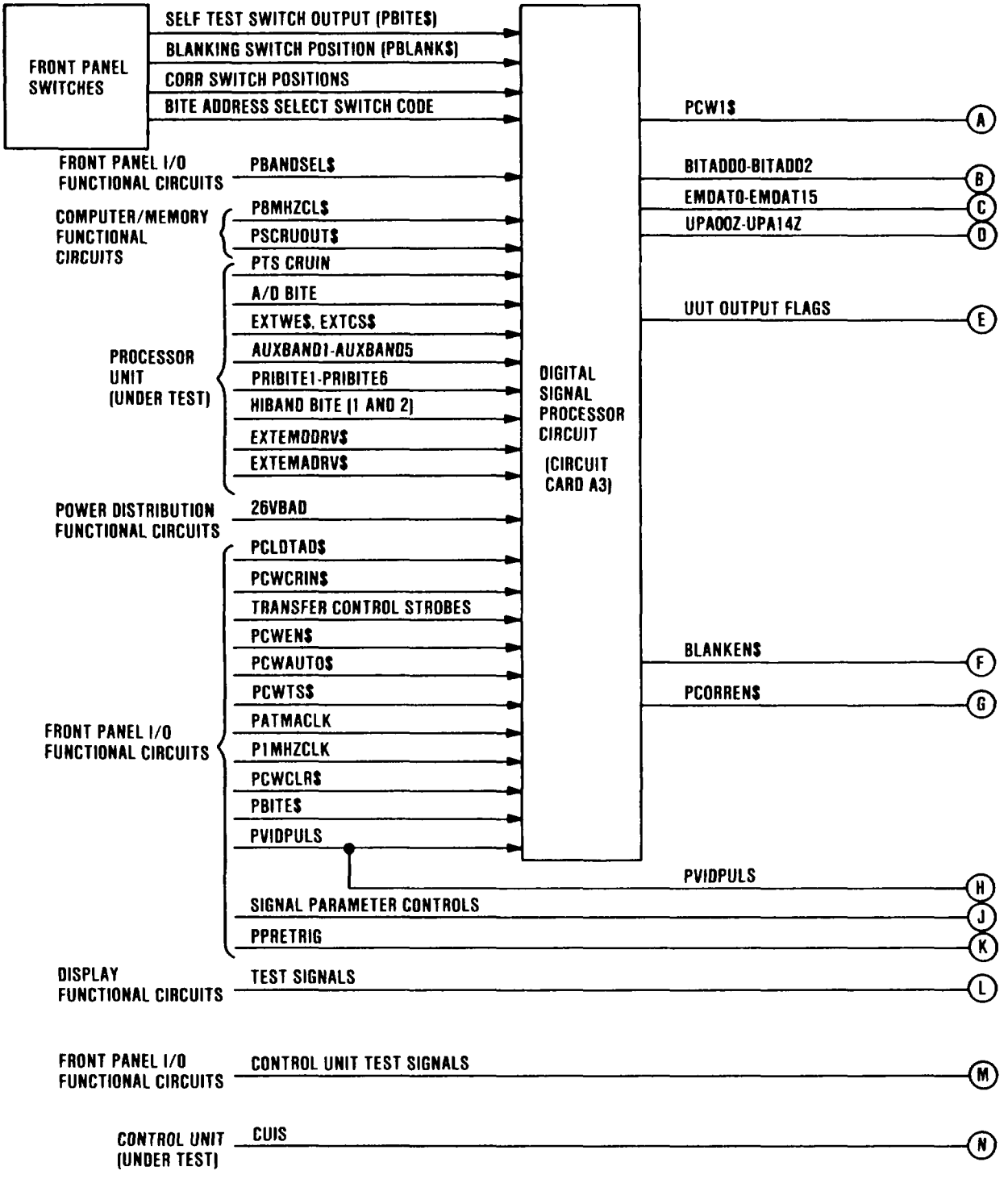
VIDEO GENERATOR CIRCUIT

The video generator circuit simulates radar receiver output pulses and the blanking pulse, in the test mode of operation, to test the input signal processing circuits of the processor unit (under test). This circuit also selects strobes, in the self-test mode of operation, to test the functional operation of the PTS, as well as developing sync outputs used in self-test and maintenance procedures.

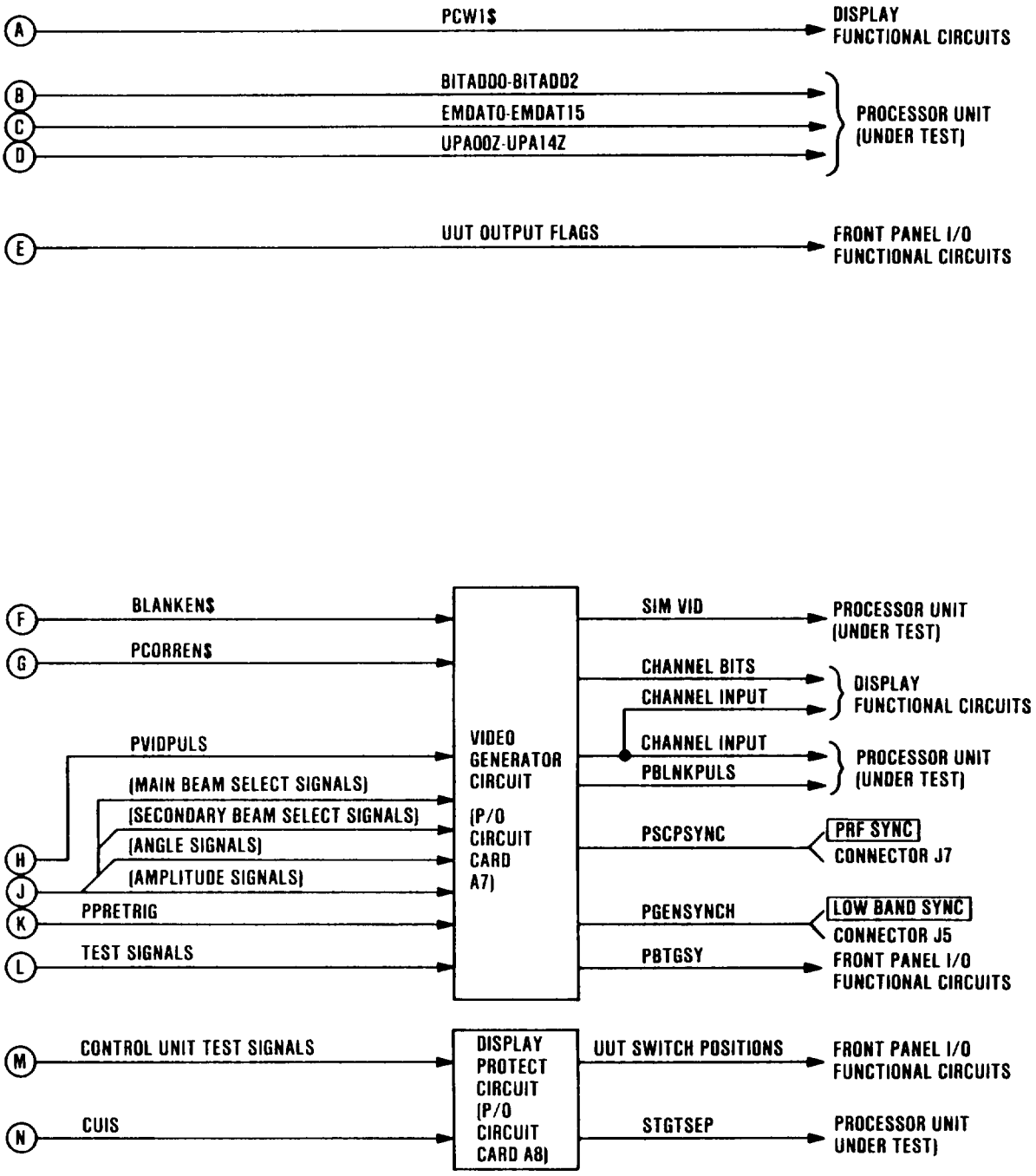
DISPLAY PROTECT CIRCUIT

The display protect circuit checks the functional operation of the control unit (under test) switch encoder circuit, processor unit (under test) switch decoder circuit, and PTS switch simulation circuits to determine the functional status of these circuits.

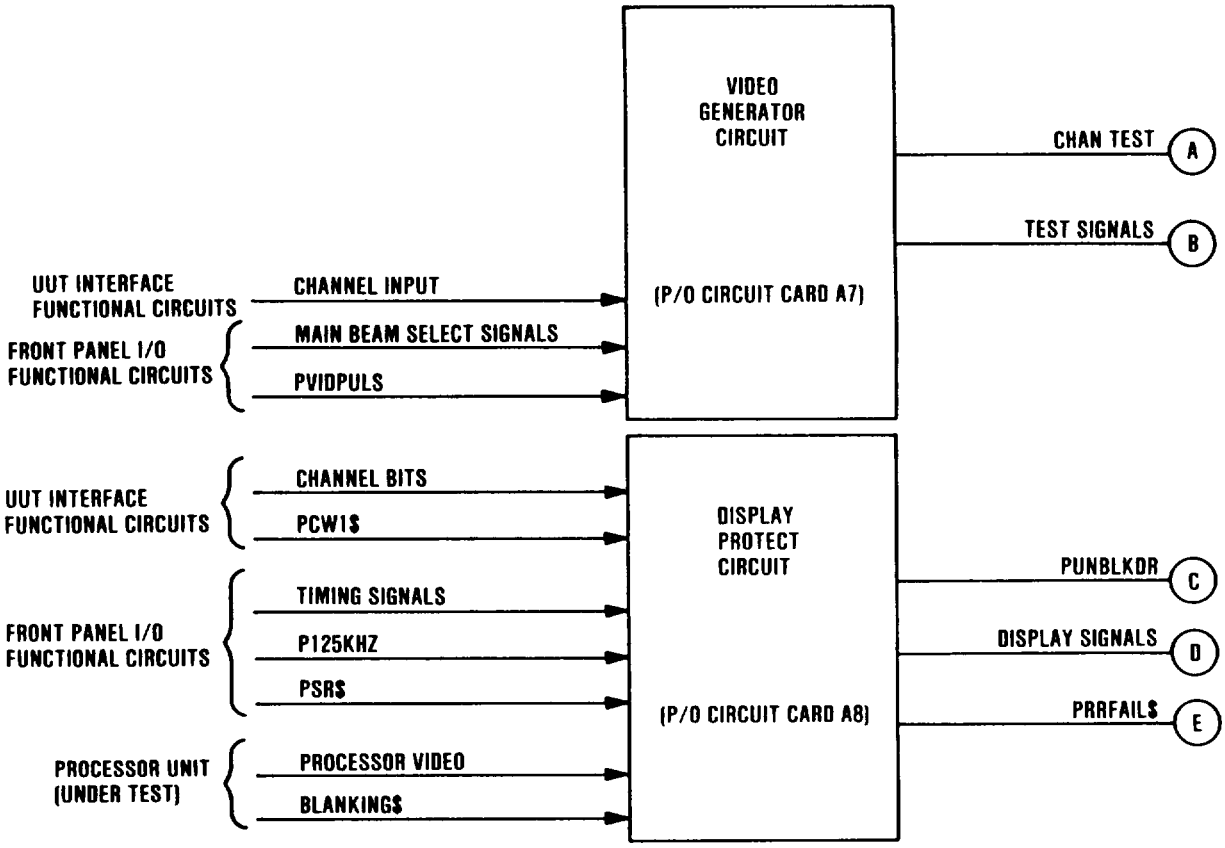
UUT Interface Functional Circuits (Sheet 1 of 3)



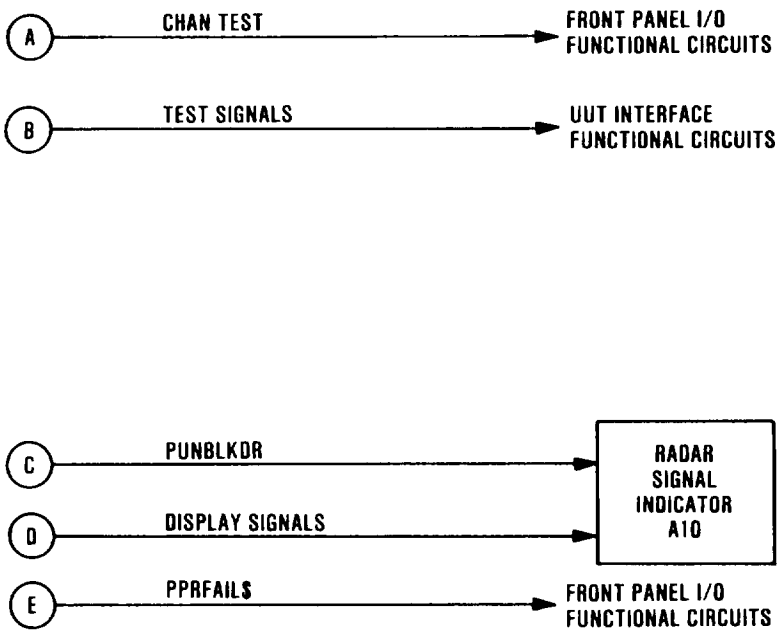
UUT Interface Functional Circuits (Sheet 2 of 3)



UUT Interface Functional Circuits (Sheet 3 of 3)



Display Functional Circuits (Sheet 1 of 3)



Display Functional Circuits (Sheet 2 of 3)

DISPLAY FUNCTIiONAL CIRCUITS

The display functional circuits develop, test and apply the signals, which develop the visual display provided on the radar signal indicator unit. The display functional circuits are comprised of the video generator circuit (P/O circuit card A7), display protect circuit (P/O circuit card A8), and the radar signal indicator unit.

VIDEO GENERATOR CIRCUIT

The video generator circuit develops the pulse signals (TEST SIGNALS) required to drive the UUT interface functional circuits to produce simulated radar receiver output pulses. The video generator circuit also produces a test signal (CHAN TEST), used in the self-test mode, to partially check the functional operation of the UUT interface functional circuits.

DISPLAY PROTECT CIRCUIT

The display protect circuit performs two basic functions. First, this circuit samples the video pulses generated by the processor unit (under test) to ensure that the pulses are within accepted limits. Second, this circuit (in the self-test mode of operation) generates the test strobes displayed on the radar signal indicator unit.

RADAR SIGNAL INDICATOR

The radar signal indicator displays the video pulses generated by either the processor unit (under test) or the display protect circuit.

Display Functional Circuits (Sheet 3 of 3)

POWER DISTRIBUTION FUNCTIONAL CIRCUITS

The power distribution functional circuits convert facility power inputs (115 Vat) to the operating voltages required by the components of the PTS, and control the distribution of the operating voltages to the various components of the PTS. The circuits also test both the PTS operating voltages and the processor unit operating voltages to ensure that the voltages are within acceptable tolerances.

DISTRIBUTION NETWORK

The distribution network performs two distinct functions. First, it routes input power(115 Vat) from the power connector to power supply PSI and cooling fan B1. Second, it routes the outputs of power supply PS1 to the various circuit boards, switches and indicators of the PTS.

POWER SUPPLY PSI

Power supply PSI receives 115 Vac input power, via the distribution network, from the facility power source. The power supply converts the input power to various output voltages required to power (drive) the components of the PTS. The power supply provides nine outputs for distribution to the components of the PTS, and seven outputs which are applied to the analog signal interface circuit for testing the functional operation of the power supply.

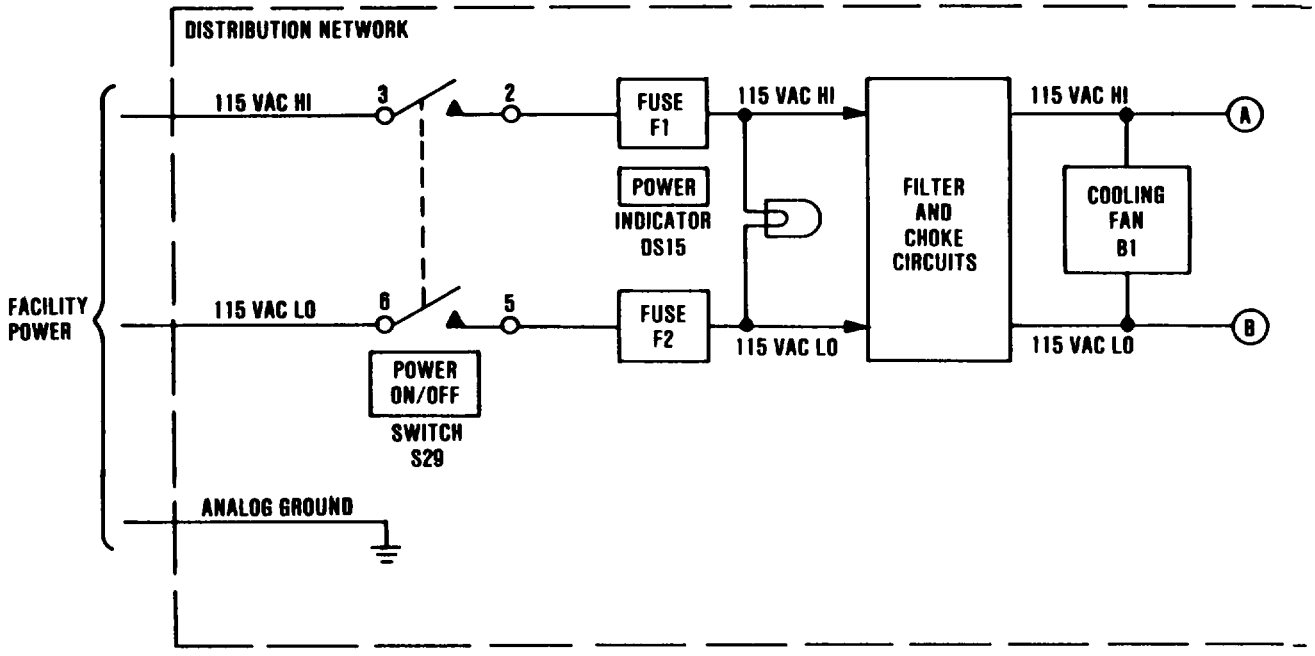
ANALOG SIGNAL INTERFACE CIRCUIT

The analog signal interface circuit tests the magnitudes of the PTS voltages and current source, and processor voltages and current source. This is accomplished to ensure that the necessary voltages and current sources are within acceptable parameters.

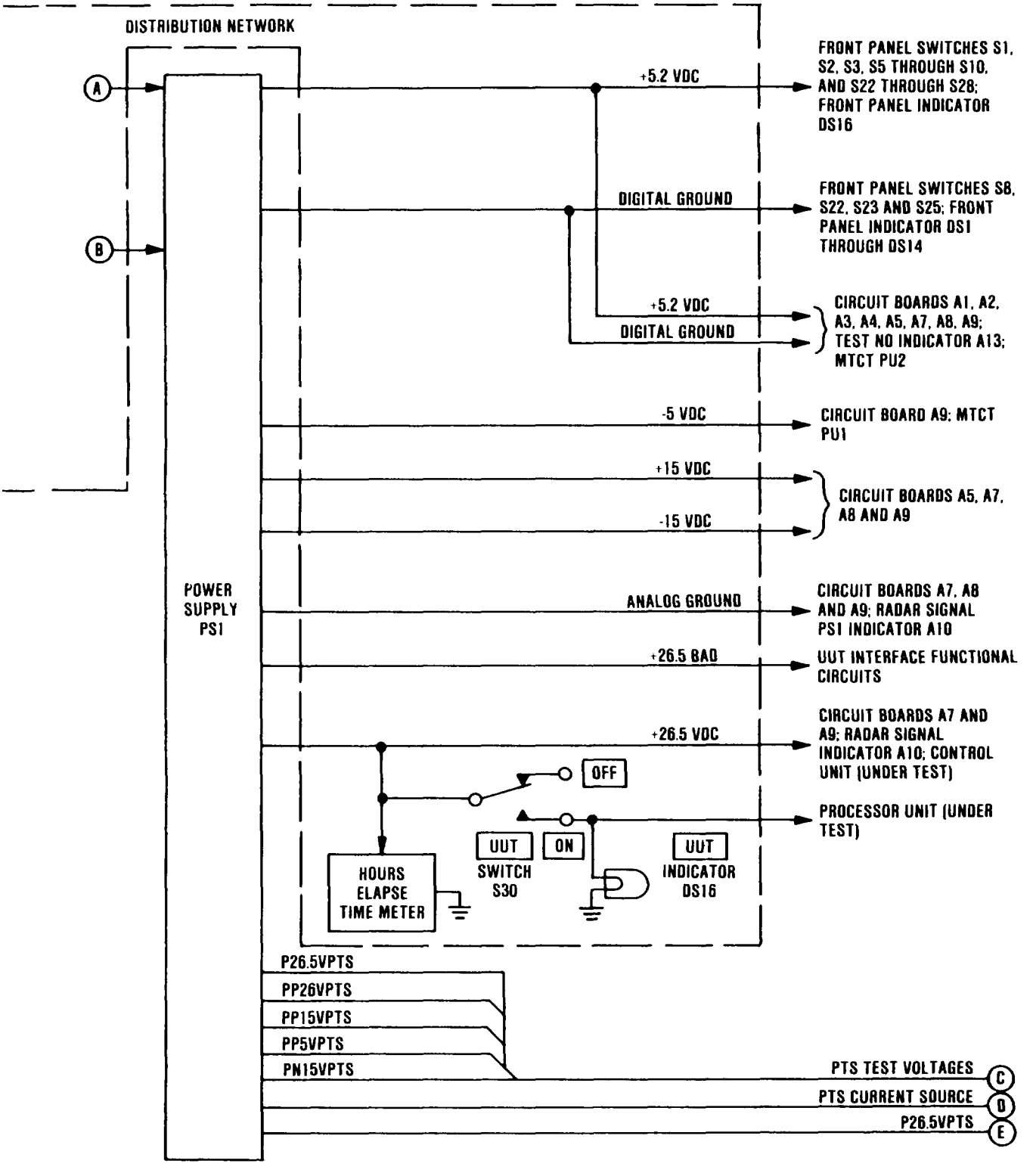
SELECTOR

The selector develops the enables needed to sequence the selection of the various PTS and processor unit voltages through the input MUX circuits to the window comparators. The enables are developed from the POWER CHECK CODES.

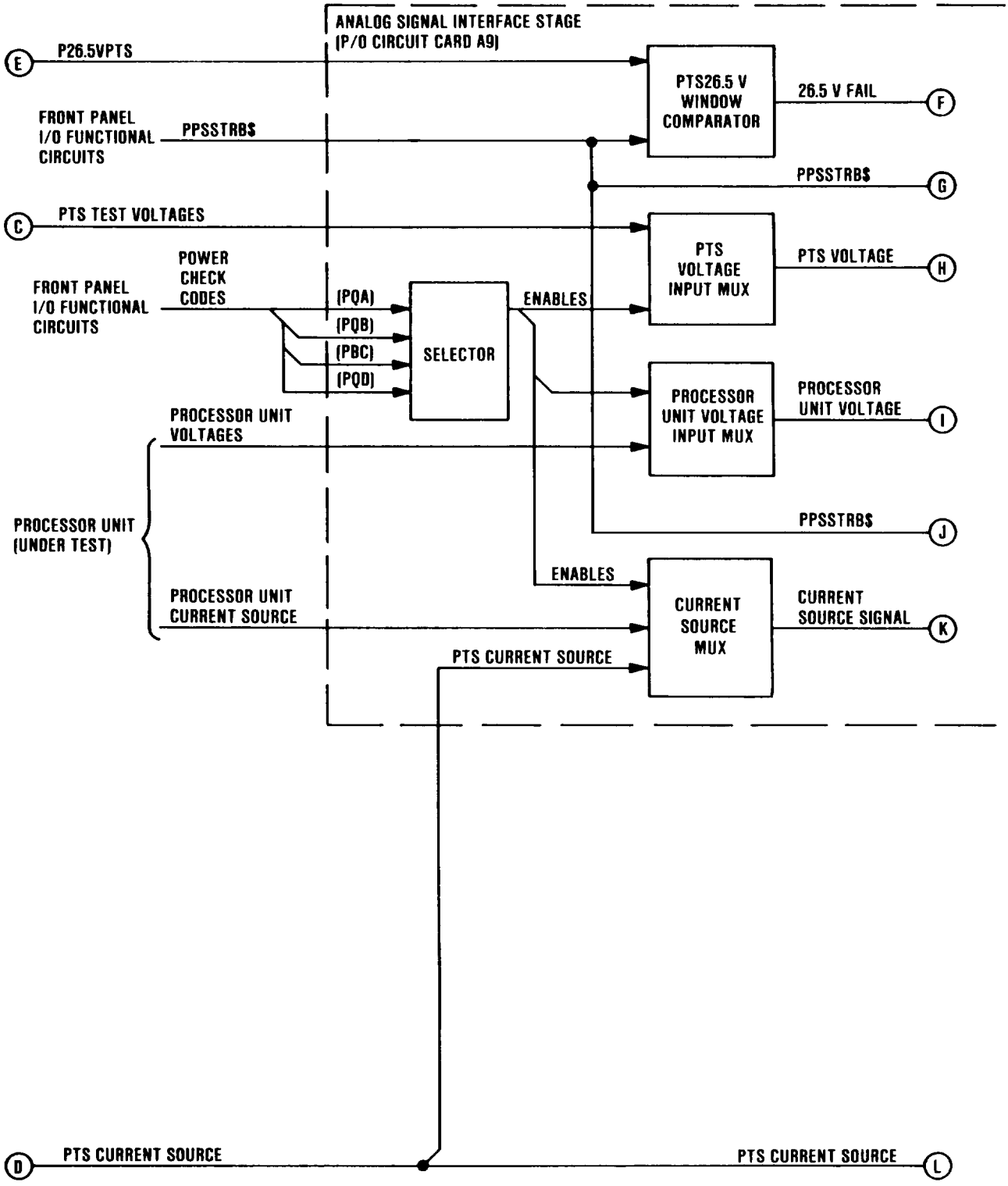
Power Distribution Functional Circuits (Sheet 1 of 7)



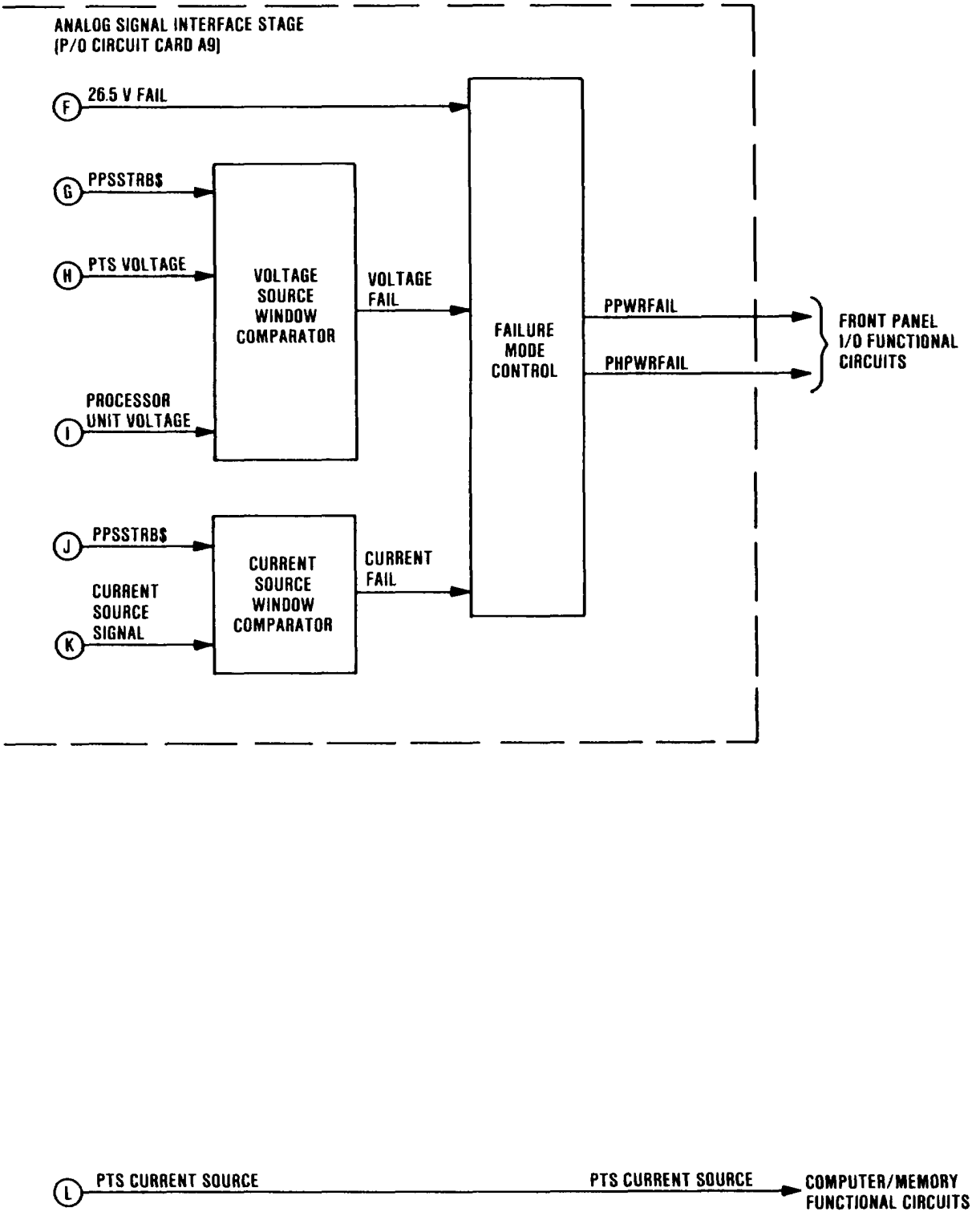
Power Distribution Functional Circuits (Sheet 2 of 7)



Power Distribution Functional Circuits (Sheet 3 of 7)



Power Distribution Functional Circuits (Sheet 4 of 7)



Power Distribution Functional Circuits (Sheet 5 of 7)

PTS VOLTAGE INPUT MUX

The PTS voltage input MUX permits the various PTSvoltages to be applied to the same voltage source window comparator. Selection of the desired input is a function of the ENABLES inputs.

PROCESSOR UNIT VOLTAGE INPUT MUX

The processor unit voltage input MUX performs the same function as the PTSvoltage input MUX, in the same manner as previously described.

CURRENT SOURCE MUX

The current source MUX performs the same function as the PTS voltage input MUX, in the same manner as previously described.

VOLTAGE SOURCE WINDOW COMPARATOR

When enabled by PPSSTRB$, the voltage source window comparator checks the applied voltage (PTS VOLTAGE or PROCESSOR UNIT VOLTAGE), against two known references (one reference set at the highest acceptable limit, and one reference set at the lowest acceptable limit)to ensure that the voltage being tested is within acceptable limits. Provided the input voltage falls within the acceptable limits, the VOLTAGE FAIL output of the voltage source window comparator stays low. If the voltage is outside of acceptable tolerances, the VOLTAGE FAIL output goes high.

CURRENT SOURCE WINDOW COMPARATOR

The current source window comparator performs a similar function in checking the CURRENT SOURCE SIGNAL. If the input is within tolerances, the CURRENT FAIL output of the current source window comparator remains low.

PTS 26.5V WINDOW COMPARATOR

The PTS 26.5V window comparator performs a similar function as previously described for the voltage source window comparator. Provided the input is within tolerance, the PTS 26.5V window comparator output (26.5V FAIL) remains low.

Power Distribution Functional Circuits (Sheet 6 of 7)

FAILURE MODE CONTROL

The outputs of the three window comparators are applied to the failure mode control. Provided all these outputs (VOLTAGE FAIL, CURRENT FAIL and 26.5V FAIL) remain low, the failure mode control outputs (PPWRFAIL and PHPWRFAIL) remain low, signifying that no failure has occurred. If any of the fail outputs go high, the change in state is detected by the failure mode control. The failure mode control outputs (PPWRFAIL and PHPWRFAIL) are set high, signifying that a failure has occurred.

Power Distribution Functional Circuits (Sheet 7 of 7)

SECTION CONTENTS

SECTION III
DETAILED FUNCTIONAL DISCUSSION

PAGE

INTRODUCTION

2-3. This section describes the major circuits that comprise the basic functional circuits of the PTS. Each discussion is supported by detailed functional diagrams.

COMPUTER/DMA CIRCUIT

The computer/DMA circuit performs five distinct functions. First, it controls retrieval operations of software instructions contained in the operational memory. Second, the circuit controls the transfer of data to and from the other functional circuits of the PTS. Third, the circuit controls the development of various test signals, test pulses, timing signals and commands used to test the functional operation of either the processor unit (under test) or control unit (under test). Fourth, the circuit processes the response signals and flags from the processor unit (under test) to determine the functional status of the unit. Fifth, the circuit performs a self-test of the PTS to determine the functional status of the PTS.

INTERRUPT STAGE

The interrupt stage informs the computer of the highest pending interrupt. This highest pending interrupt is denoted by signal INTREQ$ and interrupt code bits ICI thru IC3 where bit ICI is the highest significant bit of this three-bit code. Once the computer has serviced the interrupt, PCADD LINES PCADD1O thru PCADD14 are applied to the interrupt stage to reset the INTREQ$ signal.

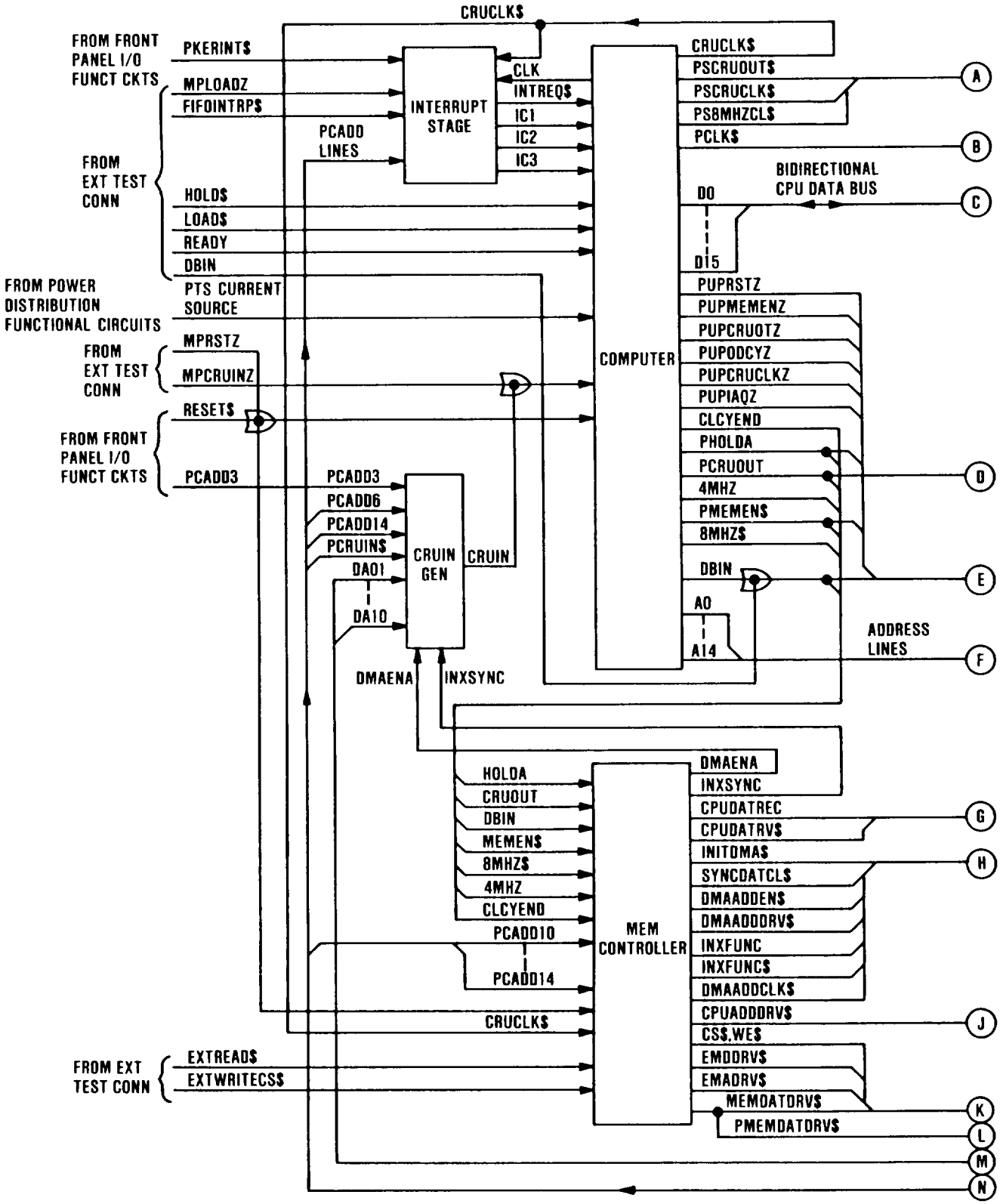
CRUIN GENERATOR

The CRUIN generator enables the computer to receive reset status information, front panel information and flags from the other functional circuits of the PTS. Depending upon the value of PCADD3 and PCADD6 thru PCADD14, any of this type information can be sent to the computer by the CRUIN generator over the serial CRUIN line.

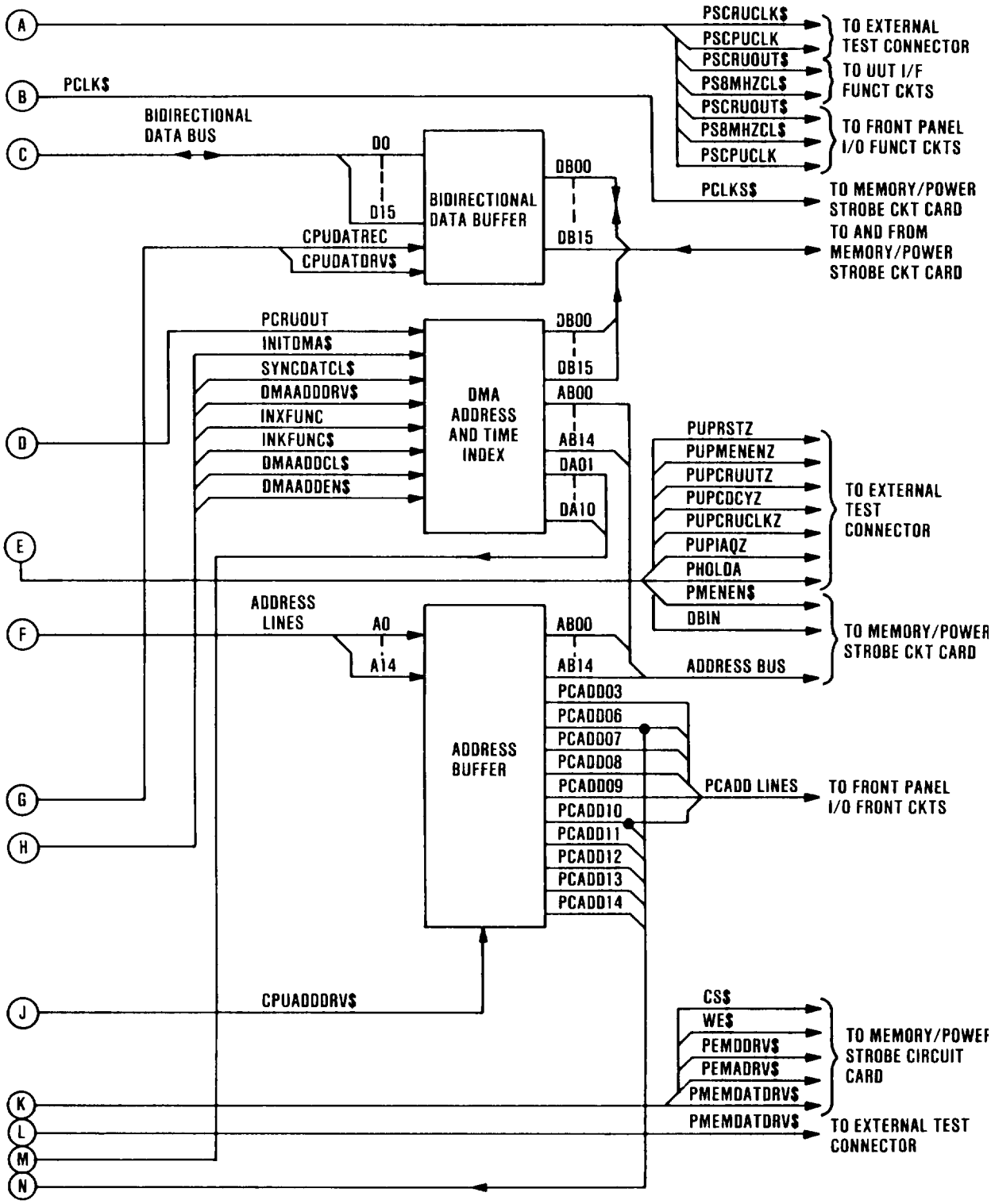
COMPUTER

Under control of the stored operational program, the computer controls the development and processing of test signals used to test the processor unit (under test) and control unit (under test). The computer is comprised of an SPB 9989 16-bit microprocessor, **a** clock generator and control gates. The microprocessor, continually performs three basic operations. First a data word (16 bits) is read from memory, then the word is decoded and/or executed, and finally the address of the next data word is incremented in order to continually repeat these three basic operations as long as power is applied to the PTS. For a more detailed operational discussion of the microprocessor, refer to the manufacturer’s data book.

Computer/DMA Circuit (Sheet 1 of 4)



Computer/DMA Circuit (Sheet 2 of 4)



Computer/DMA Circuit (Sheet 3 of 4)

MEMORY CONTROLLER

The memory controller regulates all data read/write transfers between the computer and RAM's and PROM's of the memory/power strobe circuit. All data read transfers from the memory are performed when the memory controller generates signals CS$ and MEMDATDRV$, whereas all data write transfers to the memory (RAM only) are performed when the memory controller issues signals CS$ and WE$. Furthermore, data read transfers from the memory to the computer are performed when signals CPUDATREC and CPUADDDRV$ are generated, whereas data write transfers from the computer to the memory (RAM only) are performed when signals CPUDATDRV$ and CPUADDDRV$ are generated. Read/write access to the memory for external equipment access is performed when the memory controller receives an EXTREAD$ signal or an EXTWRITECS$ signal.

BIDIRECTIONAL DATA BUFFER

The bidirectional data buffer enables the computer to either store data into the scratch-pad memory or to receive data stored in the PROM's (operational program) or in the scratch-pad memory (RAM). When signal CPUDATDRV$ is present, BIDIRECTION CPU DATA BUS bits DO thru D15 from the computer are routed through the bidirectional data buffer onto the BIDIRECTION DATA BUS as bits DBOO thru DB15. This action permits the computer to store data into scratch-pad memory of the memory/ power strobe circuit. However, when signal CPU DATREC is present, BIDIRECTION DATA BUS bits DBOO thru DB15 from either the PROM's or the RAM's are routed through the bidirectional data buffer onto the BIDIRECTION CPU DATA BUS as bits DO thru D15. In this manner, the computer receives either data pertaining to the operational program (located in PROM) or data temporarily stored by the computer or a DMA operation (located in RAM).

DMA ADDRESS AND TIME INDEX

The DMA address and time index is provided for future expansion of the PTS capabilities.

ADDRESS BUFFER

The address buffer enables the computer to access the operational program or scratch-pad memory via the ADDRESS BUS and regulate all other operations of the PTS via the control address (PCADD) lines. When signal CPUADDDRV$ is present, ADDRESS LINES AO thru Al 4 are routed through the address buffer circuit onto the ADDRESS BUS as ABOO thru AB14. This action permits the computer to access either the operational program or scratch-pad memory. In addition, PCADD LINES PCADD03 and PCADD06 thru PCADD14 are sent to the various functional circuits of the PTS to regulate all other operations.

Computer/DMA Circuit (Sheet 4 of 4)

MEMORY/POWER STROBE CIRCUIT

The memory/power strobe circuit performs three distinct functions. First, the circuit provides permanent storage for the operational program, allowing the operational program to be held in residence within the PTS. Second, the circuit provides temporary storage capabilities, which permit various test programs and test responses to be retained during test operations. Third, the circuit provides the capabilities for controlling data, addresses and commands transfer between the PTS and external equipment.

BIDIRECTIONAL DATA BUFFER

Under control of the computer/DMA circuit, the bidirectional data buffer either routes data on the BIDIRECTION DATA BUS to the BIDIRECTION MEM DATA BUS or routes data on the BIDIRECTION MEM DATA BUS to the BIDIRECTION DATA BUS. For example, when signal MEMDATDRV$ is present, data bits DBOO thru DB15 from the computer/DMA circuit are routed through this circuit and are applied to the 8K X 16 RAM as data bits MDBOO thru MDB15. However, when the MEMDATDRV$ signal from the computer/DMA circuit is not present, data bits MDBOO thru MDB15 from either the 8K X 16 RAM or the 24K X 16 PROM are routed through this circuit and are applied to the computer/DMA circuit as data bits DBOO thru DBI 5. It should be noted that data can never be routed to the 24K X 16 PROM when the MEMDATDRV$ signal is present.

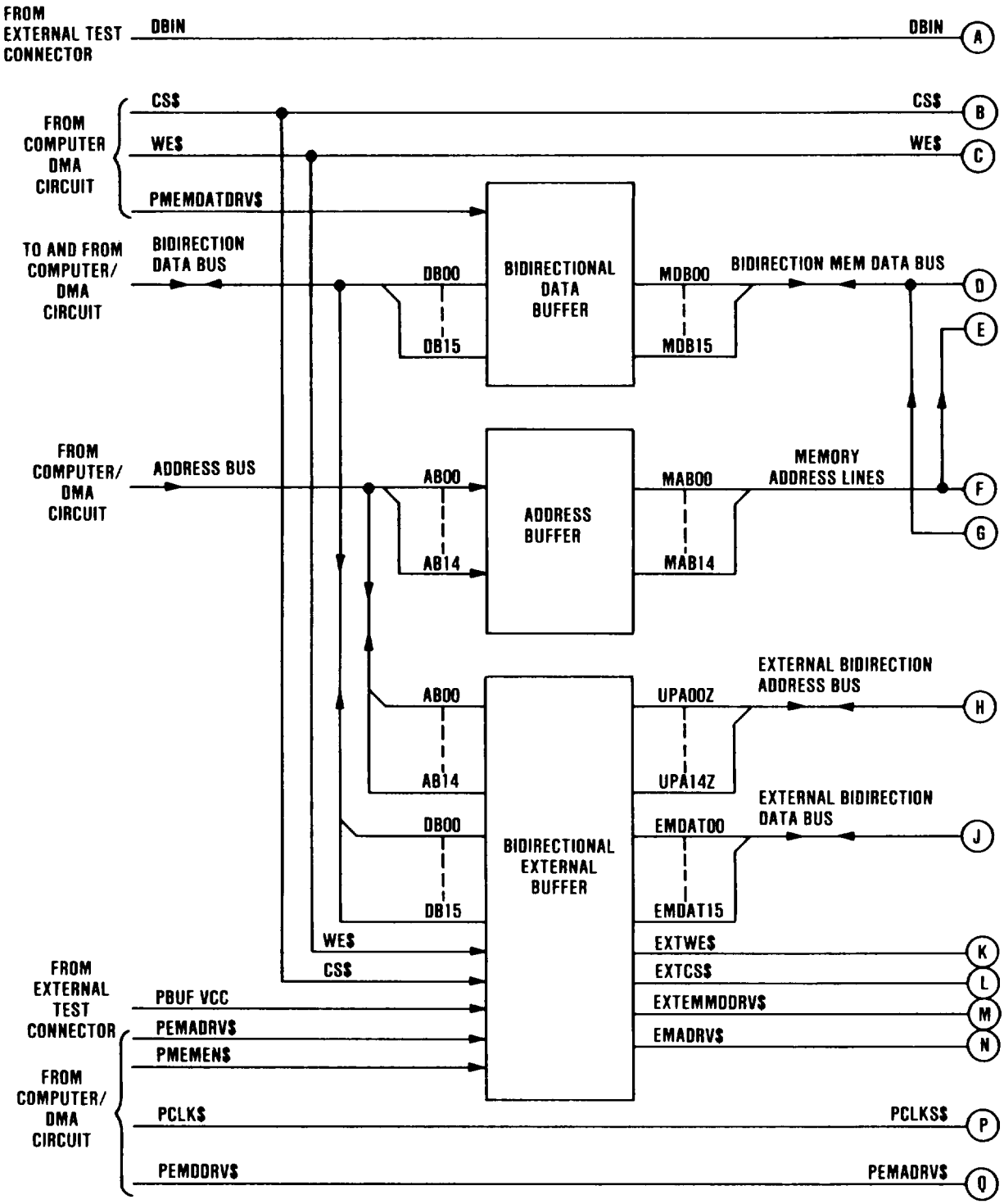
ADDRESS BUFFER

The address buffer routes address data on the ADDRESS BUS to the MEMORY ADDRESS LINES. This address data, in the form of address bits AB00 thru AB14, can be received from either the computer/DMA circuit or the external equipment, via the bidirectional external buffer. Once received, the address data is routed through this address buffer and is applied to the 8K X 16 RAM and 24K X 16 PROM as address bits MABOO thru MAB14.

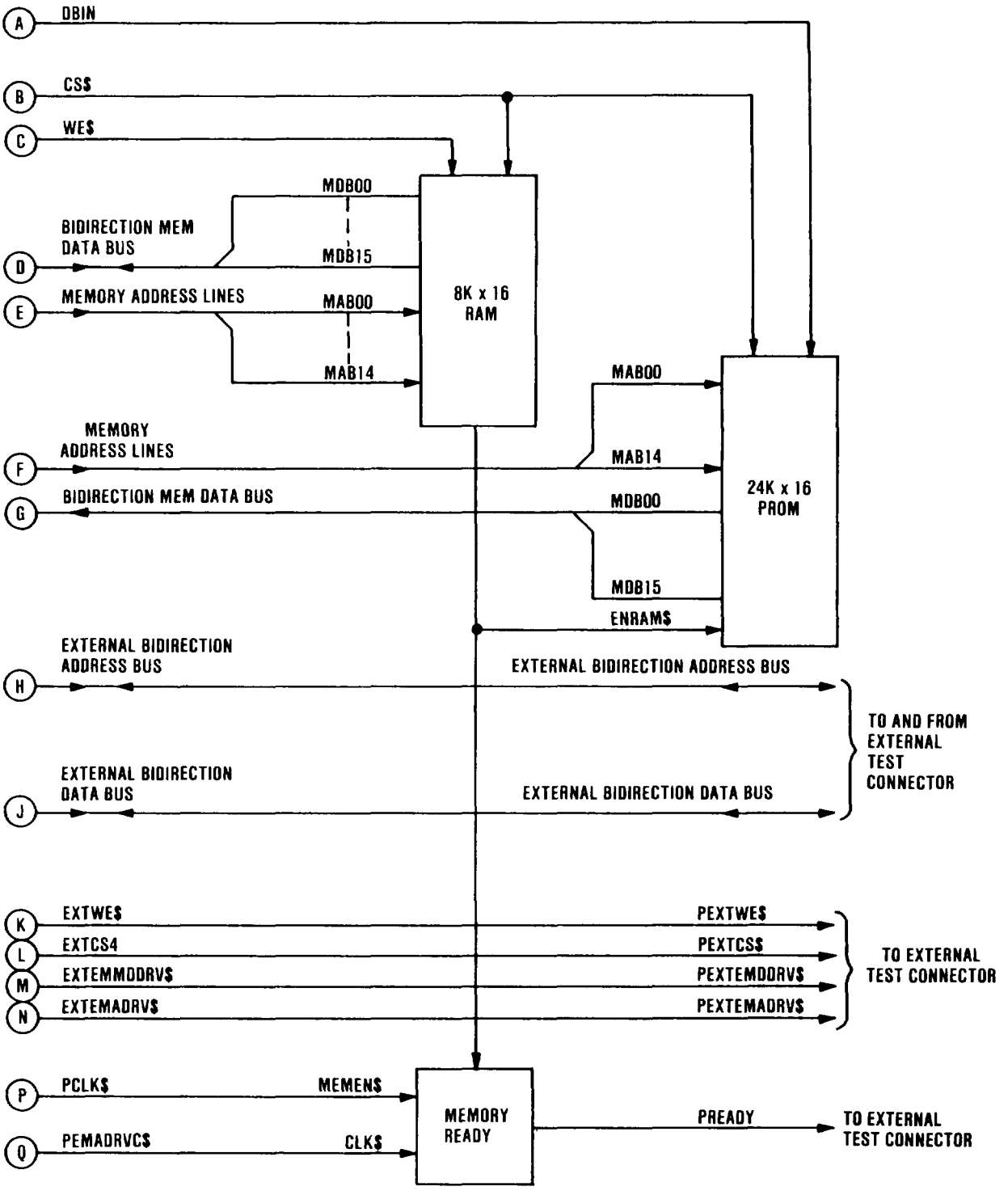
BIDIRECTIONAL EXTERNAL BUFFER

Under control of the computer/DMA circuit and the external equipment, the bidirectional external buffer routes both data between the EXTERNAL BIDIRECTIONAL DATA BUS and the EXTERNAL BIDIRECTION DATA BUS and, address data, between the ADDRESS BUS and the external equipment BIDIRECTION ADDRESS BUS. For example, when signals PBUF VCC and PEMDDRV$ are both present, data bits DBOO thru DB15 from either the external equipment or the 8K X 16 RAM and 24K X 16 PROM via the bidirectional data buffer are sent to the external equipment over the EXTERNAL BIDIRECTION DATA BUS as data bits EM DATOO thru EMDAT15. Conversely, when signal PBUF VCC is present and signal PEMDDRV$ is not present, data bits EMDATOO thru

Memory/ Power Strobe Circuit (Sheet 1 of 5)



Memory/Power Strobe Circuit (Sheet 2 0f 5)



Memory/Power Strobe Circuit (Sheet 3 0f 5)

EMDAT15 from the external equipment are routed through this circuit and are applied to the 8K X 16 RAM circuit via the bidirectional data buffer as data bits DBOO thru DB15. In the case of bidirectional address data flow, this circuit operates in a similar manner. For example, when signals PBUF VCC and PEMADRV$ are both present, address bits ABOO thru AB14 from the computer/DMA circuit are sent to the external equipment over the EXTERNAL BIDIRECTION ADDRESS BUS as address bits UPAOOZ thru UPA142. Conversely, when signal BUF VCC is present and signal EMADRV$ is not present, address bits UPAOOZ through UPA14Z from the external equipment are routed through this circuit and are applied to the 8K X 16 RAM and 24 X 16 PROM via the address buffer as address bits ABOO thru AB14.

8K X16 RAM

The 8K X 16 RAM provides scratch-pad type memory capability for either the computer/DMA circuit, or the external equipment. The memory portion of this circuit has the capacity to store approximately eight thousand (8K) 16-bit data words. Each 16-bit data word location can either be written into or read from according to address bits MABOO thru MAB14, which can specify address values between COOO and FFFE. Data bits MDBOO thru MDB15 on the BIDIRECTION MEM DATA BUS are written into a specific location of the 8K X 16 RAM whenever signals WE$ and CS$ are both received from the computer/DMA circuit.. Conversely, data from a specified location can be read from the 8K X 16 RAM and placed onto the BIDIRECTION MEM DATA BUS only when signal CS$ is received from the computer/DMA circuit. It should be noted that whenever the two most significant address bits (MABOO and MABO1) are both logic 1‘s, signal ENRAM$ is generated to inhibit the 24K X 16 PROM. Thus data can only be written into or read from the 8K X 16 RAM when these two bits are logic 1‘s.

24K X 16 PROM

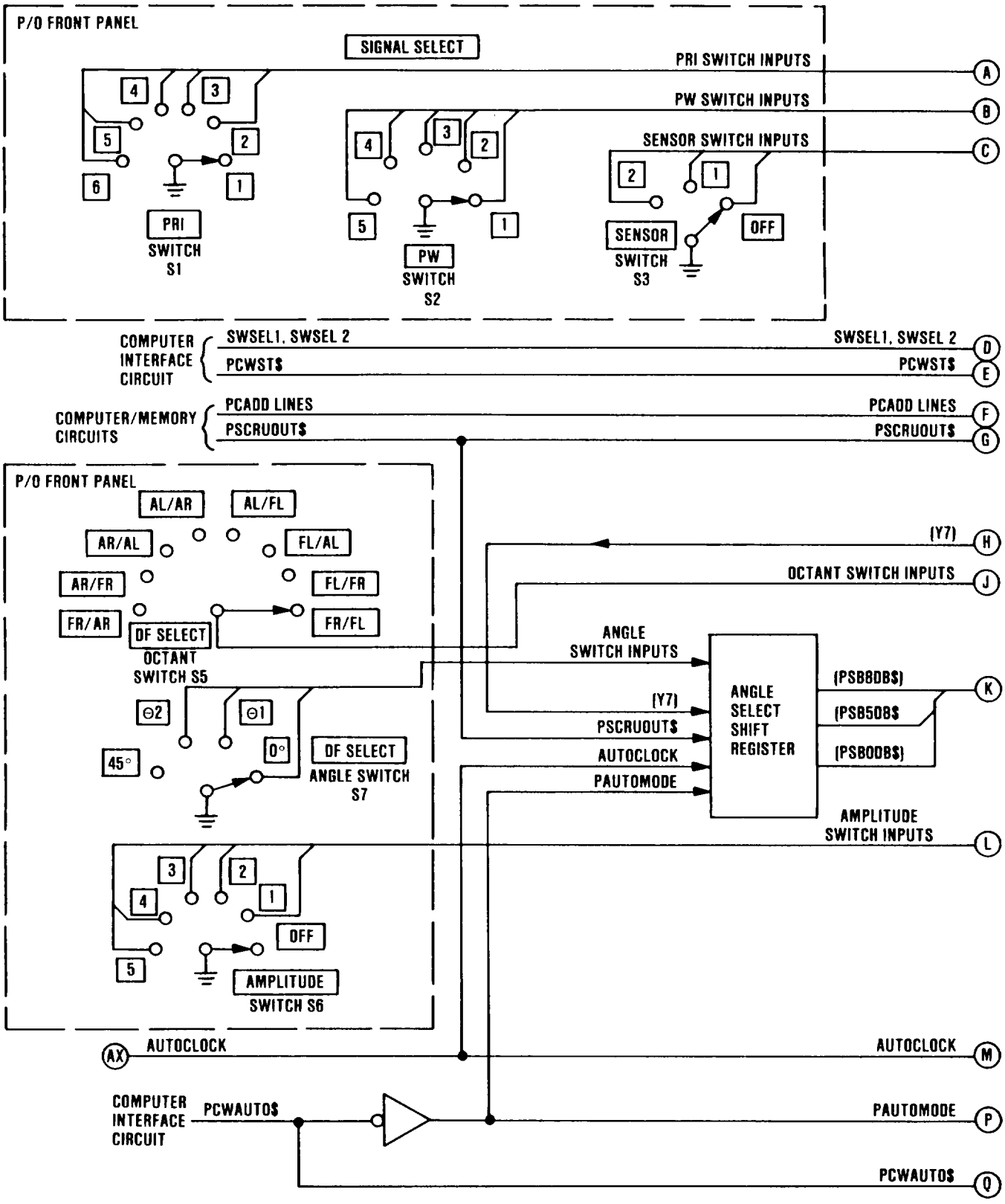
The 24K X 16 PROM contains the complete PTS software program. The memory portion of this circuit has a capacity of approximately twenty-four thousand (24K) 16-bit data words, which describe program instructions or data tables. These program instructions and data tables are read from this circuit according to address bits MABOO thru MAB14, which can only specify address values between 0000 and BFFE.. For instance, whenever the two most significant address bits (MABOO and MABO1) are not both logic 1‘s, signal ENRAM$ is not applied to the 24K X 16 PROM circuit. Non receipt of this signal enables data contained below address COOO to be read from the 24K X 16 PROM, once signals CS$ and DBIN are received from the computer/DMA circuit.

Memory/Power Strobe Circuit (Sheet 4 of 5)

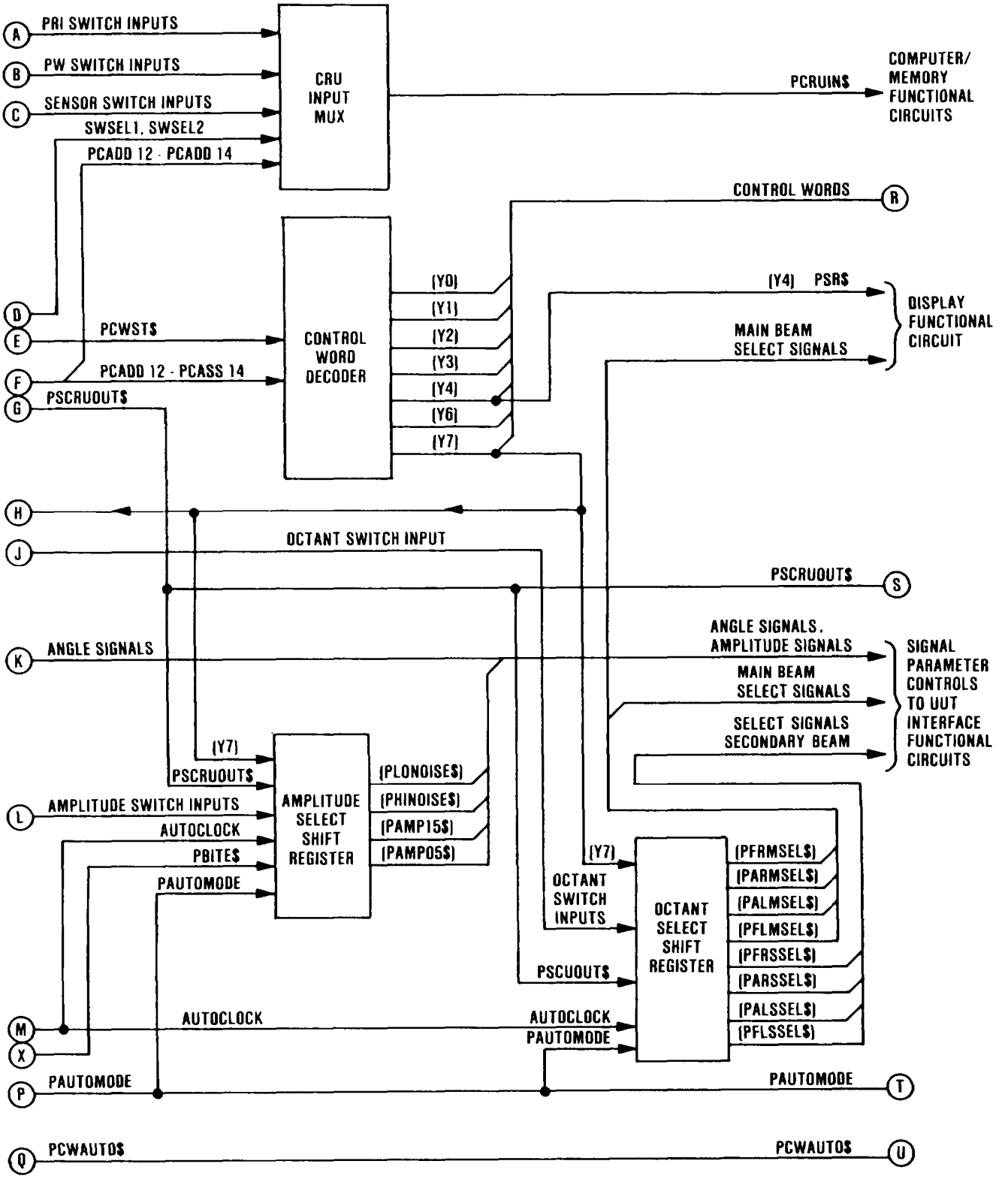
MEMORY READY

Under control of the computer/DMA circuit, memory ready informs the external equipment of memory (RAM or PROM) availability. Generation of signal PREADY is used to define this memory availability when signal PMEMEN$ is received. If the 8K X 16 RAM circuit is to be accessed, signal ENRAM$ is applied to memory ready to permit generation of this PREADY signal after a predetermined time delay for the RAM. However, if the 24K X 16 PROM circuit is to be accessed, signal ENRAM$ is not applied to memory ready and signal PREADY is generated after a predetermined time delay for the PROM.

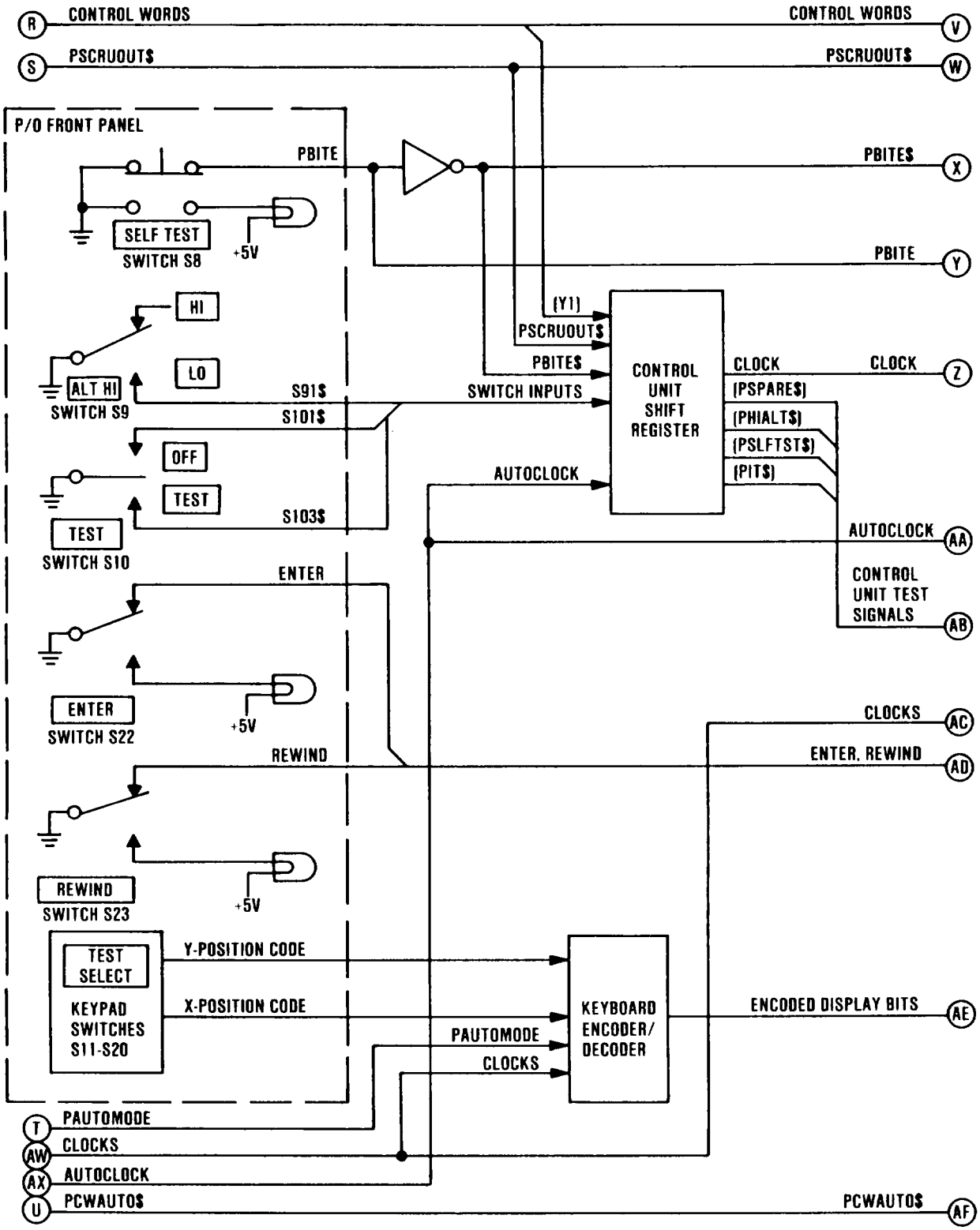
Memory/Power Strobe Circuit (Sheet 5 of 5)



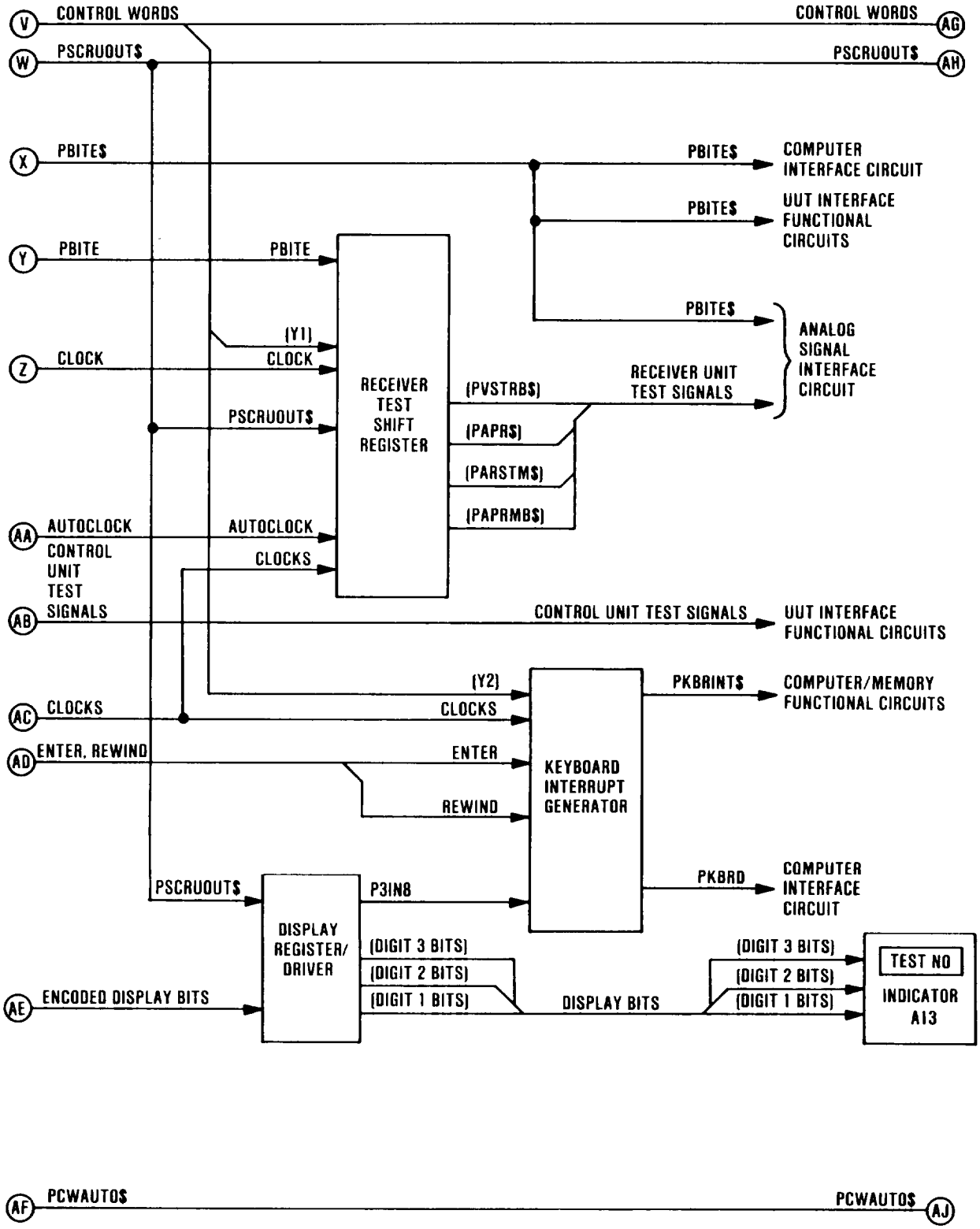
Analog Control interface Circuit Sheet l of 12)



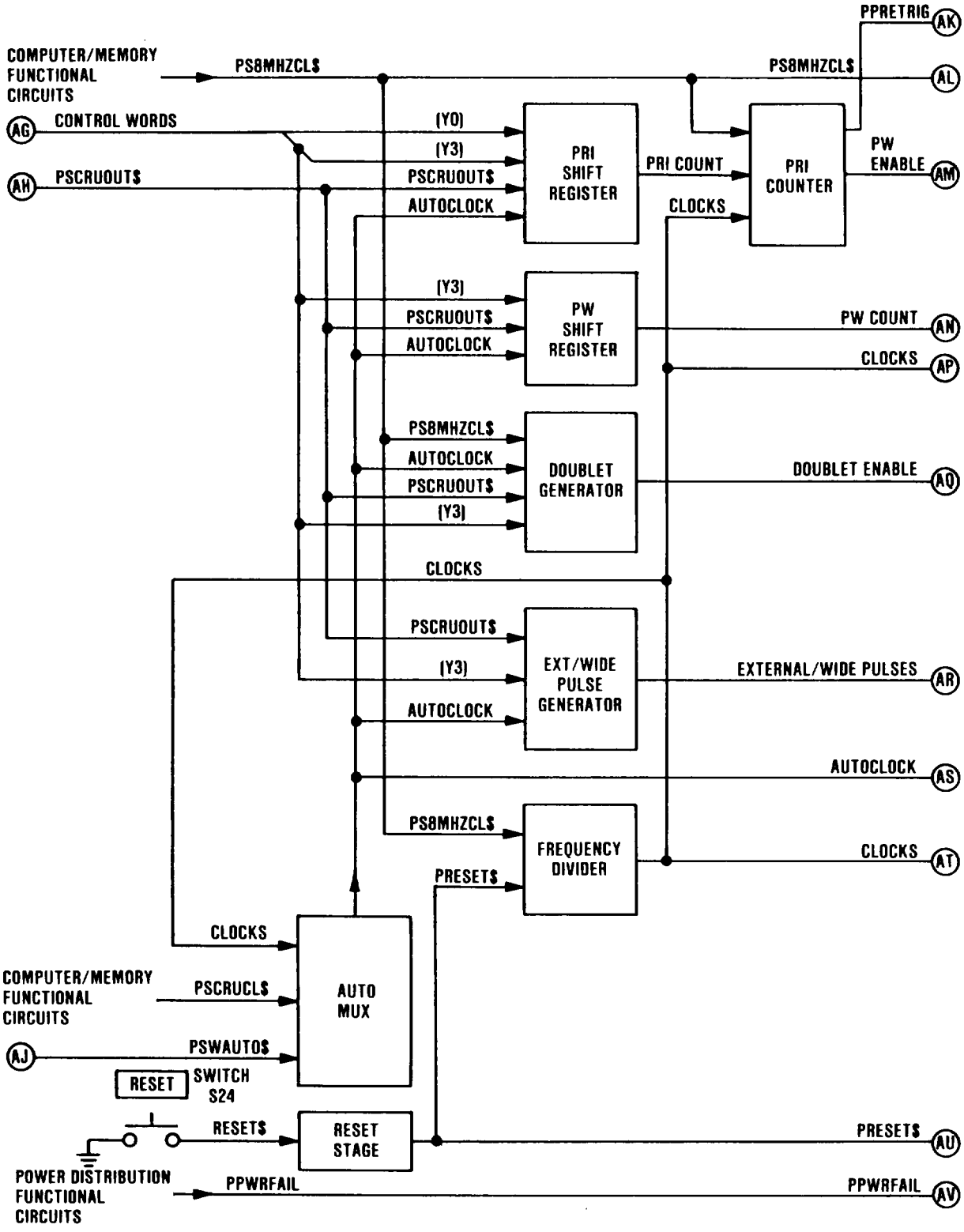
Analog Control Interface Circuit (Sheet 2 of 12)



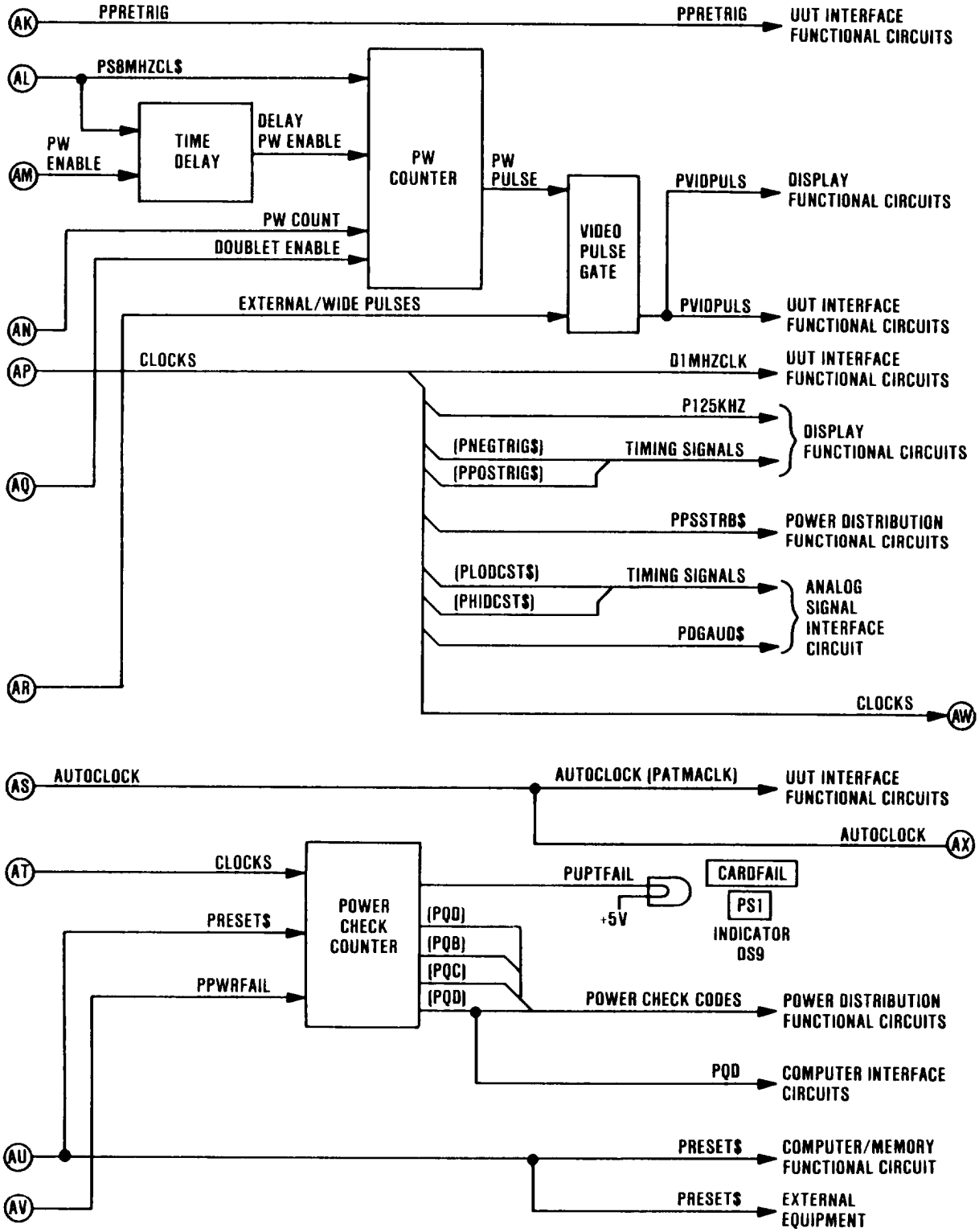
Analog Control Interface Circuit (Sheet 3 of 12)



Analog Control Interface Circuit (Sheet 4 of 12)



Analog Control interface Circuit (Sheet 5 0f 12)



Analog Control Interface Circuit (Sheet 6 of 12)

ANALOG CONTROL INTERFACE CIRCUIT

The analog control interface circuit performs five distinct functions. First, the circuit develops, in response to either the manual setting of front panel switches, or the software program, the basic pulses used to develop test signals in the display and UUT interface functional circuits. Second, the circuit develops the POWER CHECK CODES needed to test the PTS and processor unit power supplies. Third, the circuit provides the means for inputting test instructions via the TEST SELECT keypad switches, allowing the operator to select and sequence testing procedures. Fourth, the circuit develops commands, in response to the software program, for testing the control unit (under test), and the receiver circuits in the processor unit (under test). Fifth, the circuit develops commands, in response to either the manual setting of front panel switches, or the software program, to control the functional operations of the other functional circuits of the PTS.

CRU INPUT MUX

The CRU input MUX routes data from the PRI, PW and SENSOR front panel switches, to the computer/memory functional circuits to permit manual control of the development of the test pulses applied to the processor unit (under test). When the MUX is enabled by SWSEL1 and SWSEL2 strobes, the PCADD12 thru PCADD14 inputs select which data (switch) will be inputted via the MUX.

CONTROL WORD DECODER

The control word decoder develops CONTROL WORDS, used to clear the various registers and signal generators within the front panel iI/O functional circuits. This allows the hardware components to latch new data. The program instructions contained in PCADD12 thru PCADD14 are decoded by the control word decoder when PCWST$ goes low.

OCTANT SELECT SHIFT REGISTER

The octant select shift register develops MAINBEAM SELECT SIGNALS and SECONDARY BEAM SELECT SIGNALS which are used to represent the octant locations of the simulated target. The shift register is cleared by CONTROL WORDS (Y7). Octant data is then loaded into the octant select shift register by AUTOCLOCK. In the manual mode of operation, PAUTOMODE is low. Octant data is developed by the front panel DF SELECT octant switch, and parallel-shifted into the register. In the auto mode PAUTOMODE is high. Octant data contained on the PSCRUOUT$ line is serially-shifted into the register.

Analog Control Interface Circuit (Sheet 7 of 12)

ANGLE SELECT SHIFT REGISTER AND AMPLITUDE SELECT SHIFT REGISTER

The angle select shift register and amplitude select shift register function in the same manner as the octant select shift register to develop the signals that determine the range position of the simulated target. These registers develop ANGLE SIGNALS and AMPLITUDE SIGNALS, respectively. The angle input data and amplitude input data is developed by the DF SELECT angle switch and AMPLITUDE switch, respectively.

CONTROL UNIT SHIFT REGISTER

The control unit shift register develops CONTROL UNIT TEST SIGNALS required to exercise the processor unit switch decoder circuits in the processor unit (under test). In the test (normal) mode of operation, the control unit simulated shift register is cleared by the CONTROL WORDS (Y1). The setting of the front panel ALT (altitude) and TEST switches are parallel-shifted into the register by AUTOCLOCK. In the self-test mode of operation (PB1TE$ set low), the register is cleared as previously described; however, the signal data is contained on the PSCUOUT$ line. The data is serially-clocked into the register by the AUTOCLOCK.

RECEIVER TEST SHIFT REGISTER

The receiver test shift register develops RECEIVER UNIT TEST SIGNALS required to simulate STAFT and STFWD messages from the radar receivers to the processor unit and test STAFT and STFWD messages from the processor unit to the radar receivers. In the test (normal) mode of operation, the receiver test shift register is cleared by CONTROL WORDS (Y1). The receiver test data contained on the PSCRUOUT$ line is clocked into the register by the CLOCK output of the control unit shift register. Data is clocked out of the register by CLOCKS from the frequency divider. In the self-test mode, timing is controlled by AUTOCLOCK.

KEYBOARD ENCODER/DECODER

In the manual mode of operation, the operator enters the display bits manually by depressing the TEST SELECT keypad switches. These switches, when depressed, develop the Y-POSITION CODE and X-POSITION CODE outputs. The outputs are clocked into the keyboard encoder/decoder. The keyboard encoder/decoder converts the outputs into a hexadecimal code (ENCODED DISPLAY BITS).

Analog Control Interface Circuit (Sheet 8 of 12)

DISPLAY REGISTER/DRIVER

The display register/driver latches display bits (DIGIT 3 BITS, DIGIT 2 BITS and DIGIT 1 BITS) for application to the TEST NO indicator. The display bits are developed automatically when PSCRUOUT$ is serially loaded into the display register/driver. This occurs in the self-test mode and, when responses are generated by the computer/memory functional circuits, in the test (normal) mode. The display bits are also developed manually by the operator in the test (normal) mode when the TEST SELECT keypad switches are depressed.

TEST NO INDICATOR

The TEST NO indicator converts the DISPLAY BITS to a visual representation. The visual representation takes the form of an alphanumeric code for use by the operator in determining the functional status of the PTS, and the processor unit (under test).

KEYBOARD INTERRUPT GENERATOR

The keyboard interrupt generator develops two output flags. The first flag (PKBRINT$) notifies the computer/memory functional circuits that an interrupt function is required. The second flag (PKYBRD) designates whether the interrupt is required for a rewind or enter function. When PKYBRD is high, a rewind function is designated. When PKYBRD is low, an enter function is designated.

RESET STAGE

The reset circuit reads the status of the front panel RESET switch to determine if a reset function has been selected by the operator. When the RESET switch is depressed, the circuit develops a PRESET$ output pulse. This pulse, when applied to the computer/memory functional circuits, re-initializes the PTS.

FREQUENCY DIVIDER

The frequency divider develops the various clocks required for testing (normal) and self-test modes of operation. The frequency divider counts the system clock (PS8MHZCL$) pulses, producing from its various outputs, the clocks and strobes used within the PTS.

Analog Control Interface Circuit (Sheet 9 of 12)

POWER CHECK COUNTER

The power check counter develops the POWER CHECK CODES required to test the processor unit (under test) and PTS voltages and current sources. The counter is clocked by CLOCKS from the frequency divider unless a failure is detected in the processor unit or PTS power supply. If a failure is detected, PPWRFAIL goes high, inhibiting the power checks counter. This latches the failure indication and causes the CARD FAIL PSI indicator to light.

AUTO MUX

The auto MUX gates one of two input clocks (either PSCRUCL$ or the internally generated CLOCKS) for application as the AUTOCLOCK to the components of the analog control interface circuit. Selection is the function of PCWAUTO$. When PCWAUTO$ goes low (low in auto mode operation), PSCRUCL$ is applied through the auto MUX as AUTOCLOCK. When PCWAUTO$ is high (high in manual mode of operation), the internally generated CLOCKS is gated through the auto MUX as AUTOCLOCK.

PRI SHIFT REGISTER

The PRI shift register latches PRI data (which represents the time duration between PW pulses) after the register is cleared by CONTROL WORDS (Y0 and Y3) from the control word decoder. The PRI data contained on the PSCRUOUT$ line is serially-shifted into the PRI shift register by the AUTOCLOCK.

PRI COUNTER

The PRI counter develops the time duration between the generation of PW PULSES to allow the pulses to be applied to the processor unit (under test) at the proper frequency. The counter is loaded with PRI COUNT (PRI data) and counts down toward zero. When the proper count is reached, the counter outputs PPRETRIG and PW ENABLE.

TIME DELAY

The PW ENABLE is delayed for one count by the time delay. The delay is provided to meet internal pulse generation requirements.

Analog Control Interface Circuit (Sheet 10 of 12)

PW SHIFT REGISTER

The PW shift register latches PW data (which represents the time duration of the PW PULSE) after the register is cleared by CONTROL WORDS (Y3). The PW data contained on the PSCRUOUT$ line is serially-shifted into the PW shift register by the AUTOCLOCK.

PW COUNTER

The PW counter develops the time duration of the PW PULSE to ensure that the pulses applied to the processor unit (under test) are of the proper pulse width. The counter is loaded with PW COUNT (PW data). When enabled by DELAYED PW ENABLE, the counter develops the leading edge of PW PULSE, and counts down toward zero. When the counter reaches the proper count, the trailing edge of PW PULSE is developed. The PW counter can also be enabled by DOUBLET ENABLE when the software program calls for generation of doublet pulses.

DOUBLET GENERATOR

The doublet generator latches doublet data (representing the time duration between PW PULSES when the software program calls for the generation of doublet pulses) after the generator is cleared by CONTROL WORDS (Y3). The data contained on the PSCRUOUT$ line is serial-shifted into the generator by AUTOCLOCK. The doublet generator then counts down toward zero (clocked by PS8MHZCL$). When the proper count is reached, DOUBLET ENABLE is generated. When doublet generation has been selected by the software program, the PW counter is first loaded with the PW COUNT and enabled by DELAYED PW ENABLE. The PW counter produces the first PW PULSE, and is then loaded again with the PW COUNT. The PW counter is then enabled a second time by DOUBLET ENABLE.

EXT/WIDE PULSE GENERATOR

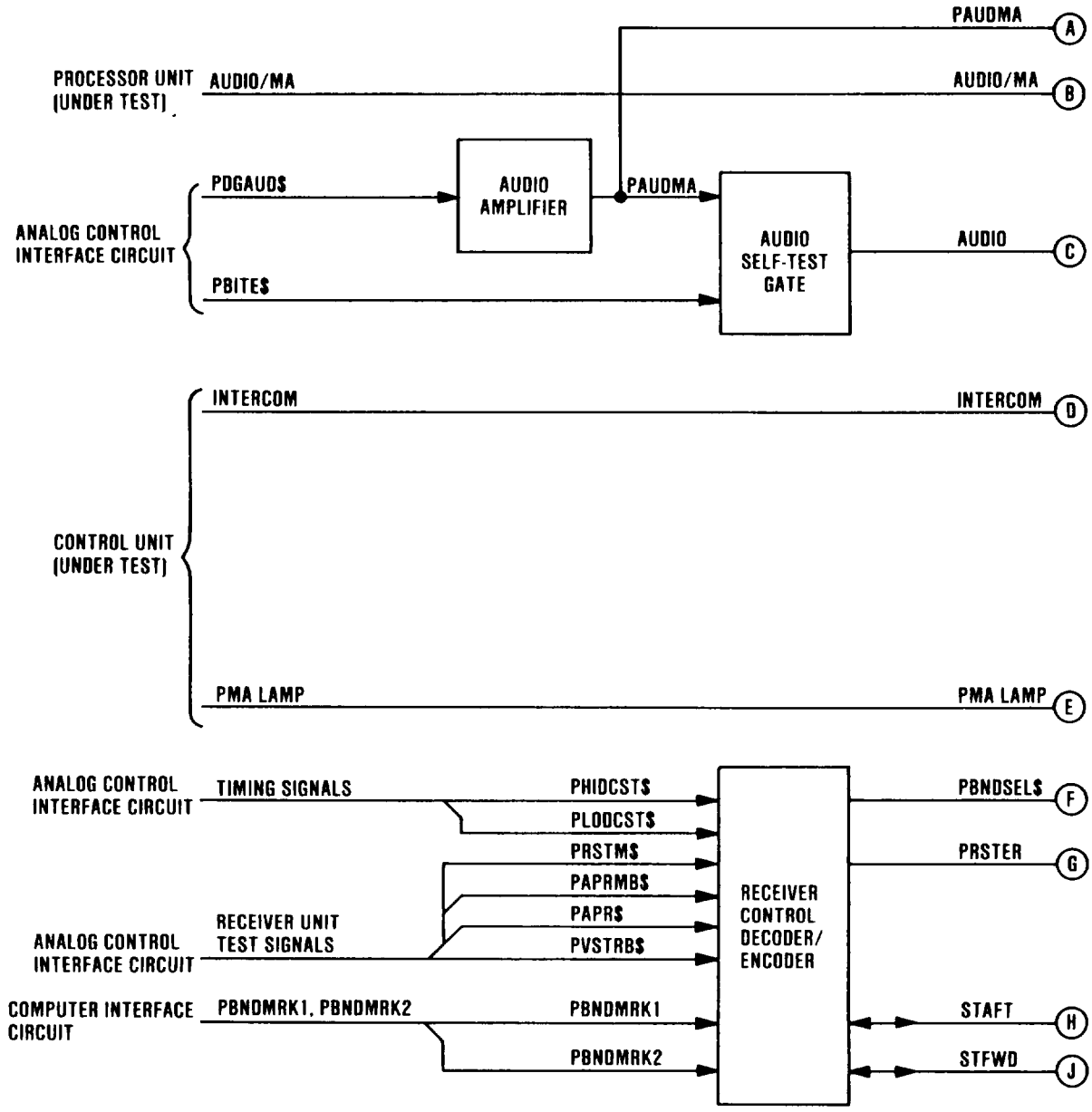
The ext/wide pulse generator develops the wide pulses and external pulse used to test the wide pulse capabilities of the processor unit (under test). The ext/wide pulse generator latches either the external data or wide pulse data contained on the PSCRUOUT$ line, after the generator is cleared by CONTROL WORDS (Y3). The wide pulse data represents selection of one of two wide pulse widths. The external data represents an externally developed pulse width. The data is serially-shifted into the ext/wide pulse generator by AUTOCLOCK, triggering the generation of either an external pulse or one of two wide pulses.

Analog Control Interface Circuit (Sheet 11 of 12)

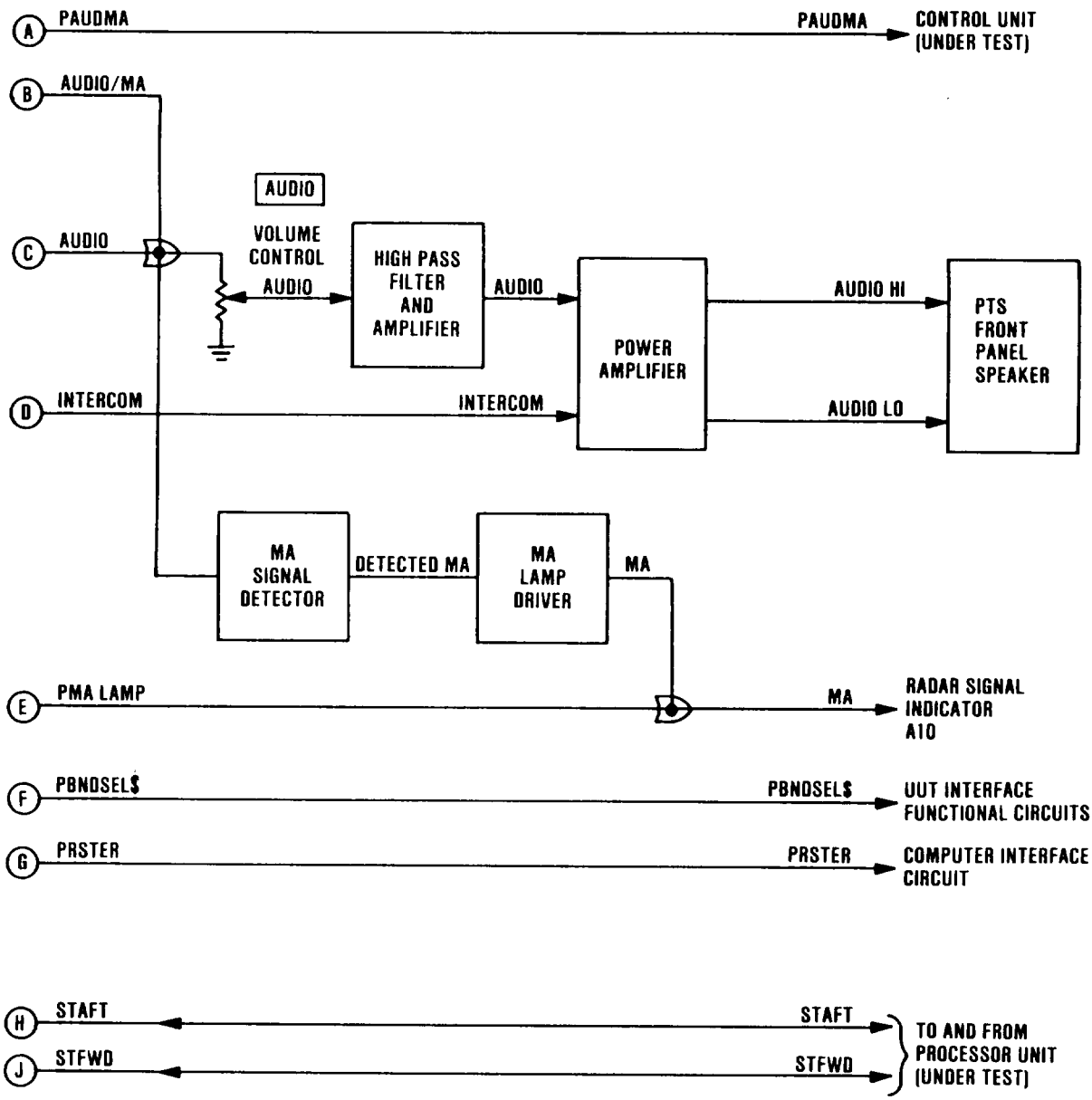
VIDEO PULSE GATE

The video pulse gate, when appropriately enabled, applies either the pw PULSE, the external pulse, or the selected wide pulse (as PVIDPULS), to the UUT interface and display functional circuits. These pulses are used as the main drive pulses to develop the simulated radar receiver pulse outputs.

Analog Control Interface Circuit (Sheet 12 of 12)



Analog Signal interface Circuit (Sheet 1 of 4)



Analog Signal Interface Circuit (Sheet 2 of 4)

ANALOG SIGNAL INTERFACE CIRCUIT

The analog signal interface circuit performs four distinct functions. First, the circuit tests the audio circuits of the control unit (under test) to determine the operational status of the circuit, by generating a test signal (PAUDMA) input to the control unit (under test), and processing the response signals (PMALAMP and INTERCOM) from the control unit. Second, the circuit tests the audio circuits of the processor unit (under test) to determine that the circuits are operational. Third, the circuit performs a self-test of the PTS audio circuits to ensure that the test circuits are functioning properly. Fourth, the circuit tests the STAFT and STFWD message lines of the processor unit (under test).

AUDIO AMPLIFIER

When a control unit is being tested, simulated audio (PDGAUD$) is amplified by the audio amplifier and applied as PAUDMA to the control unit (under test). The control unit processes the PAUDMA and returns INTERCOM and PMALAMP signals to the PTS. The PMALAMP signal turns on the radar signal indicator unit MA lamp. The INTERCOM signal drives the power amplifier.

POWER AMPLIFIER

The power amplifier provides the power handling capabilities required to drive the PTS front panel speaker. When the unit under test is a processor unit or the PTS is operating in the self-test mode, the power amplifier is driven by the AUDIO output of the high pass filter and amplifier. When the unit under test is a control unit, the power amplifier is driven by the INTERCOM output of the control unit.

PTS FRONT PANEL SPEAKER

The PTS front panel speaker converts the power amplifier signal outputs into aural indications. These aural indications are used by the operator to determine the functional status of the audio circuits of the unit under test.

HIGH PASS FILTER AND AMPLIFIER

When the unit under test is a processor unit, the high pass filter and amplifier samples the AUDIO/MA signal to determine if the signal contains an audio component. If an audio component is present at the proper frequency, an AUDIO signal is generated which is used to drive the power amplifier. In the self-test mode, the high pass filter and amplifier samples the AUDIO signal in the same manner as described above.

Analog Signal Interface Circuit (Sheet 3 of 4)

MA SIGNAL DETECTOR

The MA signal detector samples the AUDIO/MA signal when the unit under test is a processor unit to determine if the signal contains an MA component. If an MA component is present, a DETECTED MA signal is applied to the MA lamp driver. In the self-test mode, the MA signal detector samples the AUDIO signal in the same manner described above.

MA LAMP DRIVER

The MA lamp driver provides the current handling capabilities required to drive the radar signal indicator unit MA lamp. The MA lamp in the radar signal indicator unit is turned on by either the PMALAMP signal (when the unit under test is a control unit) or the MA signal (when the unit under test is a processor unit or the PTS is in the self-test mode).

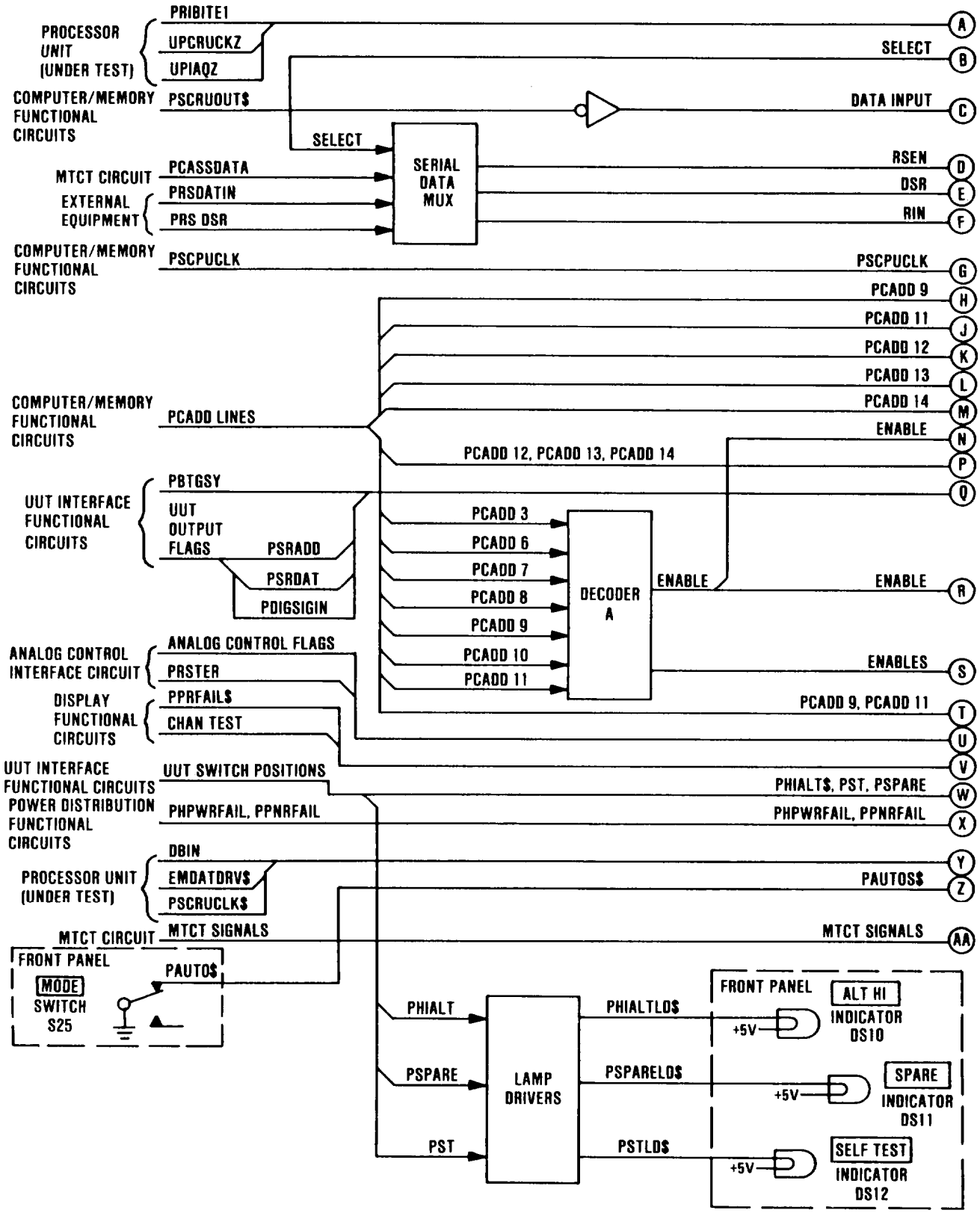
AUDIO SELF-TEST GATE

The audio self-test gate controls the application of the PTS generated audio signal (PDGAUD$) to the PTS circuits used to test the processor unit audio signal (AUDIO/MA). This is accomplished in order to determine the operational status of the PTS audio circuits. In the self-test mode, PBITE$ goes low, enabling the audio self-test gate.

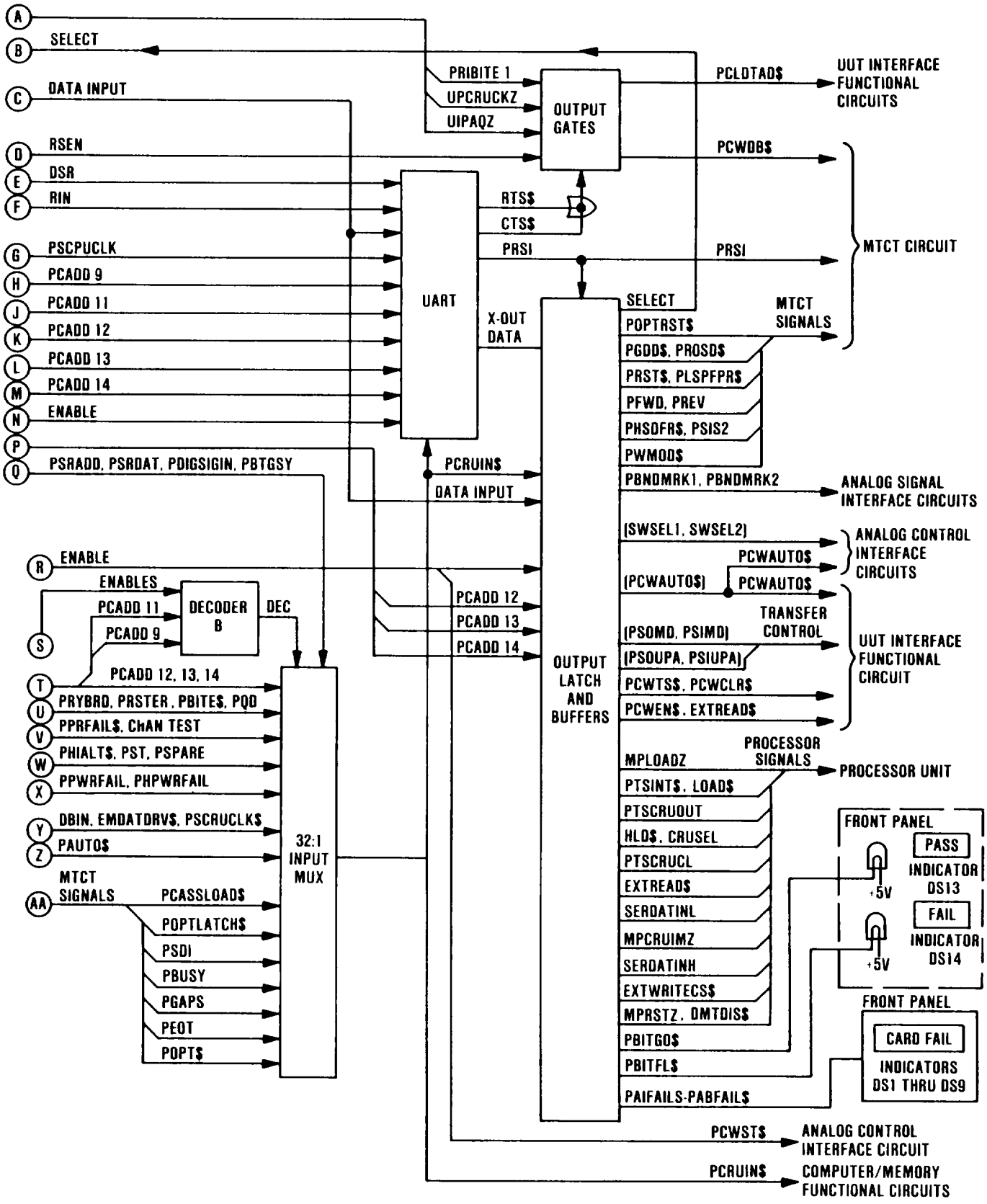
RECEIVER CONTROL DECODER/ENCODER

The receiver control decoder/encoder performs two distinct functions. First, the receiver control decoder/encoder detects the presence of STAFT and STFWD messages generated by the processor. Second, the receiver control decoder/encoder generates STAFT and STFWD messages for application to the processor unit during test, and to the UUT interface functional circuits during self-test.

Analog Signal Interface Circuit (Sheet 4 of 4)



Computer Interface Circuit (Sheet 1 of 4)



Computer Interface Circuit (Sheet 2 of 4)

COMPUTER INTERFACE CIRCUIT

The computer interface circuit performs three distinct functions. First, the circuit controls the transfer of data and response signals from the processor unit (under test), external equipment, and various circuits of the PTS to the computer/memory functional circuits to allow the computer/memory functional circuits to monitor the testing process. Second, the circuit controls the transfer of control signals and data from the computer/memory functional circuits to the processor unit (under test) and various circuits of the PTS to control the testing process. Third, the circuit controls the transfer of controls, response signals and data between the MTCT circuit and the computer/memory functional circuits. This allows test commands and data to be stored externally from the PTS memory.

DECODER A

Decoder A, when enabled by PCADD 3 and PCADD 10, decodes program instructions contained in the PCADD 6 thru PCADD 9 and PCADD 11 inputs to develop various ENABLE outputs. The ENABLE outputs control the functional operations of the other components of the computer interface circuit.

DECODER B

Decoder B, when enabled, decodes program instructions contained in PCADD 9 and PCADD 11 to select which portion of the 32:1 input MUX will accept input data and flags.

32:1 INPUT MUX

The 32:1 input MUX transfers data and flags from the various components of the PTS to the computer/memory functional circuits, providing feedback to the computer/memory functional circuits. When the 32:1 input MUX is enabled, PCADD 12 thru PCADD 14 select which input is transferred to the computer/memory functional circuits via the PCRUIN$ line.

SERIAL DATA MUX

The serial data MUX is a 2:1 MUX which allows software selection of input data from either the MTCT circuit (PCASSDATA) or the external equipment (PRSDATIN) through the PTS. Selection of which data is to be transferred is a function of the SELECT input, which is developed in accordance with programmed instructions.

Computer Interface Circuit (Sheet 3 of 4)

UART

The UART controls the data transfer to the front panel I/O functional circuits. When enabled by the ENABLE input, the UART responds to program instructions (PCADD 9 and PCADD 11 thru PCADD 14), and selects the data transfer function (read or write operations), and the source and destination of the data transfer. Data is transferred into and out of the UART by PSCPUCLK.

OUTPUT LATCH AND BUFFERS

The output latch and buffers complete the data transfer circuit from the front panel I/O functional circuits to the other components of the PTS, and to the processor unit (under test). When enabled by the ENABLE input, the output latch and buffers respond to program instructions (PCADD 12 thru PCADD 14) and transfer the data (either PSCRUOUT$ via the DATA INPUT or X-OUT DATA) to the appropriate destination.

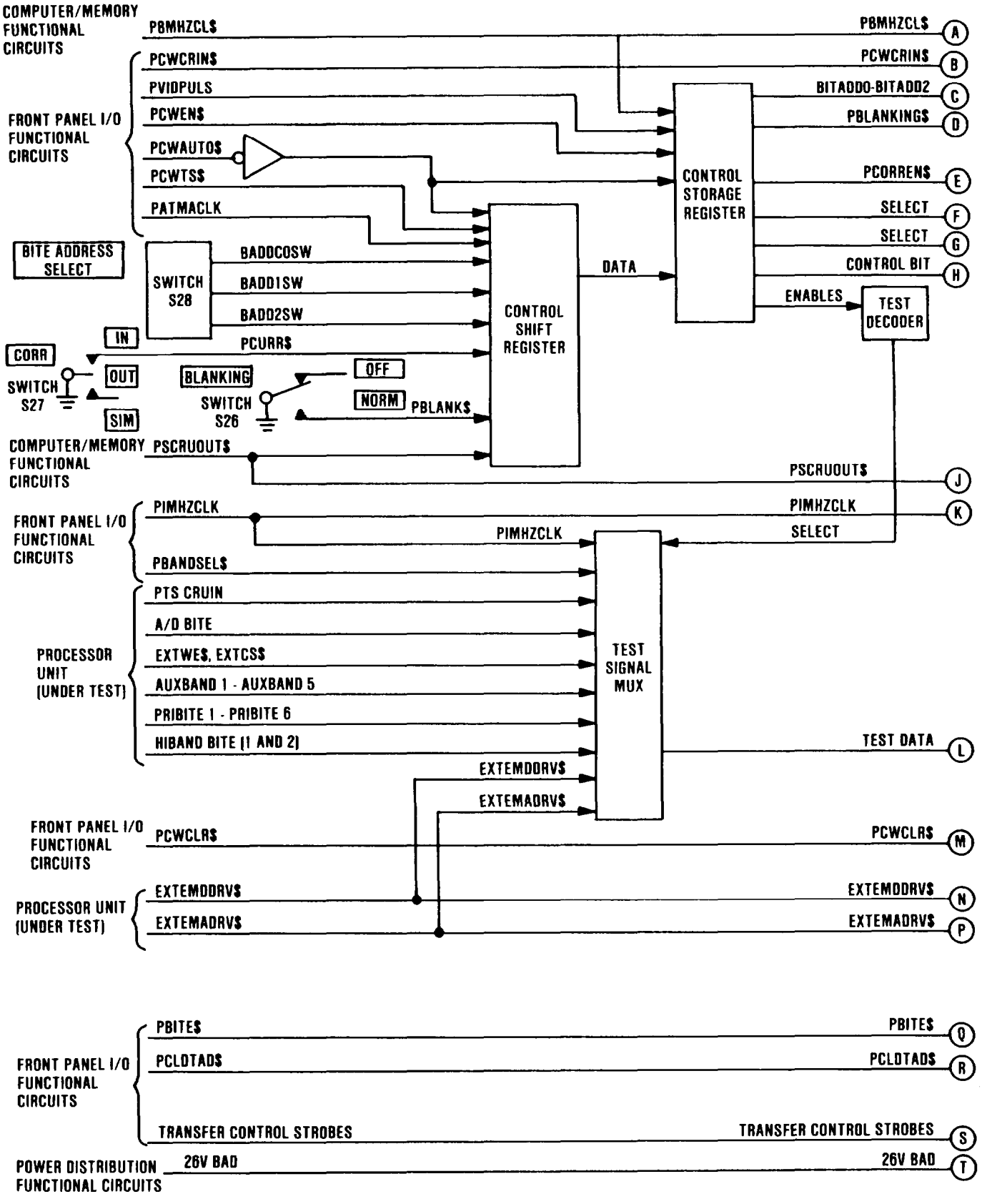
OUTPUT GATES

The output gates perform two functions. First, the gates, when enabled by either CTS$ or RTS$, apply serial data to the MTCT circuit over the PCWDB$ line. Second, the gates, when enabled by UPIAQZ and PRIBITE1, apply UPCRUCKZ (as PCLDTAD$) to clock the UUT interface functional circuits during self-test functions.

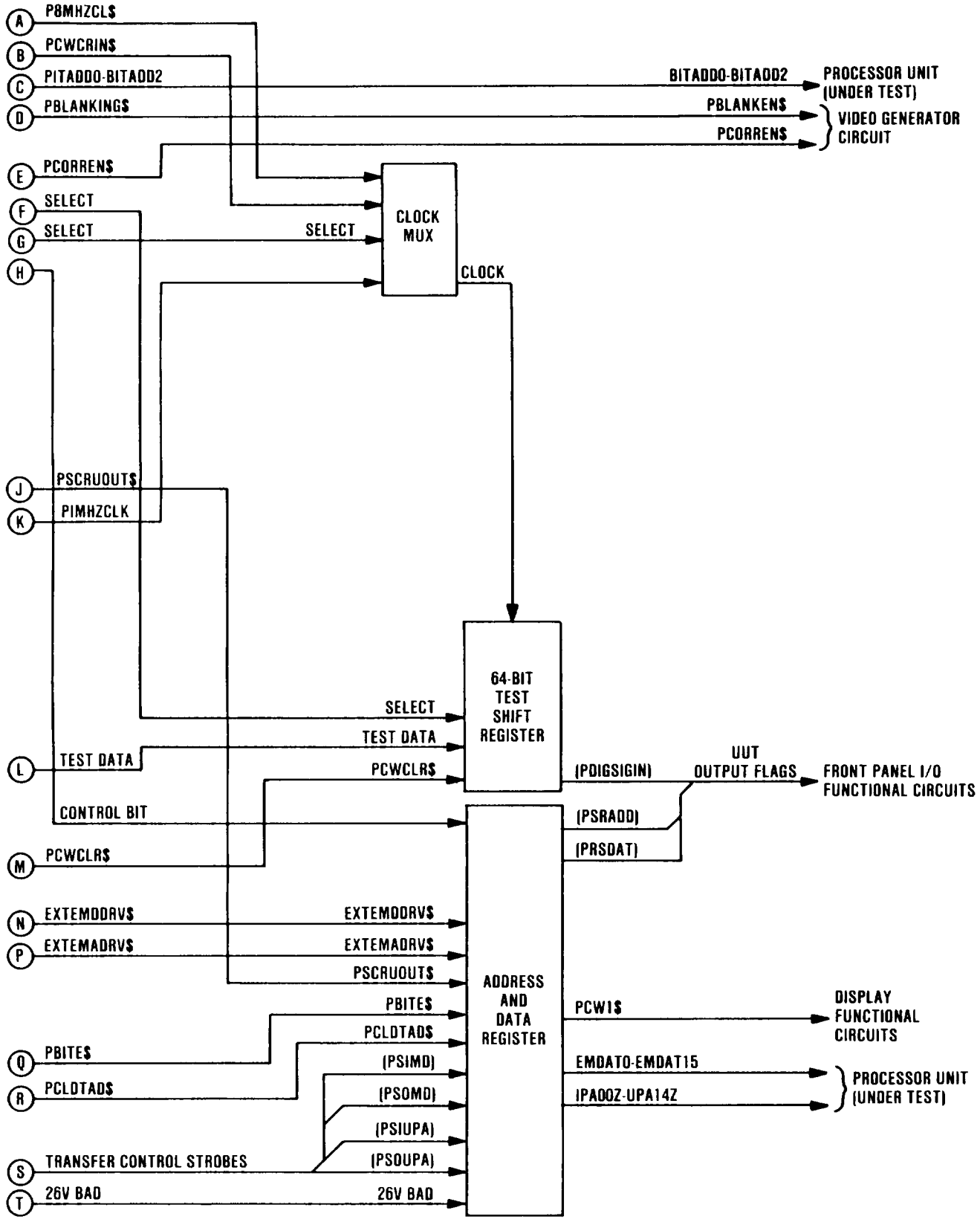
LAMP DRIVERS

The lamp drivers provide the current handling capabilities required to drive the front panel indicators.

Computer Interface Circuit (Sheet 4 of 4)



Digital Signal Processor Circuit (Sheet 1 of 4)



Digital Signal Processor Circuit (Sheet 2 of 4)

DIGITAL SIGNAL PROCESSOR CIRCUIT

The digital signal processor circuit performs three distinct functions. First, the circuit controls the transfer of digital test data, data bits and address bits from the processor unit (under test) to the front panel I/O functional circuits to monitor the testing of the processor unit. Second, the circuit controls the transfer of digital data bits and address bits to the processor unit (under test) to drive the processor unit to develop the desired response signals. Third, the circuit develops switch data to control testing of the processor unit (under test), and selects the desired points in the processor unit for interconnection to the front panel test points.

CONTROL SHIFT REGISTER

The control shift register latches test switch data inputs (representing the settings of the front panel BLANKING, CORR and BITE ADDRESS SELECT switches) after the register has been cleared by PCWTS$. In the manual mode (PCWAUTO$ is high), the test switch data from the front panel switches are parallel-shifted into the register by PATMACLK. In the auto mode of operation (PCWAUTO$ is low), the test switch data contained in the PSCRUOUT$ line is serially-shiftied into the register.

CONTROL STORAGE REGISTER

The control storage register latches the test data output of the control shift register and applies the data as control bits to control the functional operations of the digital signal processor circuit. The control storage register is first enabled by PCWEN$ and PVIDPULS. DATA is then parallel-shifted into the register by PS8MHZCL$.

CLOCK MUX

The clock MUX selects various clocks for use as timimg signals during testing and self test. Selection is a function of the SELECT output from the control storage register.

TEST DECODER

The ENABLES input are decoded by the test decoder. The test decoder develops SELECT outputs which determine which inputs to the test signal MUX are applied through the test signal MUX to the 64-bit test shift register.

Digital Signal Processor Circuit (Sheet 3 of 4)

TEST SIGNAL MUX

The test signal MUX accepts various inputs for application to the 64-bit test shift register. Each input is applied through the MUX in accordance with the SELECT input code.

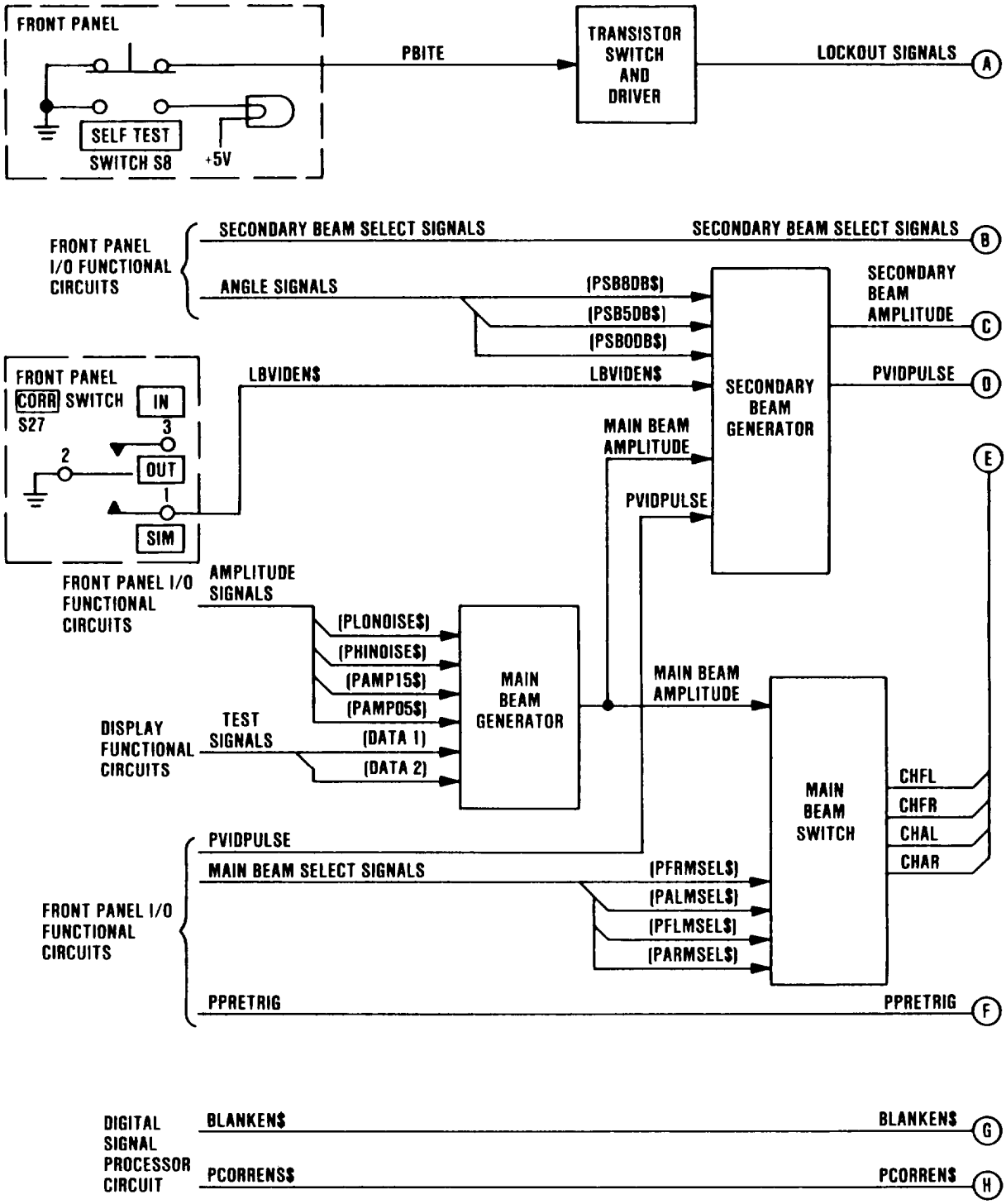
64-BIT TEST SHIFT REGISTER

The 64-bit test shift register is used during self-test mode only. Provisions for using this register during the automatic mode of testing have been made; however, these provisions are being reserved for future expansion. Currently, in the self-test mode of operation, the register is cleared by PCWCLR$. TEST DATA is then serially-shifted into the 64-bit test shift register from the test signal MUX by the CLOCK output of the clock MUX. The data is then serially-shifted out of the register (by the CLOCK output of the clock MUX), and applied (via the front panel I/O functional circuits) to the computer/memory functional circuits. The data is checked against the original input data by the computer/memory functional circuits, as part of a parity check.

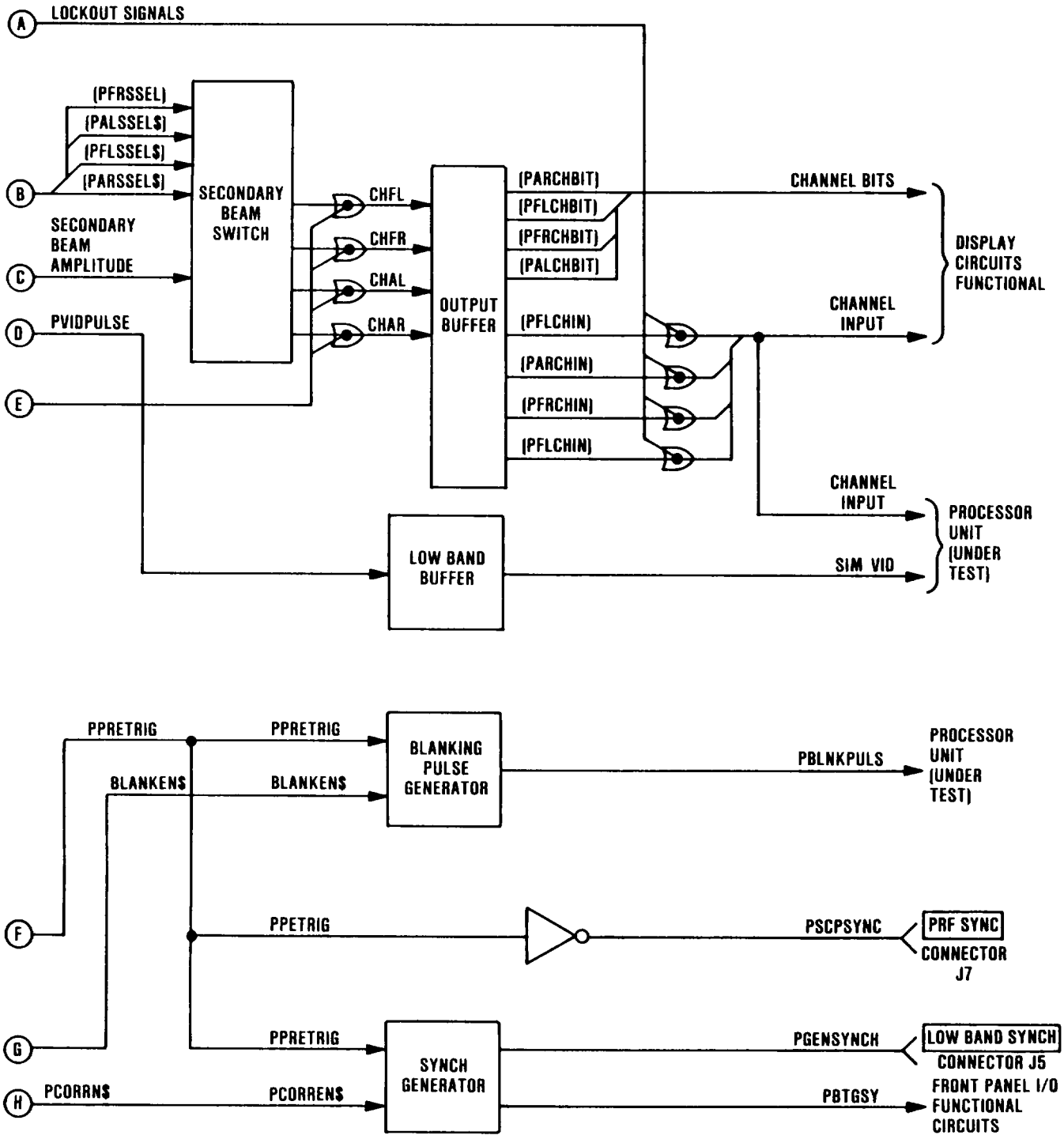
ADDRESS AND DATA REGISTER

The address and data register controls the transfer of data and address bits between the processor unit (under test) and the front I/O functional circuits. The register also develops the PCW1 $ strobe to the display functional circuits. When the register is enabled by low level PBITE$, data and address bits are serially-shifted into the register by PCLDTAD$. The TRANSFER CONTROL STROBES determine the type of transfer to take place. For a parallel transfer, data and address bits are parallel-shifted out of the register as EMDATO thru EMDAT15, and UPAOOZ thru UPA14Z. For a serial transfer, data and address bits are serially-shifted out of the register as PSRDAT and PSRADD.

Digital Signal Processor Circuit (Sheet 4 of 4)



Video Generator Circuit (Sheet 1 of 4)



Video Generator Circuit (Sheet 2 of 4)

VIDEO GENERATOR CIRCUIT

The video generator circuit performs three distinct functions. First, in the test (or normal) mode of operation, this circuit generates the CHANNEL INPUT signals which are used to simulate the radar receiver output pulses in a normal system configuration. These pulses are used to test the input processing circuits of the processor unit (under test). Second, in the self-test mode of operation, the video generator circuit generates CHANNEL BITS, which select the strobes (generated by the display functional circuits) used to test the PTS. Third, this circuit generates the blanking pulse outputs required by the processor unit (under test), and synch outputs required during self-test and maintenance operations.

MAIN BEAM GENERATOR

TEST SIGNALS, developed by the display functional circuits, drive the main beam generator to produce a pulse (MAIN BEAM AMPLITUDE). The magnitude of the pulse is determined by the AMPLITUDE SIGNALS which represent the setting of the front panel AMPLITUDE switch. The output of the main beam generator forms the basic pulse input (strongest signal positional pulse) for the processor unit (under test). The strength of the MAIN BEAM AMPLITUDE pulse, in conjunction with the SECONDARY BEAM AMPLITUDE pulse, determine the position of the simulated target displayed on the radar signal indicator unit.

MAIN BEAM SWITCH

The main beam switch transfers the pulses (MAIN BEAM AMPLITUDE) to the desired output channel (CHFR, CHAL, CHAR or CHFL), selected by the MAIN BEAM SELECT SIGNALS.

SECONDARY BEAM GENERATOR

The secondary beam generator divides the MAIN BEAM AMPLITUDE pulses down to values selected by the ANGLE SIGNALS. These pulses are the weakest signal positional pulses. The ANGLE SIGNALS represent the setting of the DF SELECT angle switch and are developed in accordance with the angular position of the simulated target, within the designated octant. When the front panel CORR switch (S27) is set to the SIM position, LBVIDEN$ goes low. The secondary beam generator then applies PVIDPULSE to the low band buffer.

SECONDARY BEAM SWITCH

The secondary beam switch transfers the pulses (SECONDARY BEAM AMPLITUDE) to the output channel (CHFR, CHAL, CHAR a CHFL) selected by the SECONDARY BEAM SELECT SIGNALS.

Video Generator Circuit (Sheet 3 of 4)

OUTPUT BUFFER

The output buffer provides isolation between the circuits generating the channel bit (PARCHBIT, PFLCHBIT, PFRCHBIT and PALCHBIT) and channel inputs (PARCHIN, PFLCHIN, PFRCHIN and PALCHIN) and the functional circuits utilizing these signals.

LOW BAND BUFFER

The low band buffer receives PVIDPULSE from the secondary beam generator when LBVIDEN$ goes low. The pulse (PVIDPULSE) is converted from a digital pulse to an analog equivalent and applied (as SIM VID) to the processor unit under test.

TRANSISTOR SWITCH AND DRIVER

When front panel SELF TEST switch S8 is depressed, the PTS enters self-test mode. In the self-test mode of operation, PBITE goes high, turning on the transistor switch and driver. The transistor switch and driver develops lockout signals which prevent the channel inputs (PFLCHIN, PARCHIN, PFRCHIN and PALCHIN) from being applied to the processor unit (under test) during self-test. The remaining components of the video generator circuit function in the same manner as previously described.

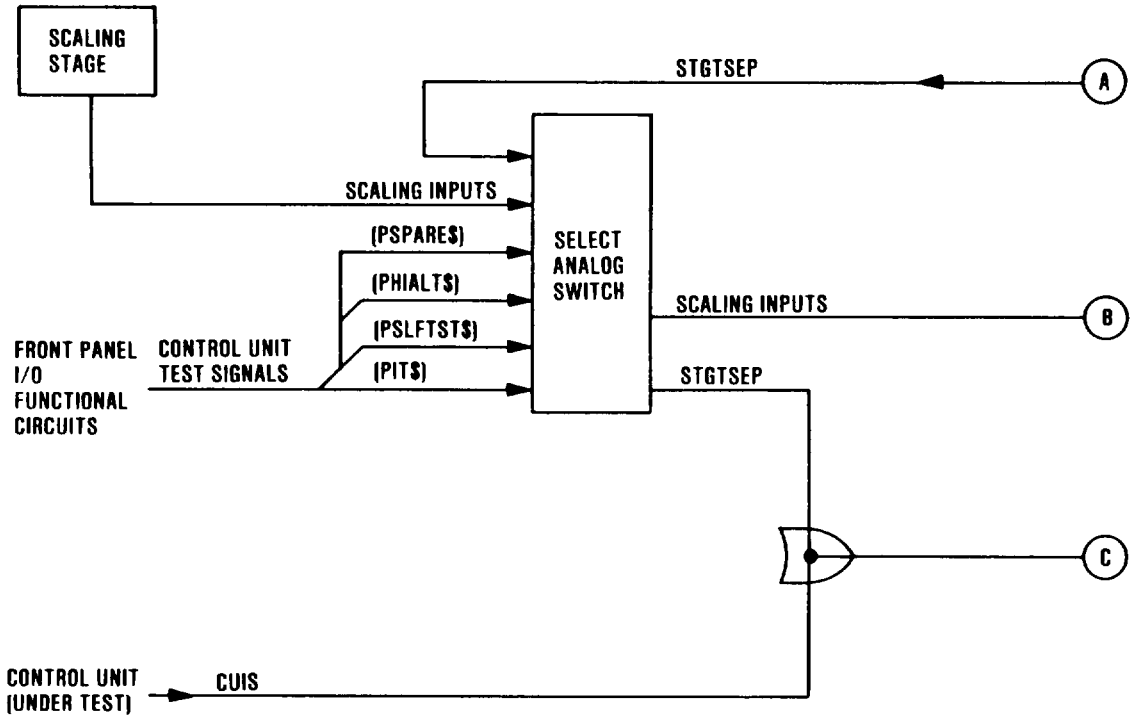
BLANKING PULSE GENERATOR

The blanking pulse generator develops the 120-millisecond pulse-width PBLNKPULS output that is applied to the processor unit (under test). The pulse is used for testing purposes within the processor unit. The PBLNKPULS output is developed when BLANKEN$ goes low, and PPRETRIG is applied to the input of the blanking pulse generator.

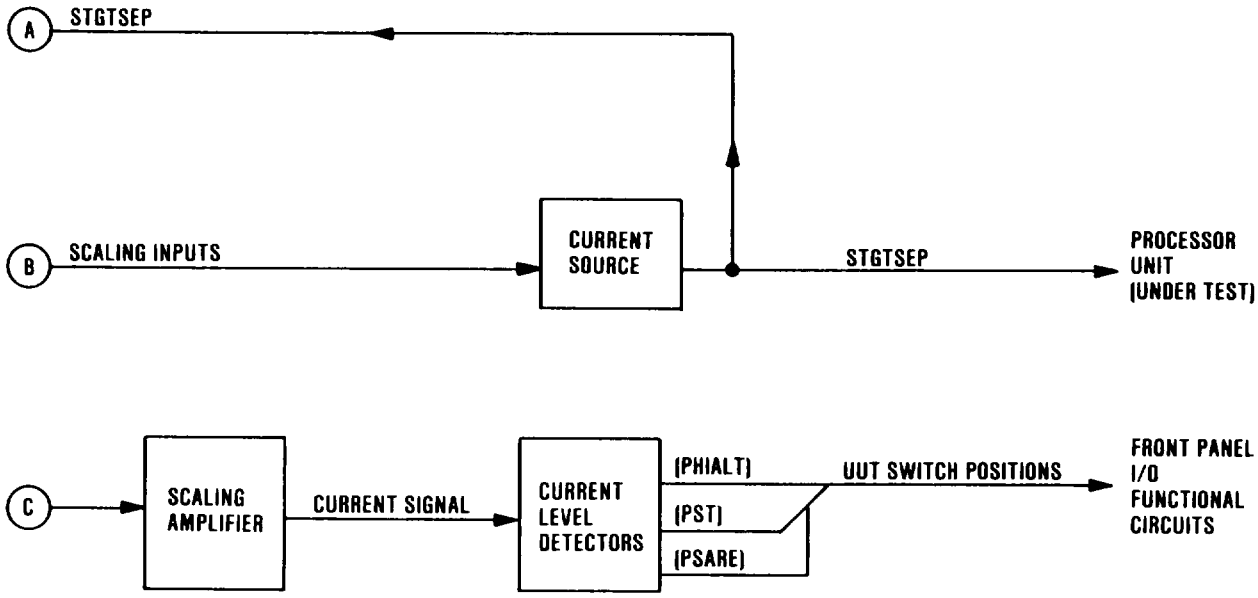
SYNCH GENERATOR

The synch generator develops the 1.75-microsecond PGENSYNC output pulses applied to LOW BAND SYNC connector J5. The pulses are generated when PCORREN$ goes low (indicating that the low band circuits have been enabled) and the PPRETRIG pulse is applied to the input of the synch generator. The synch generator also develops the PBTGSY output pulses which are used as an internal sync flag during self-test functions.

Video Generator Circuit (Sheet 4 of 4)



Display Protect Circuit (Sheet l of 4)



Display Protect Circuit (Sheet 2 of 4)

DISPLAY PROTECT CIRCUIT

The display protect circuit performs three distinct functions. First, the circuit simulates the control unit functions to test the switch decoder circuits in the processor unit (under test). Second, the circuit simulates the processor unit switch decoder circuits to test the switch encoder circuits of the control unit (under test). Third, the circuit performs a partial self-test of the PTS switch simulation and encoder test circuits to determine their operational status.

SCALING STAGE

The scaling stage is comprised of resistors whose values are chosen so as to drive the current source to develop a current signal, whose magnitude can be properly detected by the processor unit (under test). Effectively, this simulates the function of the control unit for test purposes. The resistors of the scaling stage are connected to the current source when the appropriate enables (PSPARE$, PSLFTST$ and PHIALT) are applied to the select analog switch.

SELECT ANALOG SWITCH

The select analog switch controls the interconnection of the scaling circuit and current source, during the test mode of operation, to develop the proper magnitude of current flow for current decoding circuits in the processor unit (under test). The select analog switch also interconnects the output of the current source to the input of the scaling amplifier (during the self-test mode of operation, to test the components of the display protect circuit.

CURRENT SOURCE

The current source develops the current signal that is used to drive the current decoding circuits within the processor unit (under test). The magnitude of the current signal represents the particular switch (of the control unit) that is being simulated.

SCALING AMPLIFIER

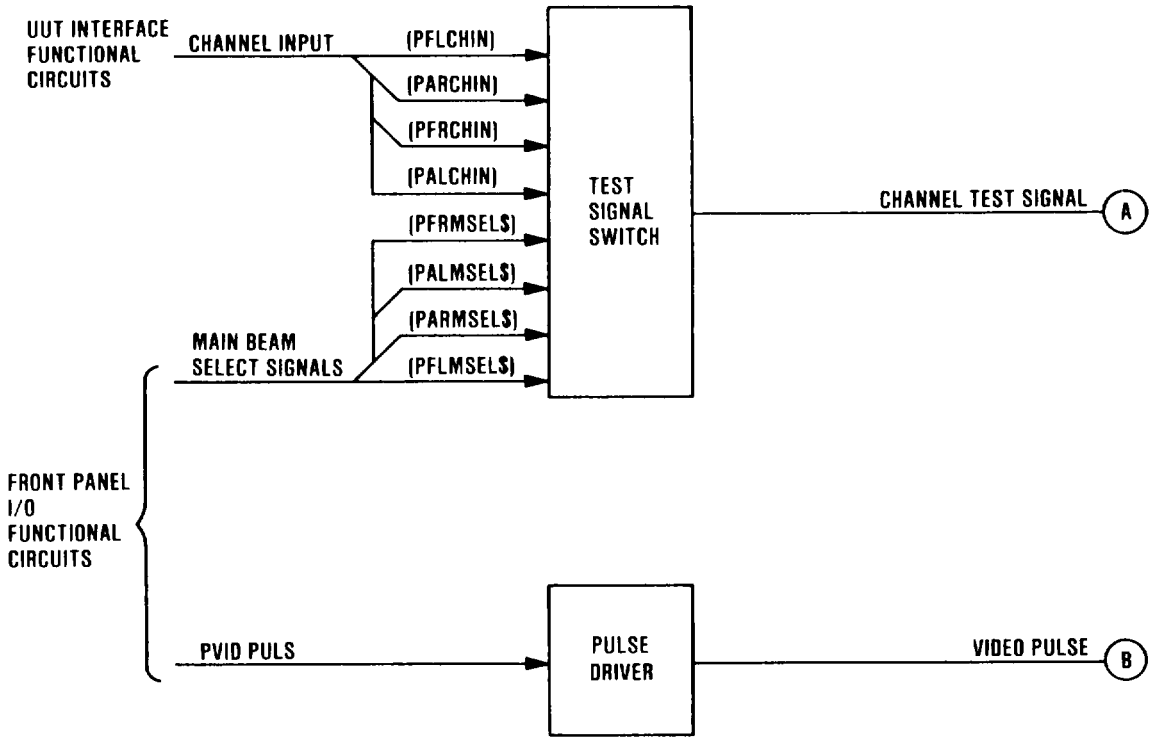
Detection and testing of the current source signal (CUIS) developed by the control unit (under test) is a function of the scaling amplifier and current level detectors. The scaling amplifier amplifies the CUIS signal to develop a signal whose magnitude is compatible with the current level detectors.

Display Protect Circuit (Sheet 3 of 4)

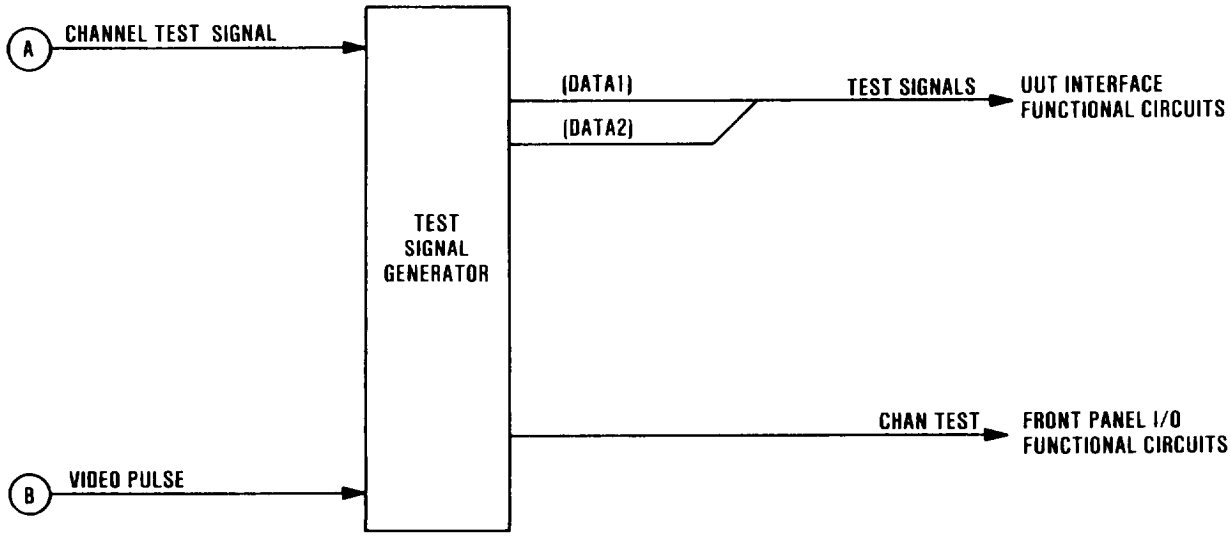
CURRENT LEVEL DETECTORS

The current level detectors sample the output of the scaling amplifier to determine which switch in the control unit (under test) has been depressed. The current level detectors compare the magnitude of the current flow of the input against preset values. If the magnitude of the current flow matches the preset value, the current level detectors develop an enable signal (PH1ALT$, PST, or PSPARE) which indicates that a switch has been depressed.

Display Protect Circuit (Sheet 4 of 4)



Video Generator Circuit (Sheet 1 of 3)



Video Generator Circuit (Sheet 2 of 3)

VIDEO GENERATOR CIRCUIT

The video generator circuit performs two basic functions within the display functional circuits. First, in the test (or normal) mode of operation, this circuit develops the pulse signal required to drive the UUT interface functional circuits to produce simulated radar receiver output pulses for use in testing the processor unit input signal processing circuits. Second, in the self-test mode of operation, this circuit produces a test signal (CHAN TEST). The test signal is generated in response to inputs (CHANNEL INPUTS) from the UUT interface functional circuits and acts as a flag denoting the functional status of the UUT interface functional circuits.

PULSE DRIVER

The pulse driver converts the digital PVIDPULS signal to an analog representation (VIDEO PULSE) of the input, so that the pulse is compatible with the analog circuitry of the video generator circuit. The VIDEO PULSE is used as the basic input pulse for developing TEST SIGNALS and the CHAN TEST.

TEST SIGNAL GENERATOR

The test signal generator performs two basic functions. First, in the test (or normal) mode of operation, VIDEO PULSE is shaped to represent two different pulses (TEST SIGNALS). These signals are used to drive the main beam generator in the UUT interface functional circuits. Second, in the self-test mode of operation, the test signal generator develops a triangular test signal (CHAN TEST). The test signal, when checked by the software program, provides a partial check of the functional status of the video generator card.

TEST SIGNAL SWITCH

The test signal switch controls the application of the appropriate CHANNEL INPUT to the test signal generator to permit testing of each of the generation channels. Selection of the appropriate CHANNEL INPUT is accomplished by the MAIN BEAM SELECT SIGNALS.

Video Generator Circuit (Sheet 3 of 3)

DISPLAY PROTECT CIRCUIT

The display protect circuit performs two distinct functions within display functional circuits. First, in the test (or normal) mode of operation, this circuit samples the video pulses generated by the processor unit (under test), to ensure that the parameters of the pulses (duty cycle and pulse width) are within accepted limits. Second, in the self-test mode of operation, the circuit generates bit pulses used to develop the self-test strobes which test the operation of the display protect circuits themselves.

POWER ON STAGE

When power is first applied to the PTS, the power on stage develops a POWER ON RESET to initialize the display protect circuits. The POWER ON RESET clears the failure latch, which in turn, sets the state decoder and triggers the reset stage.

INPUT MUX

The input MUX applies the PROCESSOR VIDEO (POSM, POSK, NEGM and NEGK) to the analog or gate. The MUX is provided for future expansion purposes only.

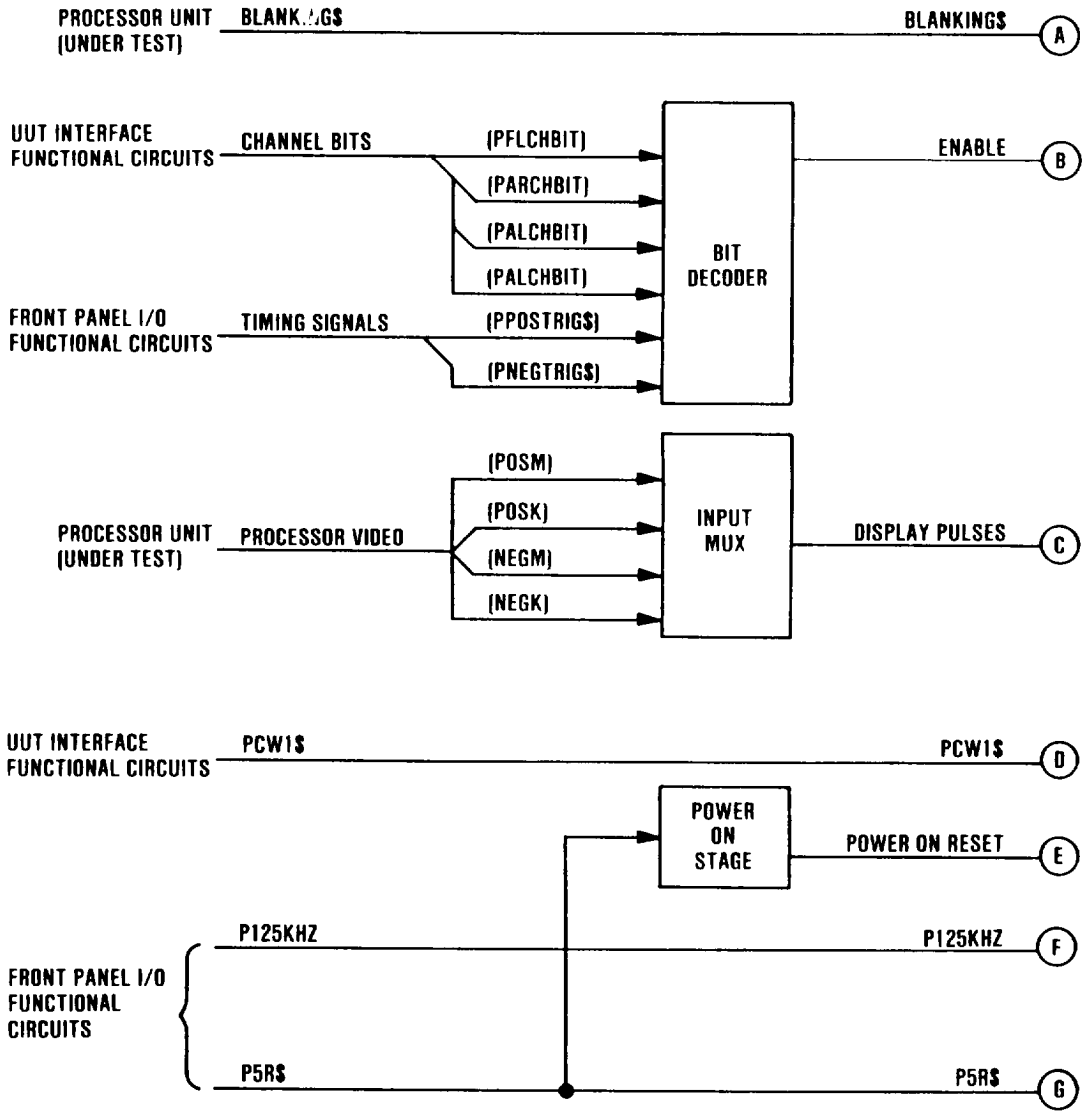
ANALOG OR-GATE

The analog OR-gate is a wired OR-gate that passes either the DISPLAY PULSES, or the PTS SELF-TEST STROBES (generated by the bit signal generator), to the output MUX, and the summing network.

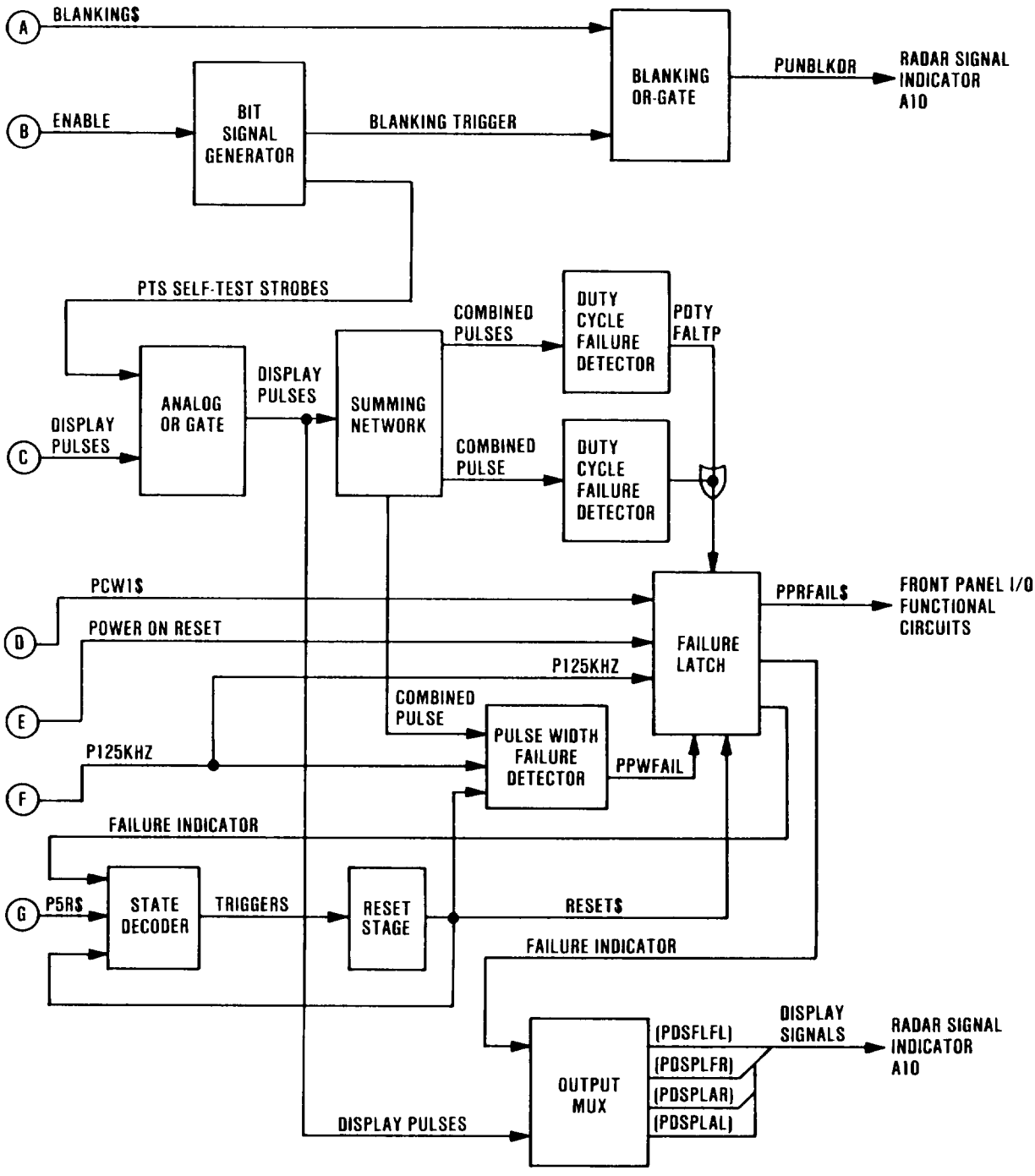
OUTPUT MUX

The output MUX selects one of two inputs (either analog ground or DISPLAY PULSES) for application to the radar signal indicator unit as DISPlAY SIGNALS. This allows the radar signal indicator unit to be disconnected during the re-initialization cycle. When no failure has been detected, the DISPLAY PULSES are selected by the output MUX. When a failure has occurred, the FAILURE INDICATOR input drives the output MUX to select the analog ground input for 1.5 milliseconds.

Display Protect Circuit (Sheet 1 of 5)



Display Protect Circuit (Sheet 2 of 5)



Display Protect Circuit (Sheet 3 of 5)

SUMMING NETWORK

The summing network is comprised of two summing circuits: one summing circuit for each set of opposing DISPLAY PULSES (NEGK and POSK, and NEGM amd POSM). Each summing circuit develops a COMBINED PULSE that is representative of the two inputs, and is used for checking the parameters of the video outputs to the radar signal indicator unit.

DUTY CYCLE FAILURE DETECTORS

The duty cycle failure detectors check the voltage rise time for the COMBINED PULSE to determine if the duty cycle of the pulse falls within acceptable parameters. Assuming that the duty cycle parameters are acceptable, the duty fail signal (PDTYFALTP) remains low. If the duty cycle parameters are unacceptable, the duty fail signal goes high. The duty fail signal is applied as one input to the failure latch.

PULSE WIDTH FAILURE DETECTOR

The pulse width failure detector checks the pulse width of the COMBINED PULSE to determine if the pulse width of the pulses fall within acceptable parameters. If the parameters are acceptable, the pulse width fail signal (PPWFAIL) remains high. If the parameters are unacceptable, the pulse width fail signal goes low. This signal is applied as a second input to the failure latch.

FAILURE LATCH

The failure latch re-initializes the display protect circuits and shuts down the video outputs to the radar signal indicator unit when a failure is detected. The failure latch is normally in the reset state with PPRFAIL$ high (indicating a non-failure state), and the FAILURE INDICATOR drives the output MUX to output the DISPLAY PULSES (as DISPLAY SIGNALS) to the radar signal indicator unit. If the duty cycle failure detectors or pulse width failure detector determine that a failure exists, the failure latch is set. With the latch set, PPRFAIL$ goes low (signfying that a failure has occurred), and the FAILURE INDICATOR outputs drive the output MUX to output analog ground to the radar signal indicator unit, and set the state decoder. The state decoder triggers the reset circuit, starting the reset cycle.

STATE DECODER

The state decoder detects the failure state (as opposed to a normal operational state) and triggers the reset circuit. This action effectively re-initializes the display protect circuit.

Display Protect Circuit (Sheet 4 of 5)

RESET STAGE

The reset stage, when triggered by the state decoder, develops a reset pulse output (RESET$). This output initiates the 1.5-millisecond reset cycle. During the reset cycle, the failure latch and state decoder are reset.

BIT DECODER

In the self-test mode of operation, the TIMING STROBES are decoded to determine whether forward (positive) on aft (negative) strobes will be generated. The PPOSTRIG$ input, when applied, routes CHANNEL BITS (PFLCHBIT and PFRCHBIT) to the bit signal generator for processing. The PNEGTRIG$ input, when applied, routes PALCHBIT and PARCHBIT to the bit signal generator for processing.

BIT SIGNAL GENERATOR

The bit signal generator develops the actual PTS SELF-TEST STROBES that are applied to the radar signal indicator unit during the self-test mode of operation. The bit signal generator also develops BLANKING TRIGGER which is used to unblank the radar signal indicator unit during the generation of strobes.

BLANKING OR-GATE

The blanking OR-gate passes either BLANKING$ (test mode of operation) or BLANKING TRIGGER (self-test mode of operation) as PUNBLKDR to the radar signal indicator unit. The PUNBLKDR output unblanks the radar signal indicator unit during strobe generation.

Display Protect Circuit (Sheet 5 of 5)

CHAPTER 3

OPERATING INSTRUCTIONS

CHAPTER CONTENTS

SECTION I

DESCRIPTION AND USE OF CONTROLS AND INDICATORS

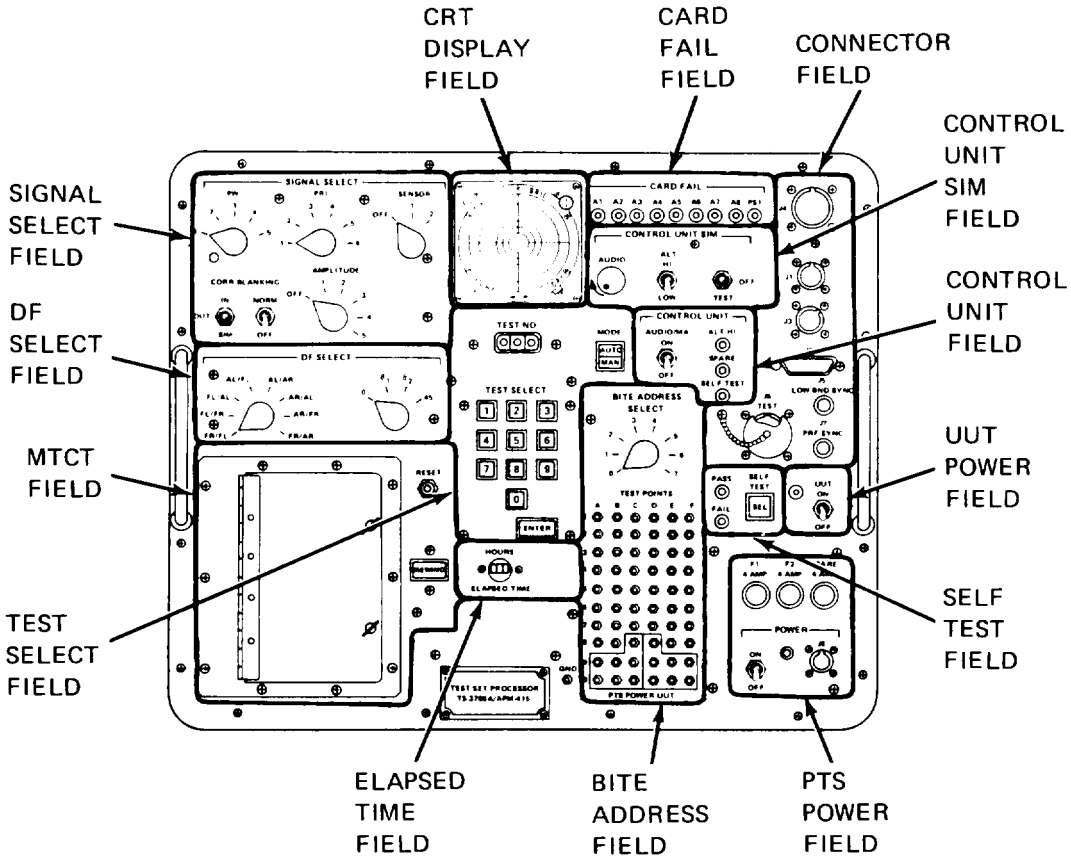
SECTION CONTENTS

PURPOSE

3-l. Cooperate and maintain Processor Test Set AN/APM-41 5A, you must know the location and function of all controls, indicators and connectors. This section describes the controls, indicators and connectors of the processor test set.

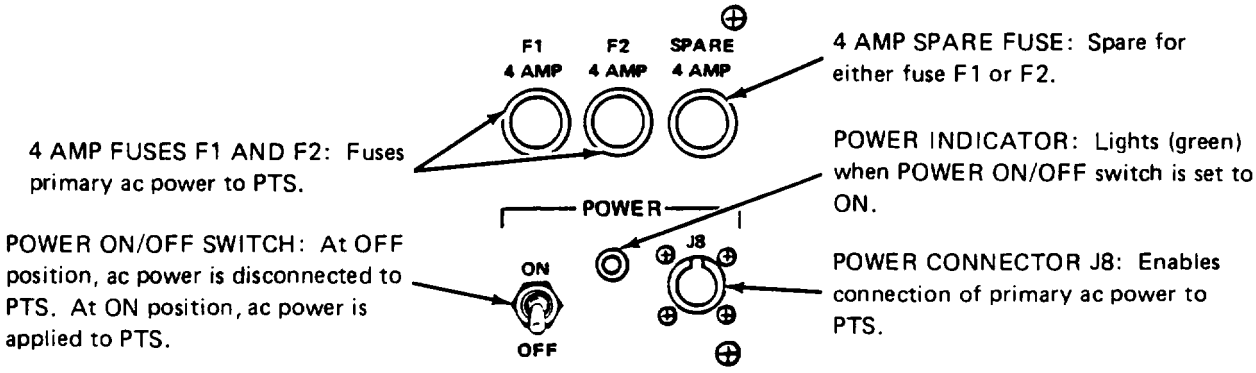
PTS FRONT PANEL

3-2. All controls, indicators and connectors of the processor test set are contained on the PTS front panel. The illustration below shows the PTS front panel controls, indicators and connectors which have been grouped together in fields. These fields are explained in the following paragraphs in their order of importance.



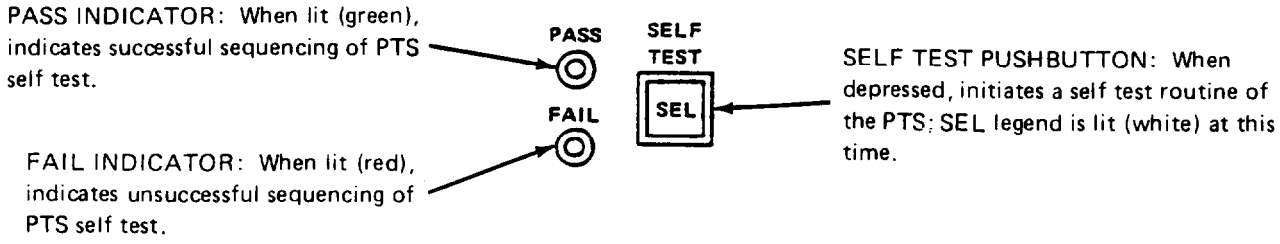
PTS POWER FIELD

3-3. The PTS power field permits you to apply primary ac power to the PTS. The function of each field item is provided below.



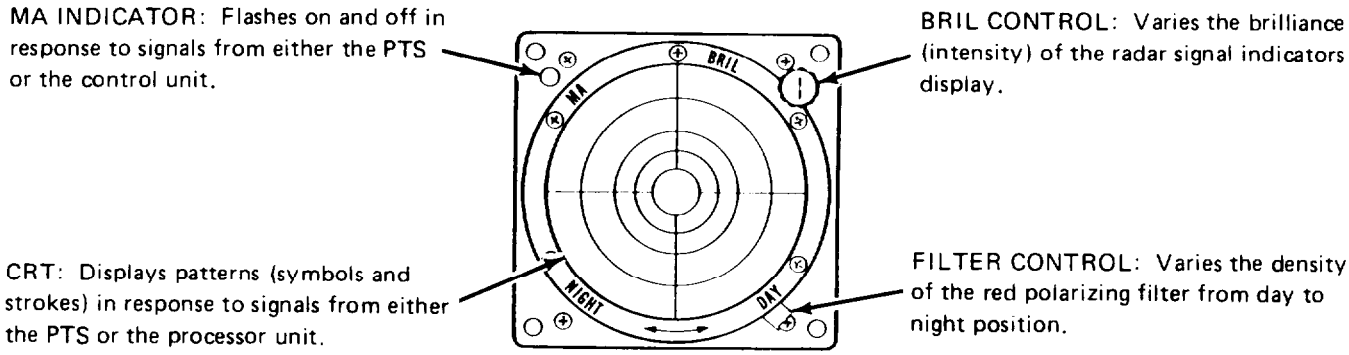
SELF TEST FIELD

3-4. The self test field permits you to perform an internal self test of the PTS. The function of each field item is provided below.



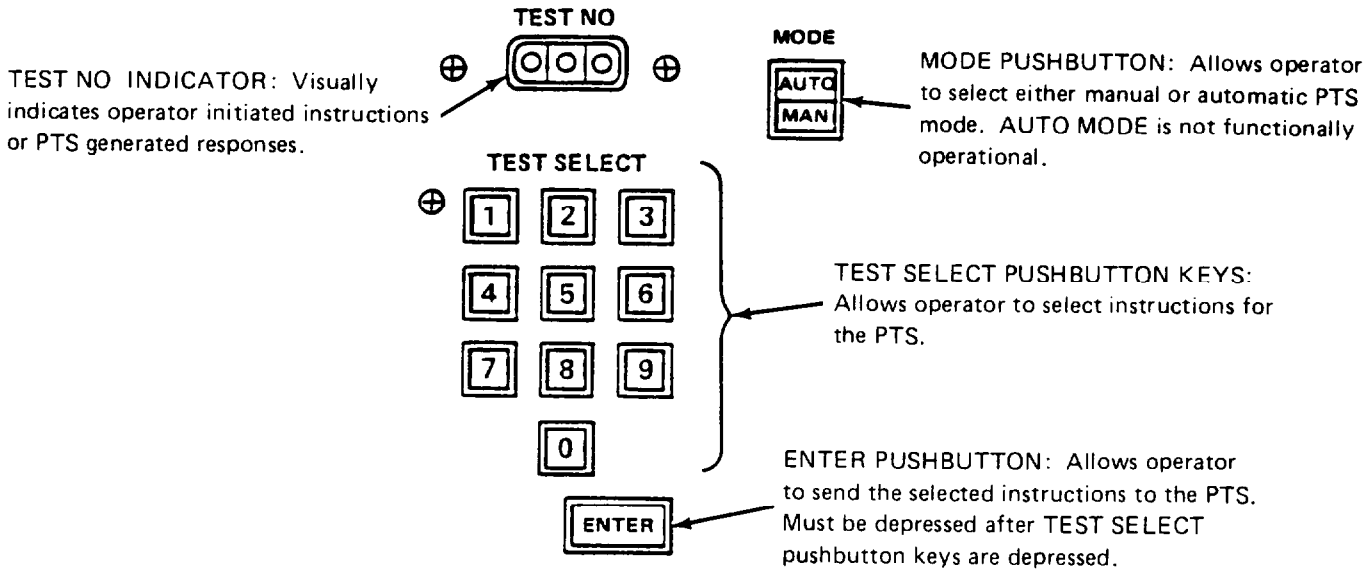
CRT DISPLAY FIELD

3-5. The CRT display field permits you to visually check the processor unit or PTS self test outputs. The function of each field item is provided below.



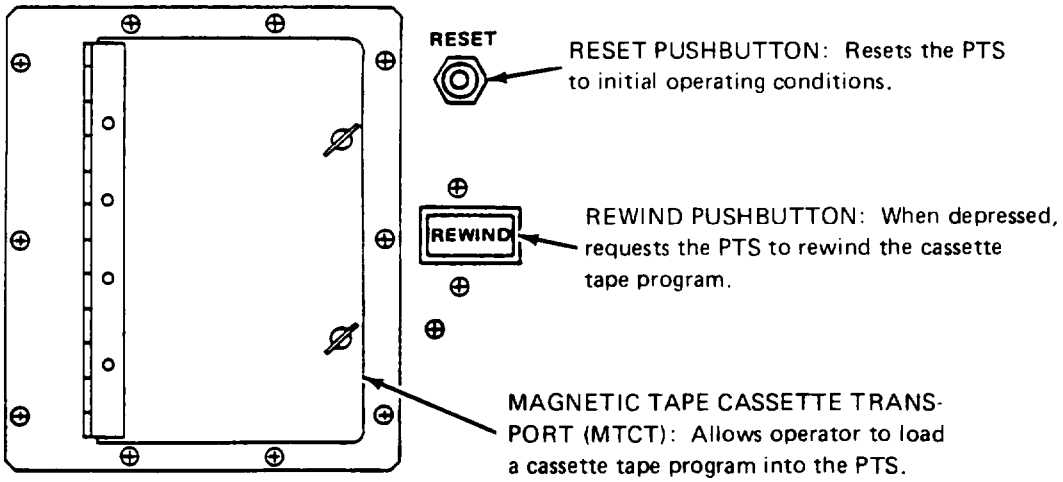
TEST SELECT FIELD

3-6. The test select field permits you to select test program subroutines from either the PUT diagnostic program or other type programs. The function of each field item is provided below.



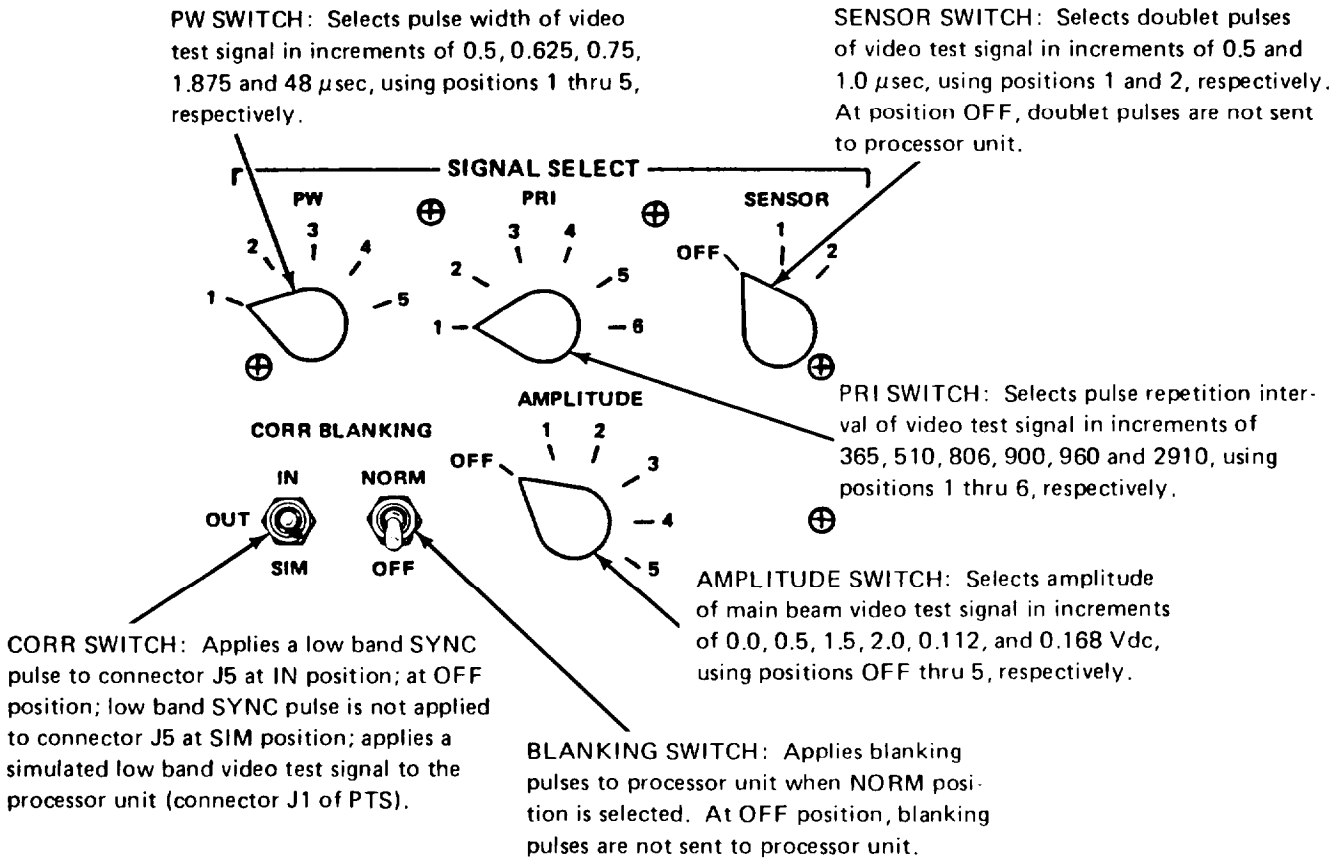
MTCT FIELD

3-7. The MTCT field permits you to load the PUT diagnostic or memory verification cassette tapes into the PTS. The function of each field item is provided below.



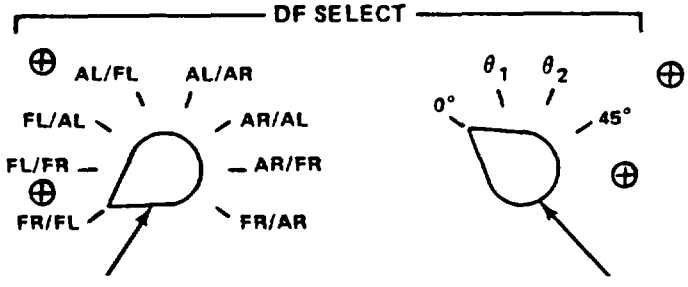
SIGNAL SELECT FIELD

3-8. The signal select field permits you to select parameters of the input video test signal, sent from the PTS to the processor unit. The function of each field item is provided below.



DF SELECT FIELD

3-9. The DF select field permits you to select the octant and angle of the input video test signal, sent from the PTS to the processor unit. The function of each field item is provided below.

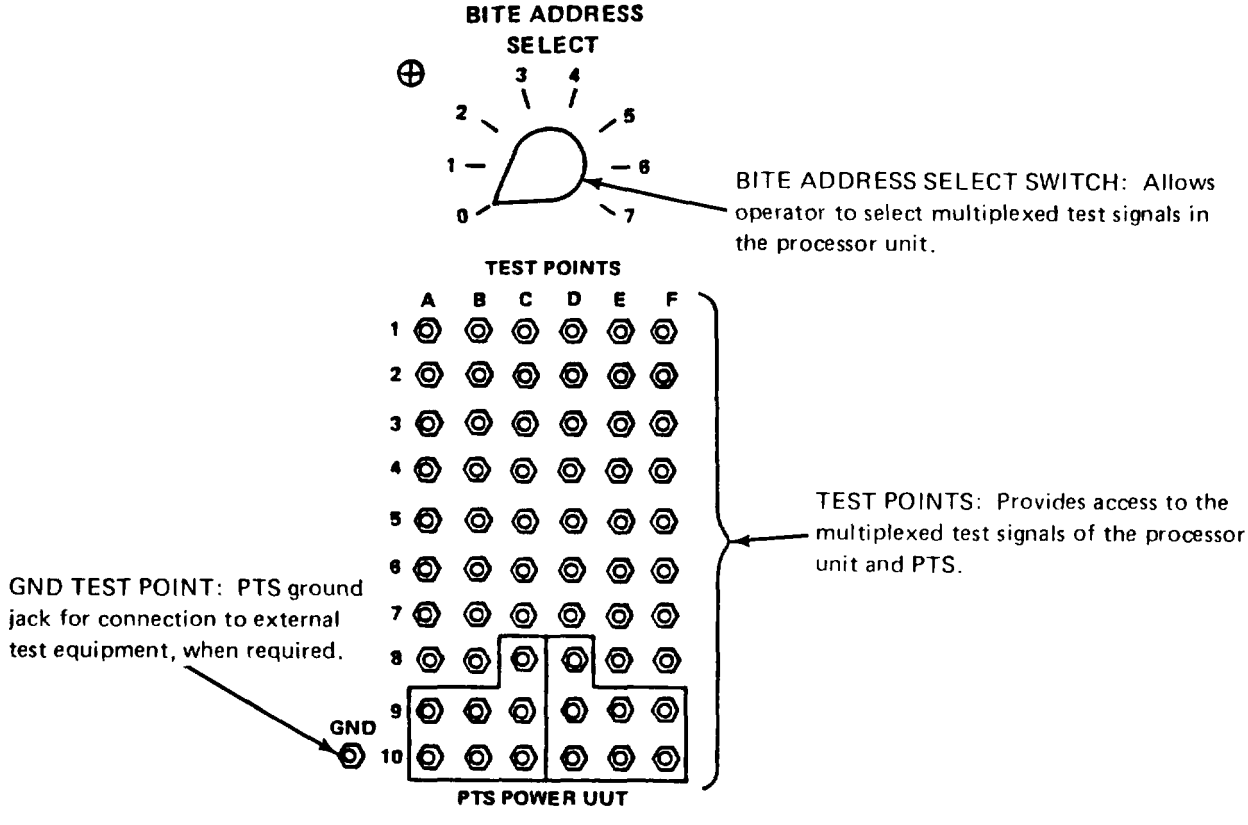


OCTANT SWITCH: Selects the octant by setting the main beam and secondary beam of the video test signals according to aft left (AL), aft right (AR), fwd left (FL), and fwd right (FR). Each switch position defines main beam/secondary beam.

ANGLE SWITCH: Selects the amplitude ratio of the secondary beam to the main beam of the video test signals, in increments of 100%, 50%, 40% and 0%, using positions 0°, θ1, θ2, and 45°, respectively.

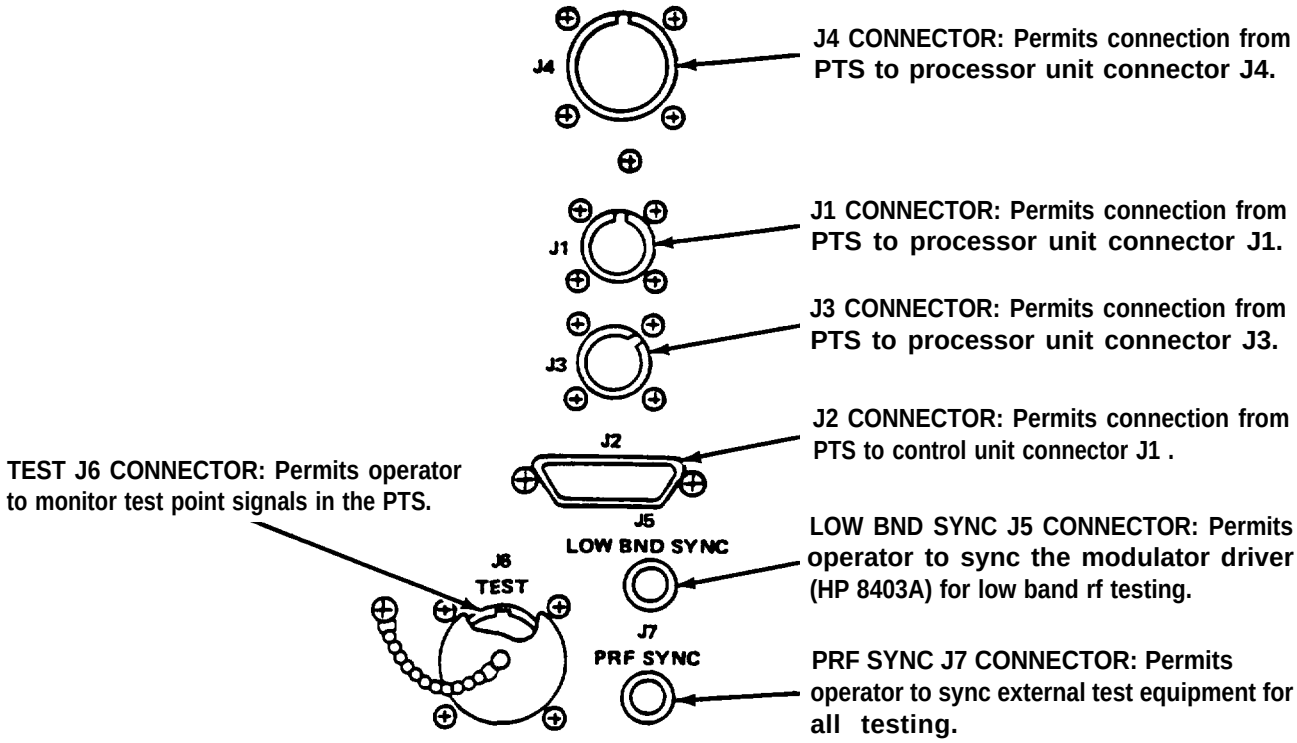
BITE ADDRESS FIELD

3-10. The BITE address field permits you to select and monitor desired test point signals in either the processor unit or PTS. The function of each field item is provided below.



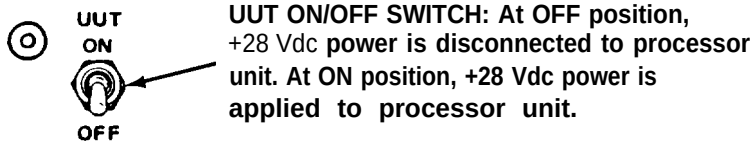
CONNECTOR FIELD

3-11. The connector field permits you to interconnect the PTS to either the processor unit or control unit and also allows you to monitor test point signals in the PTS. The function of each field item is provided below.



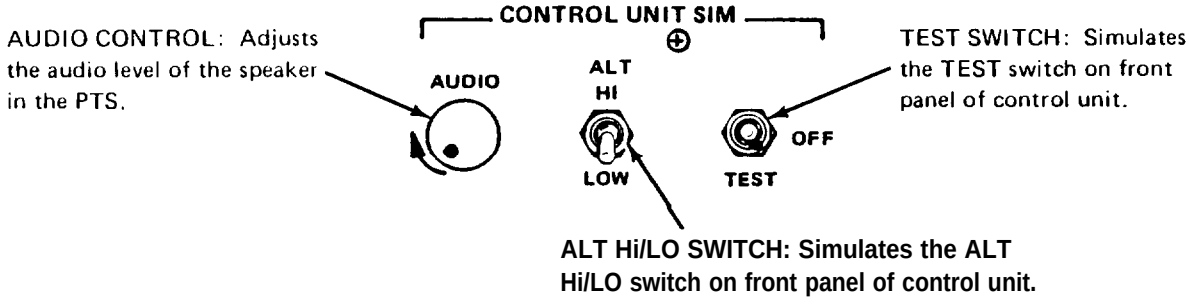
UUT POWER FIELD

3-12. The UUT power field permits you to apply +28 Vdc power to the processor unit (UUT). The function of the field item is provided below.



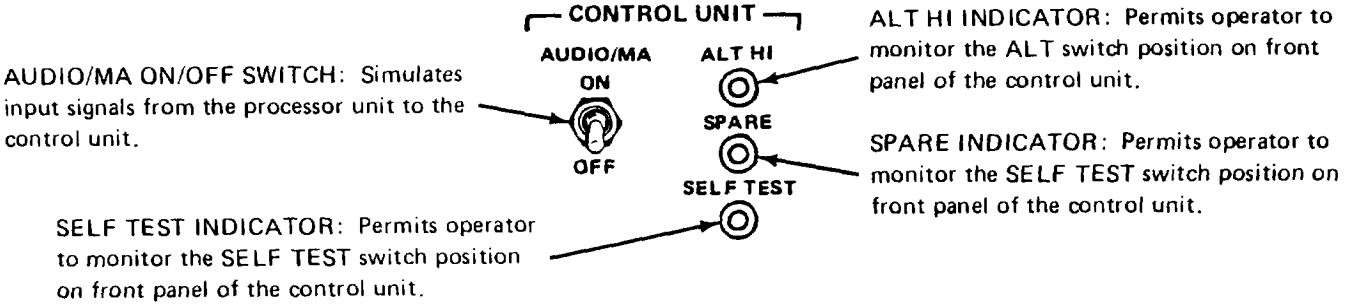
CONTROL UNIT SIM FIELD

3-13. The control unit SIM field permits you to simulate the front panel controls of the control unit. The function of each field item is provided below.



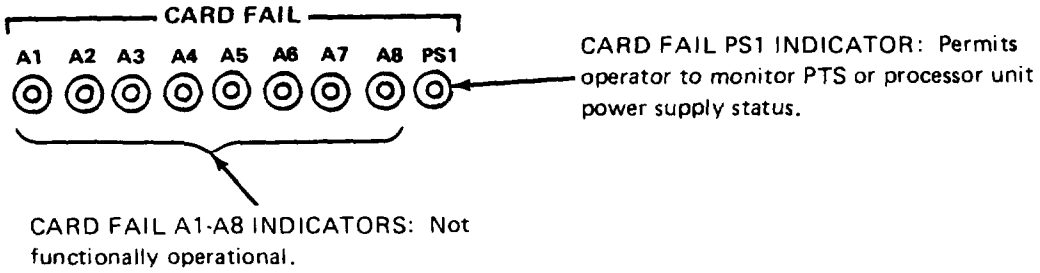
CONTROL UNIT FIELD

3-14. The control unit field permits you to simulate processor unit inputs to the control unit and permits you to monitor specific control unit responses. The function of each field is provided below.



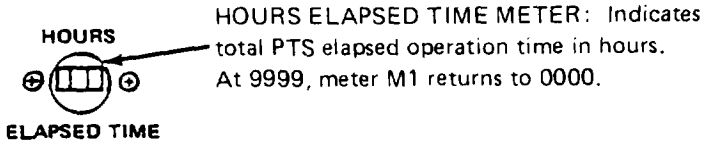
CARD FAIL FIELD

3-15. The card fail field is not functionally operational, but does provide you with an indication of PTS or processor unit power supply failure. The function of each field item is provided below.



ELAPSED TIME FIELD

3-16. The elapsed time field provides you with an indication of total PTS operational time. The function of the field item is provided below.



SECTION II
OPERATION UNDER USUAL CONDITIONS

SETUP FOR OPERATION

3-17. Open the processor test set case and remove all test set cables from inside the top cover. Also remove the two cassette assemblies from inside the top cover. Position the PTS on a suitable work surface along with the six test set cables and the two cassette assemblies. Each of the following paragraphs describe PTS setup operations you will be performing as called for in the electrical check procedures of Chapter 4, Section IV. Perform these PTS setup paragraphs ONLY when the electrical check procedures instruct you to do so. During the performance of these electrical check procedures, acknowledgement/completion messages or error messages may occur. The following list is provided to give you an understanding of these type messages.

AVUM/AVIM PTS ACKNOWLEDGEMENT/COMPLETION MESSAGES

Code	Definition
F00	This message appears after the RESET switch is pressed at the PTS and indicates that the PTS is initialized and is operationally ready.
F02	Acknowledge message for a rewind tape request.
F03	Acknowledge message: indicates that a valid test or comma number was entered.
F04	Acknowledgement for PTS self test request.
F06	The processor under test (PUT) diagnostics were successfully transferred to the cassette tape.

Code	Definition
FOC	The data in the PUT PROM's compare well to the data on the cassette, or the data in the PTS PROM's properly matches the data on the cassette tape, or the memory of the PUT or the PTS yielded the expected checksum, or the PROM's on the memory board have been successfully programmed or a successful transfer of data from the AMPL FS990 to the PTS cassette data storage has taken place.
FOD	Signifies that data is being written from the PTS memory to the cassette data tape.
FOE	Success message indicating that the PUT's CPU diagnostics have been correctly executed.
FOF	Success message indicating the end of a write to tape operation.
F1O	A prompt. The operator is requested to enter the first part (most significant) of the checksum word.
F11	A prompt. The operator is requested to enter the second part (LSB) of the checksum word.

AVUM/AVIM ERROR MESSAGES

Code	Definition
E0O	Cassette not loaded. Cassette related operation is aborted.
E01	Can not stop tape motion.
E02	Invalid command number entered.
E03	Invalid test number entered (see also E09).
E04	The memory contents of the PUT do not match the data on the cassette.
E05	Checksum error on a PTS or PUT memory read.
E06	Can not find an EOT (end of tape) mark.
E07	Data does not compare: tape to memory.
E08	Failure on transfer of diagnostics from PTS to PUT.
E09	Invalid test number entered (see also E03).
EOB	No response from PUT on a HOLD request. The EXTMEM DRV$ signal did not respond.

Code	Definition
EOC	No request from PUT on a HOLD request. The EXTADD DRV$ signal is not responding.
EOD	The PUT's CPU diagnostics failed.

NOTE

Error messages E50 through E94 pertain to and are generated during PTS self test.

E50	The PTS hardware which generates the FORWARD RIGHT video signal is defective.
E51	FORWARD LEFT hardware is defective.
E52	AFT LEFT hardware is defective.
E53	AFT RIGHT hardware is defective.
E54	Error detected in the control unit interface hardware.
E55	Defective PTS control unit switch simulator (A8 board).
E56	Band select hardware defect.
E57	Band select hardware defect.
E58	Digital signal processor 64-bit shift register error.

NOTE

Error messages E59 through E67 are generated when the digital signal processor (A3) board in the PTS does not contain fifteen 4-bit groups of alternating 1's and 0's.

E59	1 among first four zeros.
E5A	O among second four ones.
E5B	1 among second four zeros.
E5C	O among third four ones.
E5D	1 among third four zeros.
E5E	O among fourth four ones.
E5F	1 among fourth four zeros.
E60	O among fifth four ones.
E61	1 among fifth four zeros.

Code	Definition
E62	0 among sixth four ones.
E63	1 among sixth four zeros.
E64	0 among seventh four ones.
E65	1 among seventh four zeros.
E66	0 among eighth four ones.
E67	1 among eighth four zeros.
E68	Digital signal processor error.

NOTE

Error messages E69 through E77 are similar to error messages E59 through E67, except that a different multiplexer is used to channel the input signal to-the 64-bit shift register of the digital signal processor (A3) board in the PTS.

E69	1 among first four zeros.
E6A	0 among second four ones.
E6B	1 among second four zeros.
E6C	0 among third four ones.
E6D	1 among third four zeros.
E6E	0 among fourth four ones.
E6F	1 among fourth four zeros.
E70	1 among sixth four zeros.
E74	0 among seventh four ones.
E75	1 among seventh four zeros.
E76	0 among eighth four ones.
E77	1 among eighth four zeros.
E78	Digital signal processor shift register error.

NOTE

The last note applies here too, only a third multiplexer is used.

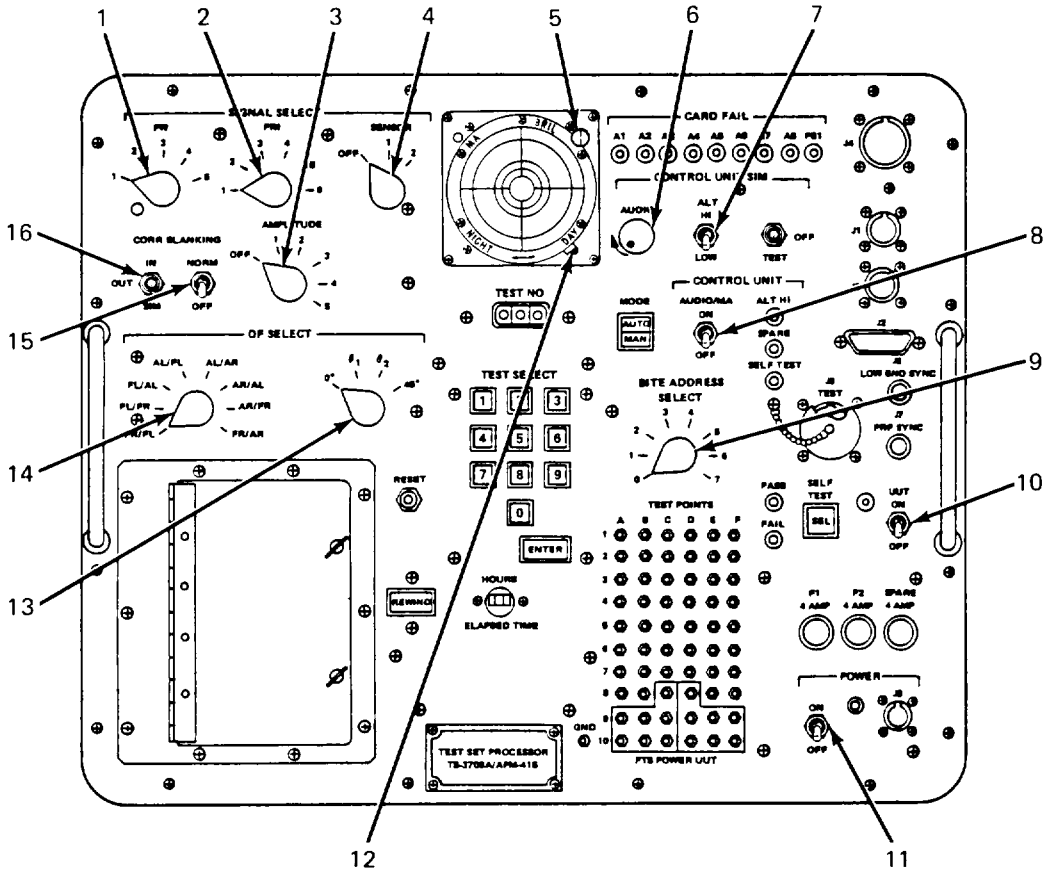
E79	1 among first four zeros.

Code	Definition
E7A	0 among second four ones.
E7B	1 among second four zeros.
E7C	0 among third four ones.
E7D	1 among third four zeros.
E7E	0 among fourth four ones.
E7F	1 among fourth four zeros.
E80	0 among fifth four ones.
E81	1 among fifth four zeros.
E82	0 among sixth four ones.
E83	1 among sixth four zeros.
E84	0 among seventh four ones.
E85	1 among seventh four zeros.
E86	0 among eighth four ones.
E87	1 among eighth four zeros.
E89	Defect in U18 of A5 board (CRU input MUX).
E8A	Defect in U19 of A5 board (CRU input MUX).
E8B	Defect in U17 of A5 board (CRU input MUX).
E8C	Defect in U20 of A5 board (CRU input MUX).
E8D	Defect in U18 of A5 board (CRU input MUX).
E8E	Defect in U19 of A5 board (CRU input MUX).
E8F	Defect in U17 of A5 board (CRU input MUX).
E90	Defect in U20 of A5 board (CRU input MUX).
E91	PUT data register of PTS is defective.
E92	PUT address register of PTS is defective.
E93	PUT data register of PTS is defective.
E94	PUT address register of PTS is defective.

INITIAL CONTROL SETTINGS

3-18. This paragraph provides you with the instructions required for setting the controls and switches of the PTS to their proper positions before power is applied to the PTS.

Set the controls and switches of the PTS to the positions stated below:

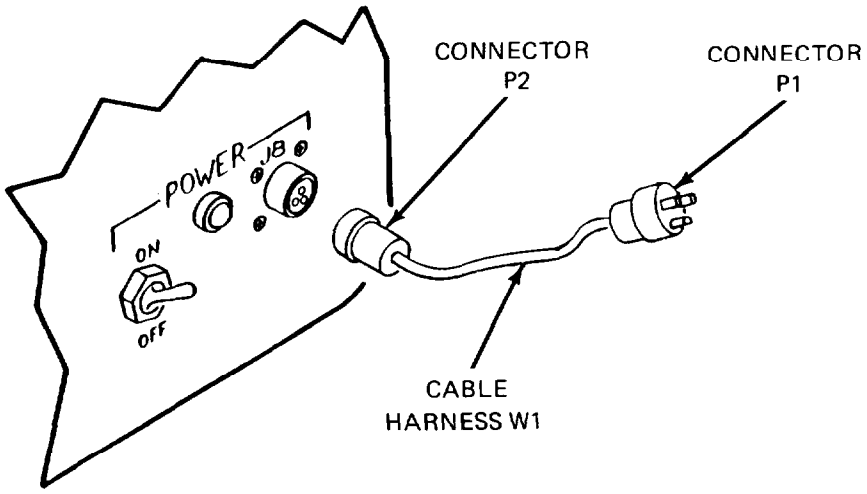


- 1. SIGNAL SELECT PW switch to 1.
- 2. SIGNAL SELECT PRI switch to 1.
- 3. SIGNAL SELECT AMPLITUDE switch to OFF.
- 4. SIGNAL SELECT SENSOR switch to OFF.
- 5. BRIL control to mid-point of its travel.
- 6. CONTROL UNIT SIM AUDIO control to maximum counter-clockwise position.
- 7. CONTROL UNIT SIM ALT switch to LOW.
- 8. CONTROL UNIT AUDIO/MA switch to OFF.
- 9. BITE ADDRESS SELECT switch to 0.
- 10. UUT switch to OFF.
- 11. POWER switch to OFF.
- 12. Filter control as desired.
- 13. DF SELECT Angle switch to 0°.
- 14. DF SELECT Octant switch to FR/FL.
- 15. BLANKING switch to OFF.
- 16. CORR switch to OUT.

PTS TO FACILITY POWER CONNECTIONS

3-19. This paragraph provides you with instructions for connecting the PTS to facility power.

1 Connect cable harness W1 connector P2 to PTS connector J8.



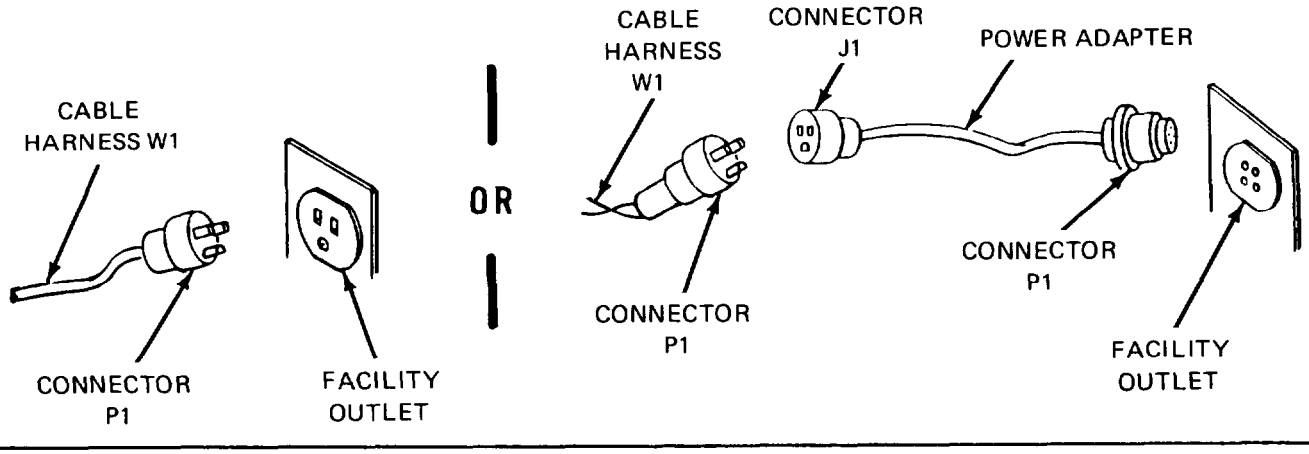
N O T E

The type of available facility power (115 Vat, 50/60 Hz or 115 Vat, 400 Hz) determines which procedure in step 2 (A or B) is performed. Perform only one of these procedures.

2 Connect PTS to facility power by ONE of the following methods -

A If facility power is 115 Vac 50/60 Hz, connect cable harness W1 connector P1 to power outlet.

B If facility is 115 VAC, 400 Hz, connect cable harness W1 connector P1 to power adapter connector J1 and power adapter connector P1 to facility outlet.



PTS TO PROCESSOR UNIT CABLE HARNESS CONNECTIONS

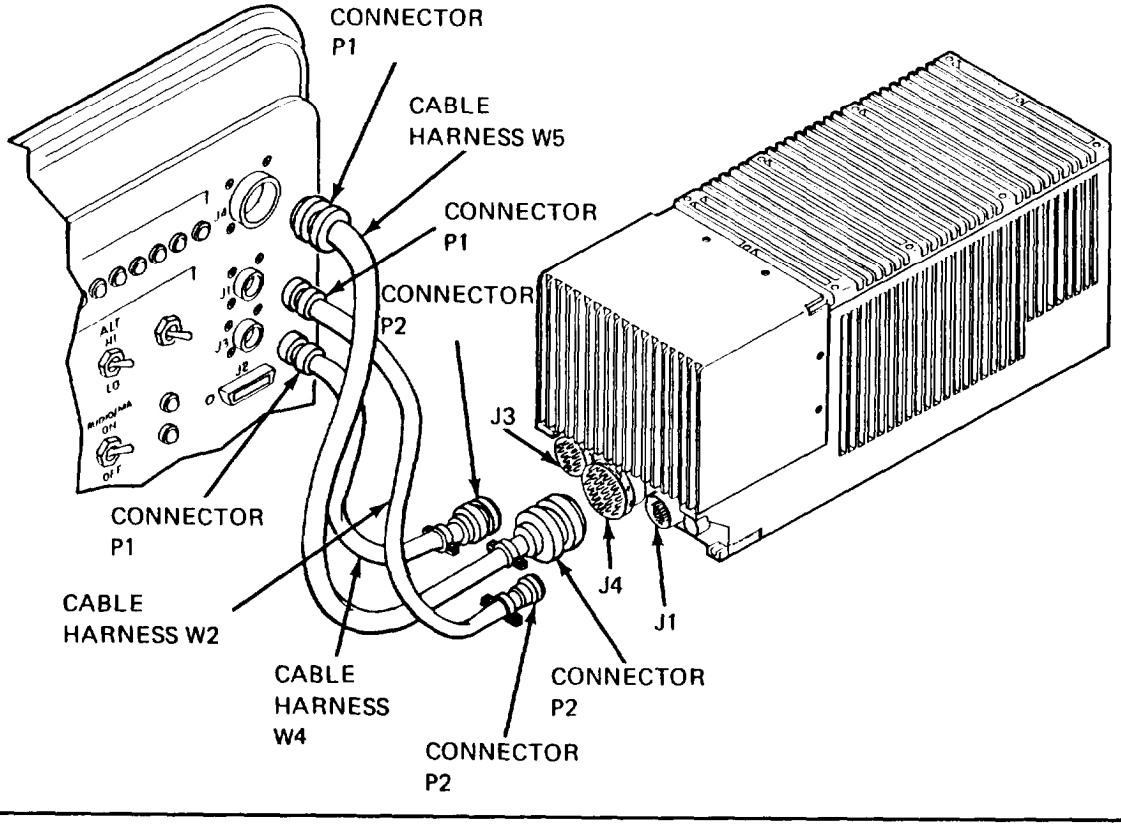
3-20. This paragraph provides you with instructions for connecting the processor unit to the PTS.

CAUTION

Do not connect both the processor unit and the control unit to the PTS at the same time. All three units can be damaged when you turn power on at the PTS.

Connect the cable harness connectors as follows:

- Cable harness W2 connector P2 to processor unit connector J1.
- Cable harness W2 connector P1 to PTS connector J1.
- Cable harness W4 connector P2 to processor unit connector J3.
- Cable harness W4 connector P1 to PTS connector J3.
- Cable harness W5 connector P2 to processor unit connector J4.
- Cable harness W5 connector P1 to PTS connector J4.



PTS TO CONTROL UNIT CABLE HARNESS CONNECTIONS

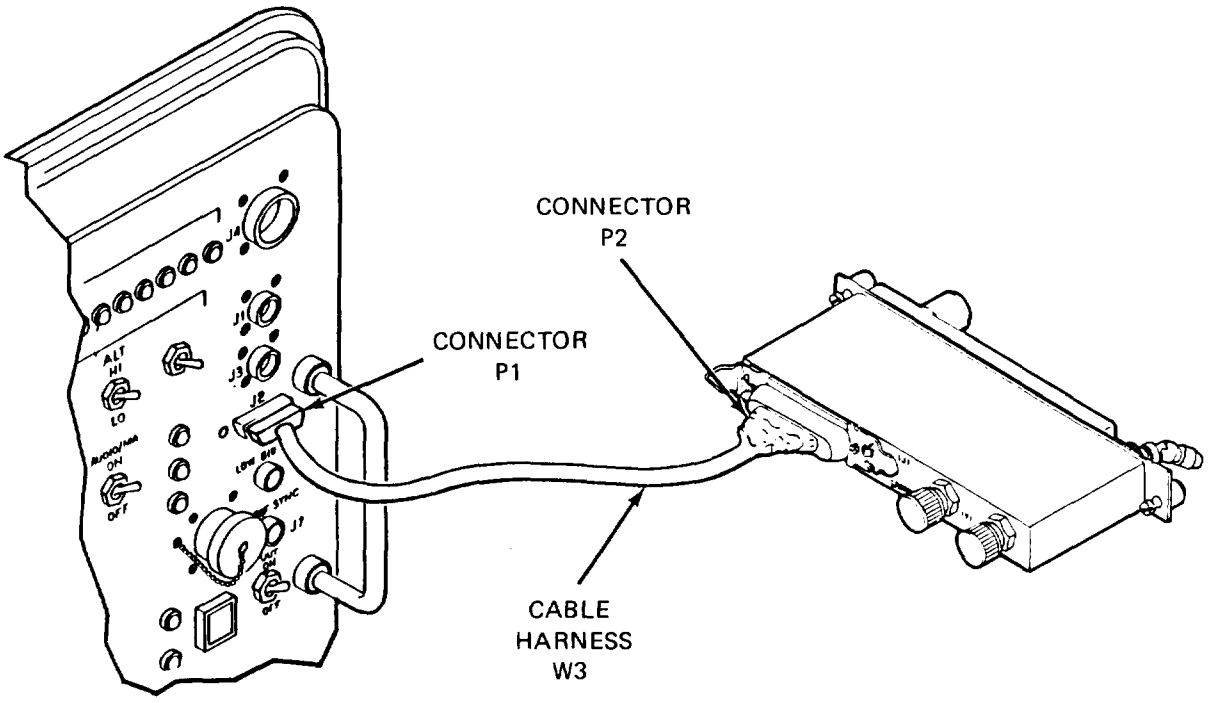
3-21. This paragraph provides you with instructions for connecting the control unit to the PTS.

CAUTION

Do not connect both the control unit and the processor unit to the PTS at the same time. All three units can be damaged when you turn power on at the PTS.

Connect the cable harness connectors as follows:

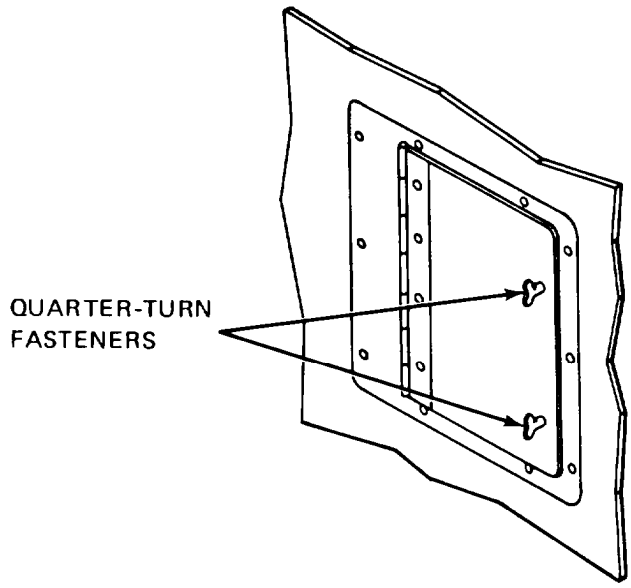
- Connect cable harness W3 connector P1 to PTS connector J2.
- Connect cable harness W3 connector P2 to control unit connector J1.



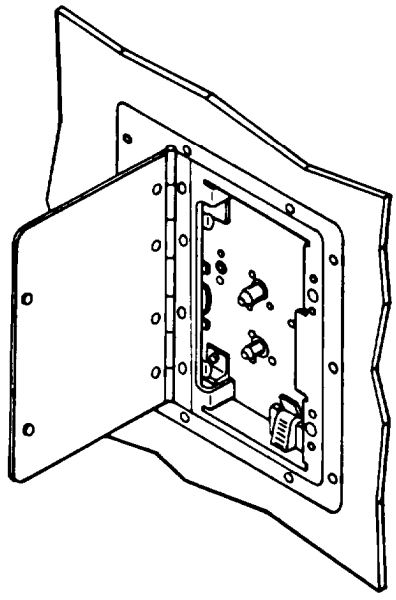
CASSETTE LOADING PROCEDURE

3-22. This paragraph provides you with instructions for loading a cassette into the PTS MTCT.

1 Twist quarter-turn fasteners to the open position.



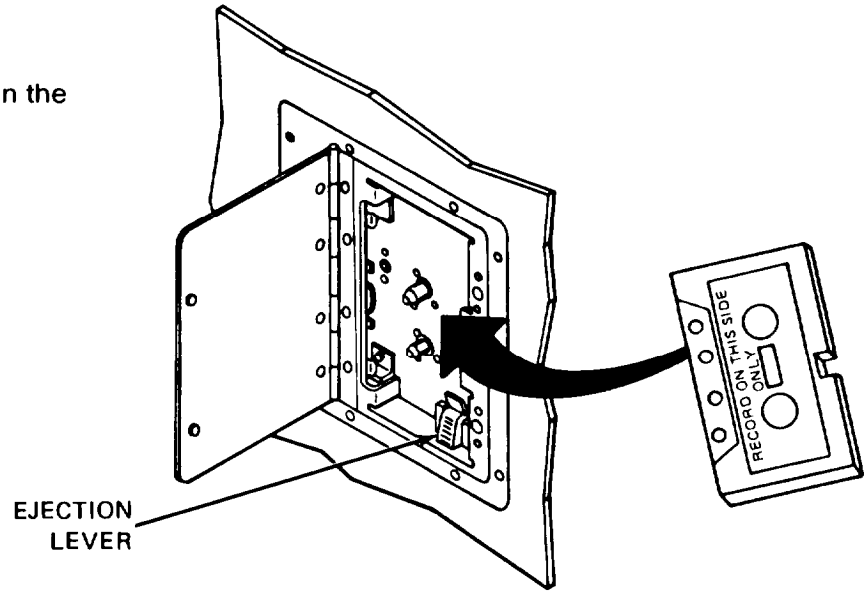
2 Open MTCT door.



3 Insert cassette into MTCT with side of cassette marked RECORD ON THIS SIDE ONLY facing outwards.

NOTE

Leave MTCT door in the open position.



CASSETTE REMOVAL PROCEDURE

3-23. This paragraph provides you with instructions for removing a cassette from the PTS MTCT.

1 Twist quarter-turn fasteners to the open position and open MTCT door.

2 Remove cassette from MTCT by depressing ejection lever.

3 Close MTCT door and twist quarter-turn fasteners to the closed position.

EXTERNAL POWER SUPPLY TO PTS CONNECTIONS

3-24. This paragraph provides you with instructions for connecting an external power supply to the PTS.

1 With power supply set to off, jumper a wire between the negative output (DC-) and ground (G) on the power supply.

2 Connect a wire to the positive output (DC+) of the power supply.

3 Connect a wire to the ground output of the power supply.

CAUTION

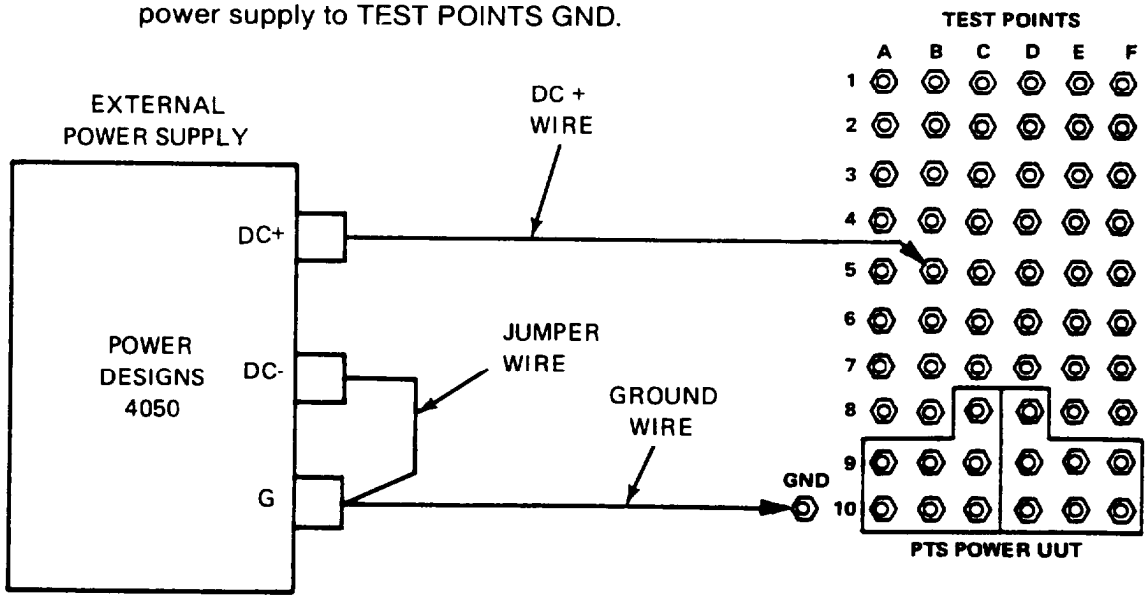
Do not let the DC+ and ground wires touch during the performance of step 4; damage to the power supply may result.

4 Set power supply to on and adjust power supply output to 0 Vdc.

5 Set power supply to off.

6 Connect the power supply to the PTS TEST POINTS as follows:

- Connect the DC+ wire from the power supply to TEST POINTS B5.
- Connect the ground wire from the power supply to TEST POINTS GND.



SECTION III

OPERATION UNDER UNUSUAL CONDITIONS

SECTION CONTENTS PAGE

GENERAL

3-25. When you are located in an area where some feature of the climate - such as heat, humidity, or cold - is abnormal, you will have to change your operating procedures. In addition to performing normal maintenance, you must protect the processor test set and perform services more often to keep the processor test set in top operating condition.

LOW/HIGH TEMPERATURE OPERATION

3-26. The PTS will operate normally between 0°C and 55°C. If the PTS is to be operated outside this temperature range, the electrical check procedures involving the Magnetic Tape Cassette Transport (MTCT) or the 162 Interface test may not function properly.

EXTREME DUST AND SAND OPERATION

3-27. During extreme dust and sand operation, perform your Preventive Maintenance Checks and Services more often than scheduled. Remove sand and dust with a vacuum cleaner and a brush. When you are not using the PTS, keep the case closed.

CHAPTER 4

MAINTENANCE

SECTION I
INTRODUCTION

GENERAL

4-1. This chapter provides you with the instructions for maintaining the processor test set at the intermediate (AVUM) and (AVIM) level of maintenance. By performing these procedures, as contained in the following sections, you will be able to maintain the processor test set in a proper operating state.

TOOLS AND EQUIPMENT

4-2. The tools and equipment required to maintain the processor test set are listed in appendix B.

LUBRICATION

4-3. The processor test set does not require any lubrication.

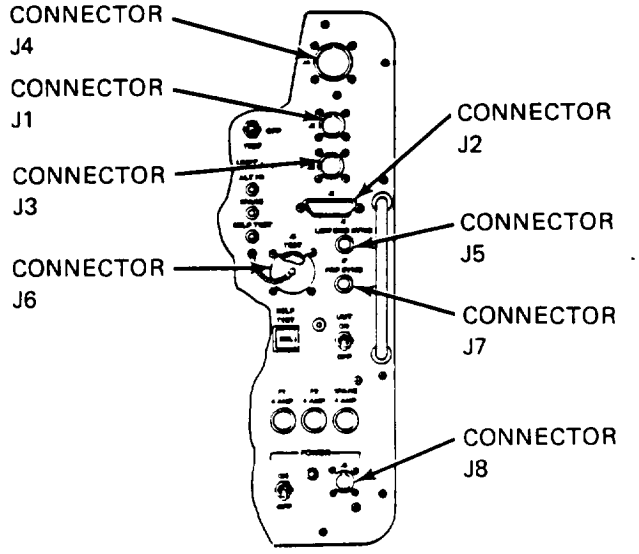
INSPECTION

4-4. As a technician, you're often working with the processor test set. Therefore, you should be alert for signs of damage, such as cracks, chipped paint, loose, bent or pushed in pins of connectors, stripped, worn or corroded wiring, knobs and switches that do not rotate smoothly, signs of overheating, shorting, or other obvious damage. Your care and alertness in repairing these defects or reporting them to your supervisor will help keep the processor test set in top operating condition.

GENERAL CLEANING

4-5. Keeping your equipment clean is one of the most important maintenance functions that you perform. Proper cleaning is necessary to keep the processor test set in A-1 shape and should be a part of your daily routine. The following general cleaning procedure should be performed.

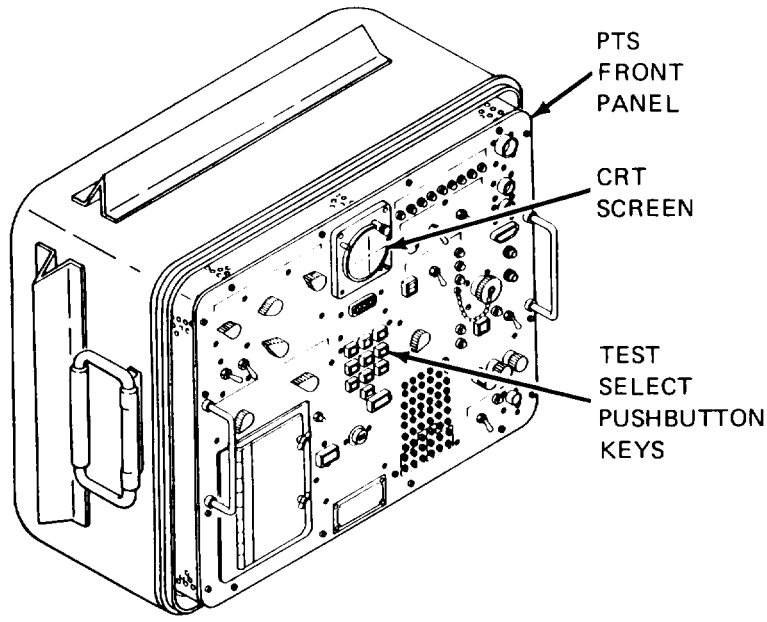
1 Using a soft bristle brush, clean out any dust or dirt from connectors J1 thru J8.



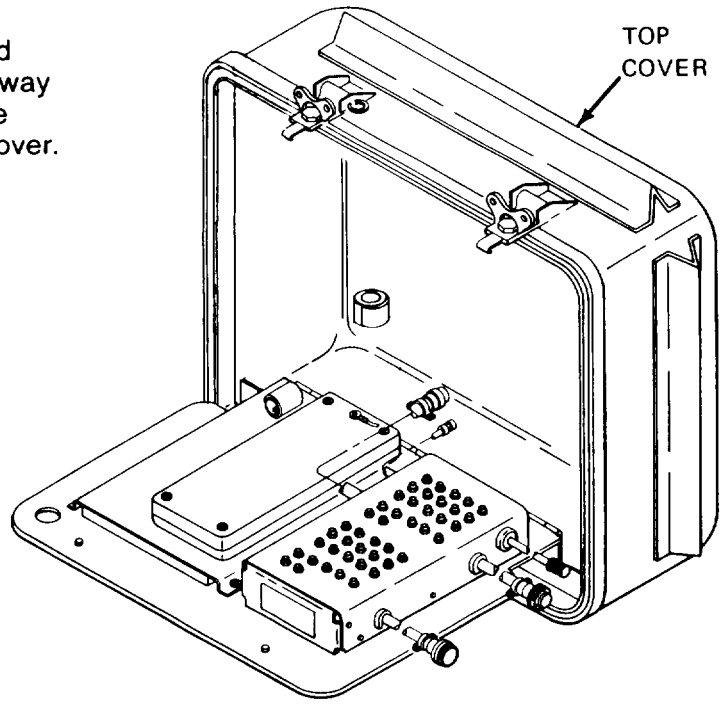
CAUTION

For step 2, do not clean CRT screen or TEST SELECT pushbutton keys with isopropyl alcohol.

2 Using a lint-free cloth and isopropyl alcohol, wipe away ground-in dirt and grease on the PTS front panel.



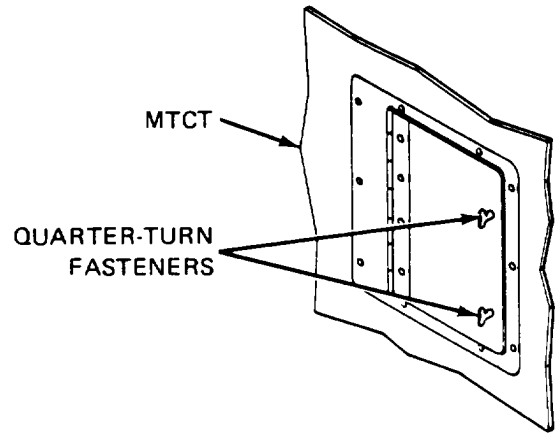
3 Using a lint-free cloth and isopropyl alcohol, wipe away ground-in dirt and grease inside test set case top cover.



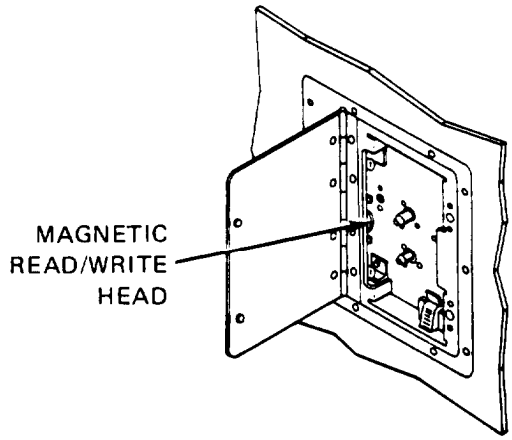
MTCT CLEANING

4-6. Cleaning the magnetic read/write head and other parts of the MTCT which come in contact with the cassette tape is a MUST. Otherwise, oxide build-up on these parts can cause incorrect loading of information into the PTS during the performance of the electrical check procedures section IV of this chapter. As referenced in the preventive maintenance checks and services of section III, perform the following cleaning procedure after each 8 hour operational period of MTCT use.

1 Twist the quarter-turn fasteners of the MTCT to the open position.



2 Open the MTCT door to gain access to the magnetic read/write head and other parts which require cleaning.

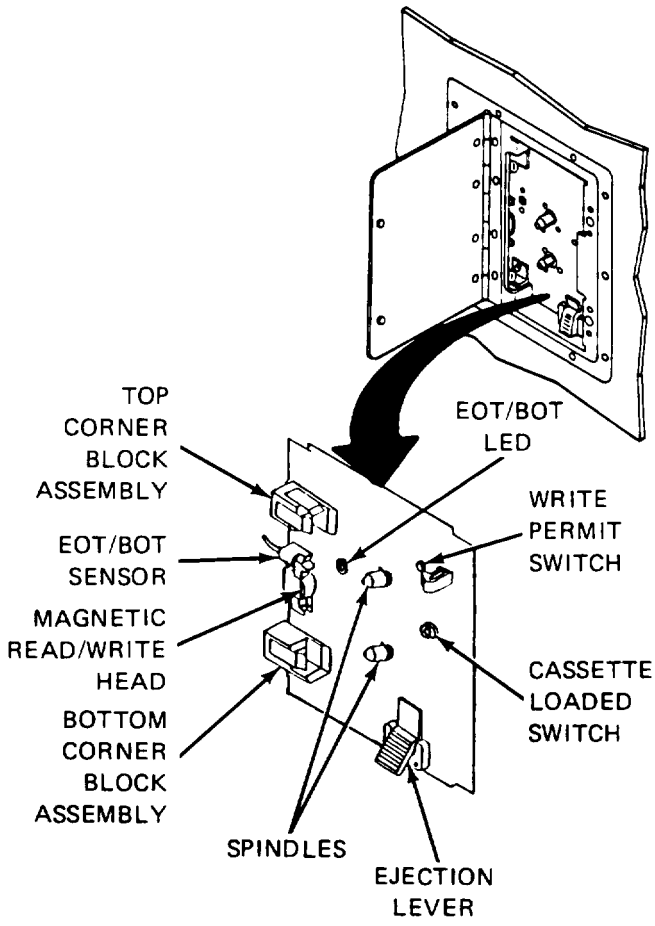


WARNING

Do not use acetone, chlorinated, or aromatic hydrocarbons. These type cleaning agents will attack the adhesives used in the magnetic read/write head and plastic parts of the MTCT.

3 Using either a brand name cleaner, freon, or isopropyl alcohol and an ordinary hygienic cotton-tipped swab applicator, clean the following parts of the MTCT:

- magnetic read/write head
- inside of top and bottom corner block assemblies
- EOT/BOT sensor
- EOT/BOT light emitting diode (LED)
- spindles
- write permit switch
- cassette loaded switch
- underside of ejection lever



4 Using a LINT-FREE cloth, wipe away excess cleaning solution from all parts of the MTCT.

WARNING

Do not use MTCT until cleaning solution has completely dried.

5 Visually inspect magnetic read/write head to assure that there is no residue left on the head after cleaning.

PAINTING

4-7. If minor touch-up painting is required, refer to TB 43-0118 (Field Instructions for Painting and Preserving Electronics Command Equipment) for correct cleaning and refinishing practices.

EXPENDABLE SUPPLIES AND MATERIALS

4-8. Refer to appendix D for a listing of supplies and consumable materials.

SECTION II

SERVICE UPON RECEIPT

SECTION CONTENTS PAGE

UNPACKING

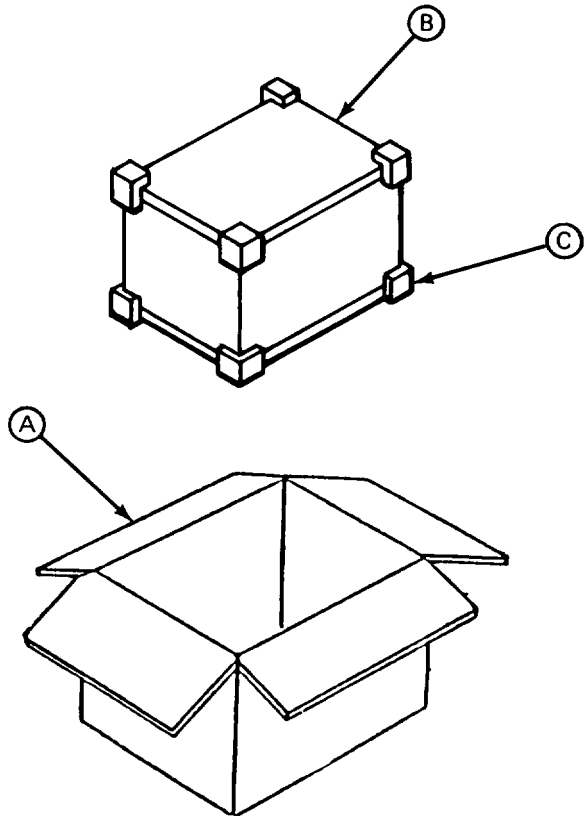
4-9. The following procedure provides you with the instructions required to unpack the complete Processor Test Set AN/AP M-415A. Once you have unpacked the processor test set, check the equipment according to paragraph 4-10. Refer to paragraph 1-8 of Chapter 1 for a description of the major items contained in the processor test set. After all major items have been checked, store the complete Processor Test Set AN/APM-415A in a secure area only. To unpack the processor test set, proceed as follows:

1

A Cut the sealing tape along the top of the fiberboard box and open the flaps.

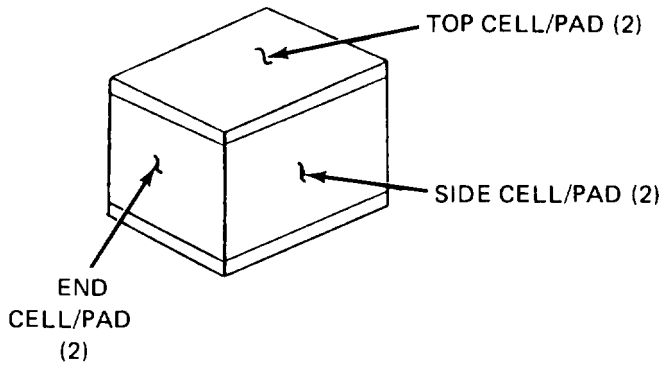
B Remove the cushioning package containing the processor test set.

C Remove the eight fiberboard corner pads.



2

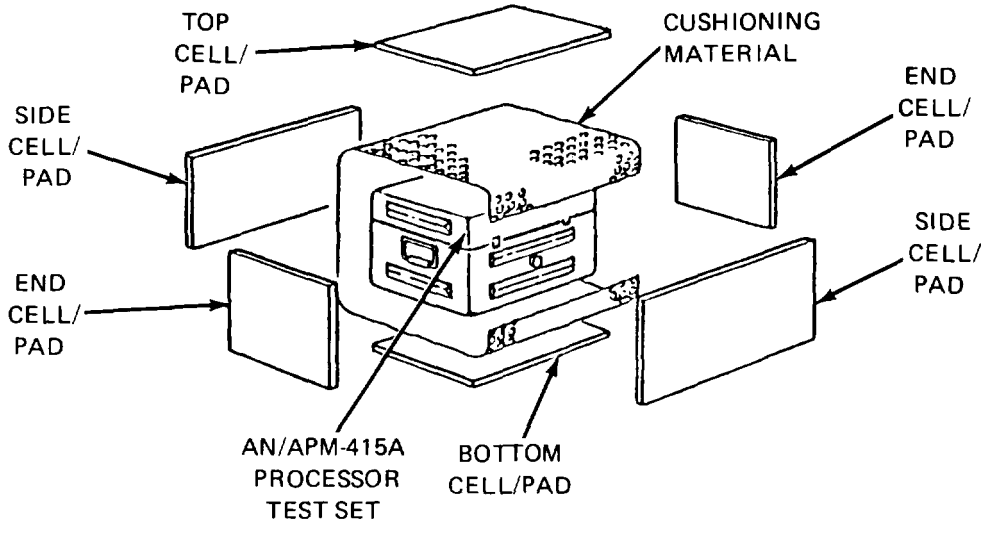
Cut the tape securing cell/pads together.



CAUTION

Lifting of the processor test set requires two men.

3 Remove the two side cell/pads, two end cell/pads, and the top cell/pad. Lift the processor test set off of the bottom ceil pad and remove cushioning material.



4 Place the cushioning material and all eight cell/pads along with the eight fiberboard corner pads inside the fiberboard box, and store the box in a secure area for future use.

CHECKING UNPACKED EQUIPMENT

4-10. Inspect the major items of the processor test set for damage incurred during shipment. Refer to Chapter 1, Section II, paragraph 1-8 for a definition of major items. If any item has been damaged, report the damage on SF 361, Discrepancy in Shipment Report (DISREP).

Check each major item against the packing slip to determine if the shipment is complete. Report all discrepancies in accordance with the instructions provided in DA PAM 738-750.

Check whether any major item has been modified (items which have been modified will have the MWO number on the front panel of the PTS (TS-3706A/APM-415), near the nomenclature plate). Also check whether all currently applicable MWO'S have been applied. Current MWO'S applicable to each major item are listed in DA Pam 310-1.

SECTION III

PREVENTIVE MAINTENANCE CHECKS AND SERVICES

SECTION CONTENTS PAGE

GENERAL

4-11. The Preventive Maintenance Checks and Services (PMCS) are an easy way to find and correct faults before they cause serious damage to the processor test set. To make sure that the processor test set is in good working order before operation, perform at the PMCS procedures listed in the charts of paragraph 4-14.

Before you begin the PMCS procedures, REMEMBER:

1. Before each processor test set operation, perform PMCS (paragraph 4-14) to be sure that the equipment is ready to go.

2. Always remember the PMCS cautions and warnings.

3. If your processor test set fails to operate, record the problem on DA Form 2404 and notify Intermediate Maintenance as soon as possible. (See sample DA Form 2404 on next page.)

4. Routine maintenance tasks such as cleaning, dusting, checking for frayed or loose cables, covering unused connectors, storing items not in use, checking for loose nuts and bolts, etc. are not scheduled on a periodic basis and should be accomplished anytime the AVUM or AVIM technician sees that they must be done.

BASIC PMCS INFORMATION

4-12. These procedures assume that the processor test set is properly shut down. Be careful in areas where voltage may exist. If at any point in the procedures you cannot perform an operation, do not proceed to subsequent steps before maintenance has corrected the problem. If you cannot perform the required maintenance or corrective action, notify Intermediate Maintenance immediately.

DA FORM 2404, EQUIPMENT INSPECTION AND MAINTENANCE WORKSHEET

EQUIPMENT INSPECTION AND MAINTENANCE WORKSHEET

For use of this form, see TM 38-750; the proponent agency is the Office of the Deputy Chief of Staff for Logistics.

1. ORGANIZATION	2. NOMENCLATURE AND MODEL
2ND SIGNAL BRIGADE	PROCESSOR TEST SET AN/APM-415A

3. REGISTRATION/SERIAL/FSN	4a. MILES	b. HOURS	c. ROUNDS FIRED	d. HOT STARTS	5. DATE	6. TYPE INSPECTION
					13 JUN	PMCS

7. APPLICABLE REFERENCE

TM NUMBER	TM DATE	TM NUMBER	TM DATE
TM 11-6625-2940-14			

INSTRUCTIONS - Perform each check listed in the TM applicable to the inspection performed. Following the sequence listed in pertinent TM, complete form as follows:

COLUMN a - Enter TM item number.

COLUMN b - Enter the applicable condition status symbol.

COLUMN c - Enter deficiencies and shortcomings.

COLUMN d - Show corrective action for deficiency or shortcoming listed in Column c.

COLUMN e - Individual ascertaining completed corrective action initial in this column.

ALL INSPECTIONS AND EQUIPMENT CONDITIONS RECORDED ON THIS FORM HAVE BEEN DETERMINED IN ACCORDANCE WITH DIAGNOSTIC PROCEDURES AND STANDARDS IN THE TM CITED HEREON.

8a. SIGNATURE (Person(s) performing inspection)	8b. TIME	9a. SIGNATURE (Maintenance Supervisor)	9b. TIME	10. MANHOURS REQUIRED
David Franklin	0930 HOURS			

TM ITEM NO. a	STATUS b	DEFICIENCIES AND SHORTCOMINGS c	CORRECTIVE ACTION d	INITIAL WHEN CORRECTED e
2	B	BRT CONTROL LOOSE	TIGHTENED CONTROL	DWF

USE PMCS ITEM NO.

DA FORM 1 JAN 64 2404

COLUMN ENTRIES USED IN PMCS TABLES

4-13. Each of the column entries used in the PMCS tables is explained below.

1) Column 1, ITEM NO. - numbers and checks and services to be performed in order. This column is also used as a source of item numbers on DA Form 2404.

2) Column 2, INTERVAL - tells you when each PMCS item should be performed.

B = Before Operation H = Operational Hours W = Weekly

3) Column 3, ITEM TO BE INSPECTED PROCEDURE - identifies which part of the processor test set is to be inspected and the procedure to follow.

4) Column 4, FOR READINESS REPORTING EQUIPMENT IS NOT READY/AVAILABLE IF: contains a brief description of the procedure by which the check is to be performed, and the results expected.

PMCS PROCEDURES

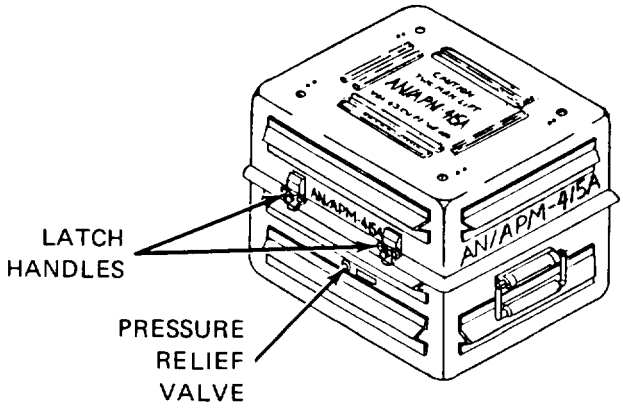
4-14. The following pages contain PMCS tables. Please read them carefully and follow the directions “to the letter”. REMEMBER, if you reach a point where the result obtained does not agree with the expected result, refer to section V of this chapter for related troubleshooting procedures.

WARNING

HIGH VOLTAGE is present in the equipment.
Use proper precautions when operating.

Inspect all exterior surfaces of the processor test set case for cracks, strains or deformities.

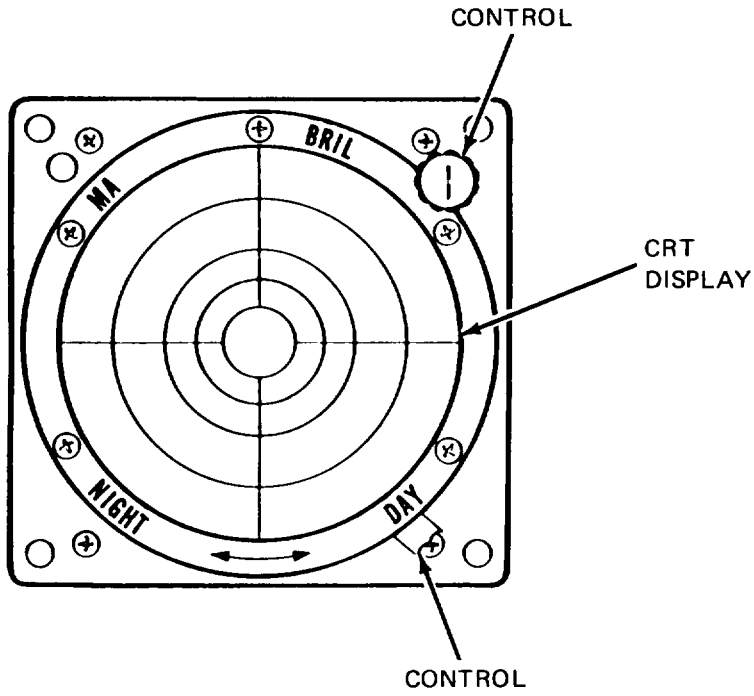
Check latch handles and pressure relief valve for binding and tightness.



Inspect the PTS front panel for cracks and scratches. Clean PTS front panel in accordance with paragraph 4-5.

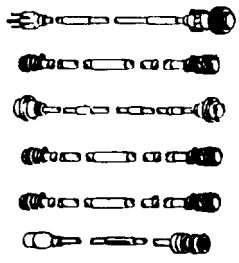
Check action of all switches and controls on PTS front panel for smooth response without looseness, binding or backlash.

Check action of controls on PTS radar signal indicator for smooth response without looseness, binding or backlash.



Inspect PTS radar signal indicator CRT display for scratches. Clean face of CRT display with a lint-free cloth.

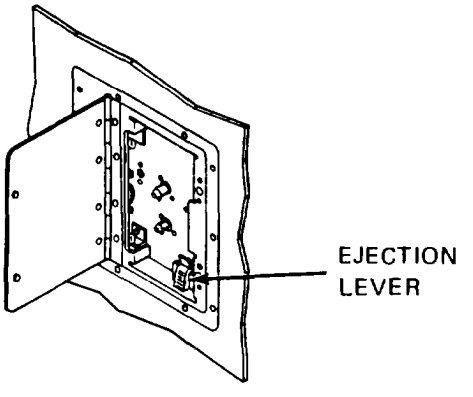
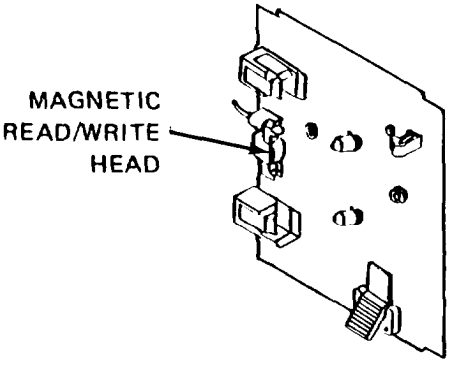
Verify that all six PTS cables are present and that the pins of each connector is not broken, bent or missing.



W1 (C5079649)
W2 (C5079588)
w3 (C5079589)
W4 (C5079590)
W5 (C5079591)
SM-C-933053

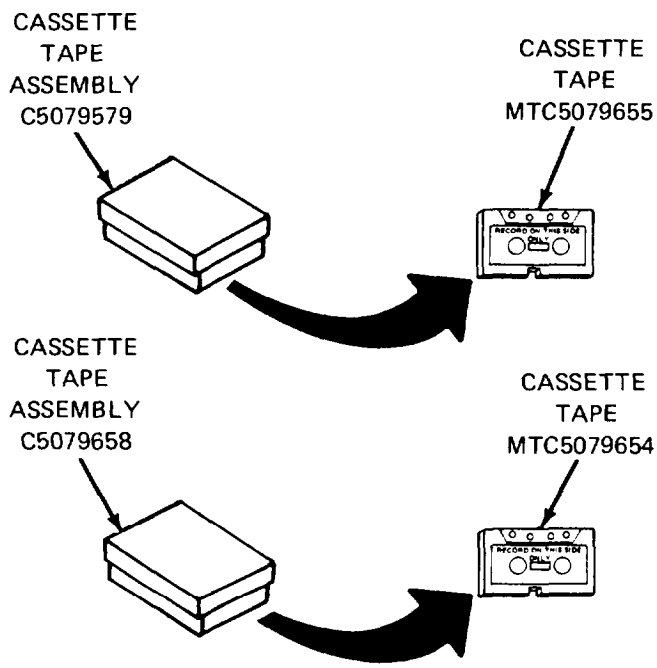
PREVENTIVE MAINTENANCE CHECKS AND SERVICES
PMCS PROCEDURES

B = Before Operation H = Operational Hours W = Weekly

ITEM NO.	INTERVAL B	INTERVAL H	INTERVAL W	ITEM TO BE INSPECTED PROCEDURE	FOR READINESS REPORTING EQUIPMENT IS NOT READY/AVAILABLE IF:
				NOTE BE ALERT. If you find a fault which you can fix, fix it. Check out anything that seems wrong or unusal.	
1.	•			MTCT Ejection Lever. Check action of MTCT ejection lever for smooth response without binding.  	Ejection lever is defective.
2.		•		MTCT Magnetic Read/Write Head. Inspect MTCT magnetic read/write head cleanliness. Clean head in accordance with paragraph 4-6.  	Head must be cleaned.

PREVENTIVE MAINTENANCE CHECKS AND SERVICES
PMCS PROCEDURES (Continued)

B = Before Operation H = Operational Hours W = Weekly

ITEM NO.	INTERVAL B	H	W	ITEM TO BE INSPECTED PROCEDURE	FOR READINESS REPORTING EQUIPMENT IS NOT READY/AVAILABLE IF:
3.	•			PTS Cassette Tape Assemblies. Verify that two cassette tape assemblies are present and that each assembly contains a magnetic cassette tape. Inspect each tape for smooth operation and that each tape is not broken. 	Cassette assembly missing or cassette tape is broken.
4.			•	PTS Electrical Check Procedures. Perform the electrical check procedures contained in Section IV of this chapter. If a failure occurs, refer to Section V (troubleshooting procedures).	Specific step no. and paragraph no. of Section IV cannot be performed successfully.

SECTION IV
ELECTRICAL CHECK PROCEDURES

SECTION CONTENTS — PAGE

GENERAL

4-15. This section contains the electrical check procedures for the PTS. Use of these procedures enables you to determine PTS operational status. If, when performing these procedures, a specified CHECK step cannot be obtained, a malfunction exists. Refer to Section V (troubleshooting) to find out what you should do to correct the malfunction. Once the troubleshooting procedure has isolated the malfunction to a suspected component, refer to Section Vl (maintenance) for the suspected component removal and subsequent installation of a new component. When all of the procedural steps of the electrical check procedures can be performed without necessitating the use of Section V, the PTS has met minimum performance standards and is considered functionally operational.

NOTE

Unless otherwise stated, all controls, switches and indicators mentioned within the electrical check procedures are contained on the PTS.

Should a failure occur while you are performing a specific step of the PTS electrical check procedures, refer to the TROUBLESHOOTING SEQUENCE provided in Section V of this chapter. It is IMPORTANT that all troubleshooting be accomplished FOLLOWING THIS TROUBLESHOOTING SEQUENCE. Failure to do so can result in your incorrectly identifying the defective components.

PTS POWER ON TEST

4-16. This paragraph provides you with the instructions required to check that the PTS can be successfully powered up and initialized. Perform the PTS to facility power connections of chapter 3, section II, paragraph 3-19.

1 Record the ELSPAED TIME of the PTS in hours on a piece of paper.

2 Set PTS POWER ON/OFF switch to ON.

3 **CHECK** that the PTS POWER indicator is lit.

4 **CHECK** that the cooling fan is operating by listening for the sound of the

5 Observe the status of the SELF TEST SEL pushbutton switch: if the SEL lamp is lit, press the SELF TEST SEL pushbutton switch and proceed to step 6; if the SEL lamp is not lit, proceed to step 7.

6 **CHECK** that the SEL lamp is not lit.

7 Observe the status of the AUTO/MAN MODE pushbutton switch: if the AUTO lamp is lit, depress the AUTO/MAN MODE pushbutton switch and proceed to step 8; if the MAN lamp is lit, proceed to step 9.

8 **CHECK** that the AUTO lamp is not lit and that the MAN lamp is lit.

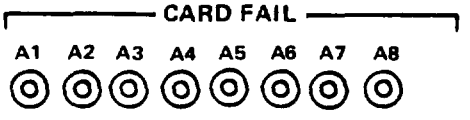
9 Press the RESET pushbutton switch.

10 After approximately 3 seconds, **CHECK** that the CARD FAIL PSI indicator is lit.

11 **CHECK** that the TEST NO indicator displays FOO.

12 **CHECK** that the CONTROL UNIT ALT HI indicator is lit.

13 **CHECK** that ail other CARD FAIL indicators are not lit.



SELF TEST

4-17. This paragraph provides you with the instructions required to check the self test circuits of the PTS.

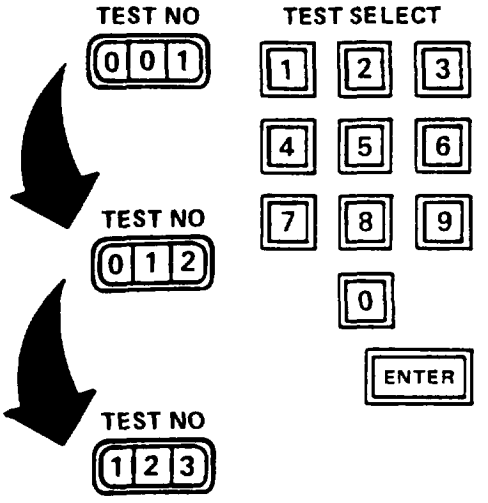
NOTE

During the performance of this self test procedure, ONLY concern yourself with the indications (requirements) shown in each check step. DISREGARD all other PTS front panel indications that may occur which are not shown as part of each check step.

1 Sequentially press TEST SELECT pushbutton keys 1 through 9, and then press pushbutton key 0, two consecutive times.

CHECK that - as each key is pressed, the digit of the depressed key is displayed on the right side of the TEST NO indicator.

- as each key is pressed, the two rightmost digits are shifted to the left.

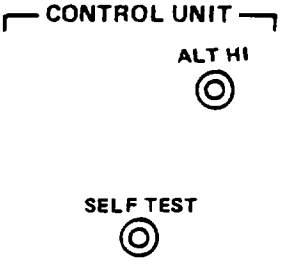


2 Press the SELF TEST SEL pushbutton switch and **CHECK** that the SEL lamp lights.

3 Press the SELF TEST SEL pushbutton switch and **CHECK** that the SEL lamp goes

4 Press the SELF TEST SEL pushbutton switch and **CHECK** that - the CONTROL UNIT ALT HI indicator first goes off, then relights, and then goes out.

- the CONTROL UNIT SELF TEST indicator lights after the CONTROL UNIT ALT HI indicator goes out.



NOTE

If either of these two lamps fail to operate properly, check the TEST NO indicator for presence of an error message. If error message is displayed, refer to troubleshooting index (Para 4-30) for step 5. If no error message is displayed, refer to troubleshooting cross-reference index for step 4.

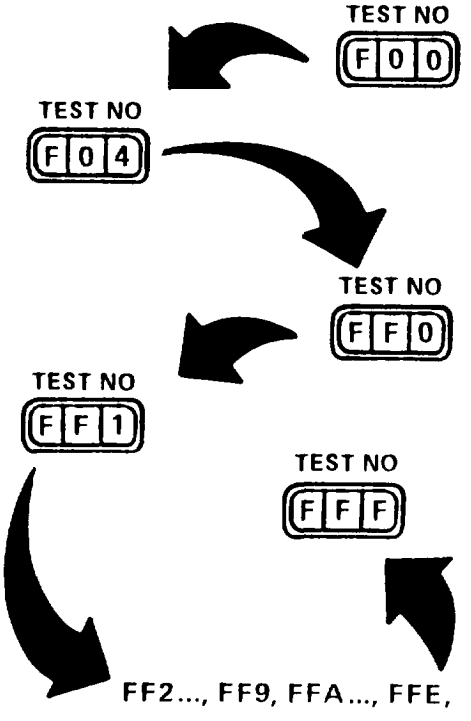
NOTE

The successful completion of step 5 requires that you understand the type of messages that can be displayed on the TEST NO indicator. This indicator provides two types of messages: error messages and acknowledgement/completion messages. Error messages are defined by an E followed by a two digit code. Acknowledgement/completion messages are defined by an F followed by a two digit code.

5 Press the RESET pushbutton switch and **CHECK** that - the TEST NO indicator momentarily displays F00, then F04, then FFO, then increments from FF1 to FFF.

as the TEST NO indicator is displaying these type acknowledgement/completion messages, no error messages are displayed.

the CONTROL UNIT SELF TEST indicator goes out when the TEST NO indicator displays FFF.



6 Press the RESET pushbutton switch and **CHECK** that - the PASS indicator flashes on and off as the TEST NO indicator goes from F04 to FFE.

- the FAIL indicator does not light as the TEST NO indicator goes from F04 to FFE.

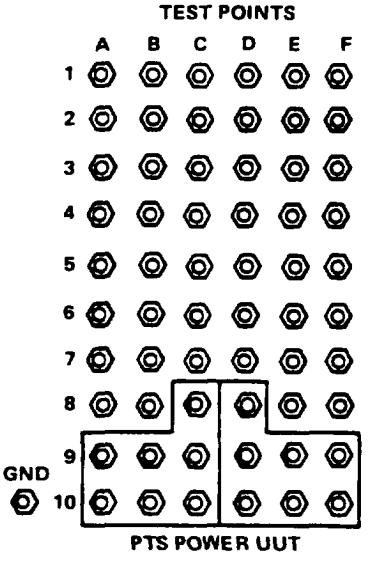
7 **CHECK** that the CARD FAIL PSI indicator flickers (dimly lit).

8 Press the RESET pushbutton switch and after the TEST NO indicator displays FFF, **CHECK** that the following indicators light simultaneously and then go out approximately 5 seconds later.

- CARD FAIL indicators A1 thru A8
- CONTROL UNIT indicator ALT HI
- CONTROL UNIT indicator SPARE
- SELF TEST indicator PASS
- SELF TEST indicator FAIL

9 Connect the oscilloscope to TEST POINTS F4. Then set oscilloscope controls to the following:

- VOLTS/ DIV: 5
- TIM E/ DIV: 0.1 SEC
- SOURCE: CH 1
- TRIGGER MODE: NORM
- COUPLING: DC
- SLOPE: +



10 **CHECK** that the oscilloscope displays a waveform which flashes on for approximately 250 milliseconds and then off for approximately 250 milliseconds.

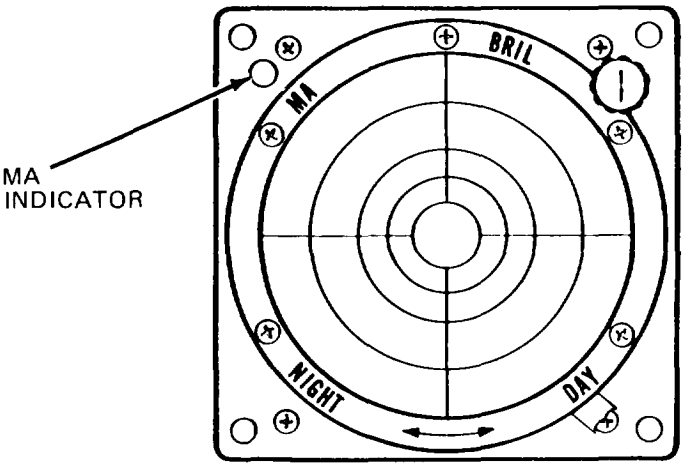
11 Set oscilloscope TIME/DIV control to 0.1 MSEC and **CHECK** that the pulse repetition interval (PRI) of the waveform is between 450 and 550 microseconds.

NOTE

Complete waveform still flashes on and off at a 500-millisecond rate.

12

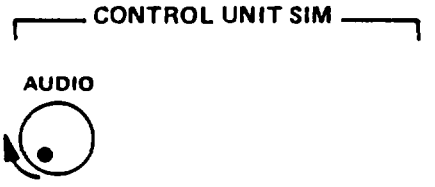
CHECK that the MA indicator of the PTS radar signal indicator flashes on and off.



13

Slowly turn the CONTROL UNIT SIM AUDIO control from the full counterclockwise position to full clockwise position and **CHECK** the following:

- that a beeping audio tone is heard.
- that the tone increases in volume as the AUDIO control is turned clockwise.

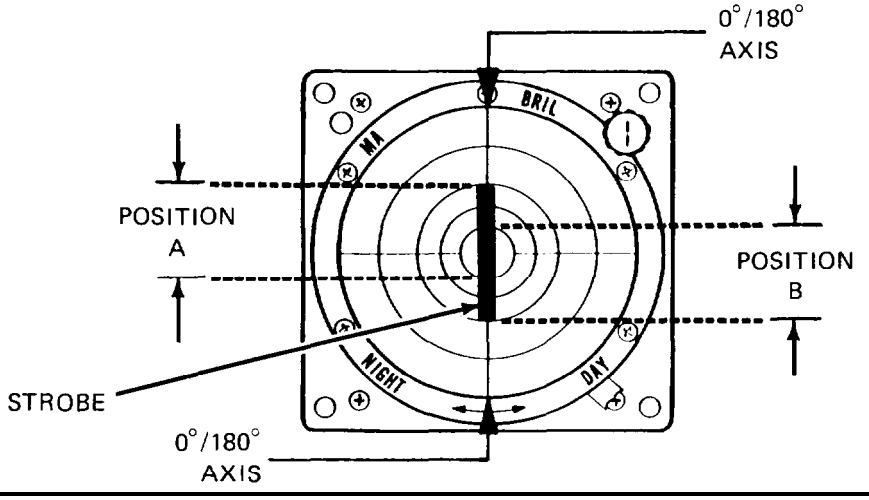


14

Turn the CONTROL UNIT SIM AUDIO control back to full counterclockwise position.

15

On the PTS radar signal indicator, **CHECK** that a strobe is displayed, which continually shifts up and down along the 0°/180° axis, approximately between position A and position B.



16

On the PTS radar signal indicator, vary the BRIL control from its present position to full clockwise position, then back to its approximate starting position and **CHECK** that the brilliance (intensity) of the display can be increased and decreased.

17

Press the SELF TEST SEL pushbutton switch and observe that the SEL lamp goes out.

18

Observe that the PTS radar signal indicator is blank.

19

Press the RESET pushbutton switch.

20

Open cassette assemblv C5079658 and insert the PTS memory verification program cassette tape MTC5079654 into the MTCT. Refer to Chapter 3, Section II, paragraph 3-22 for the cassette loading procedure.

21

Press the REWIND pushbutton switch and **CHECK** that the REWIND lamp is lit for as long as the REWIND pushbutton switch is pressed.

22

CHECK that - the TEST NO indicator displays F02.

- no error messages are displayed.

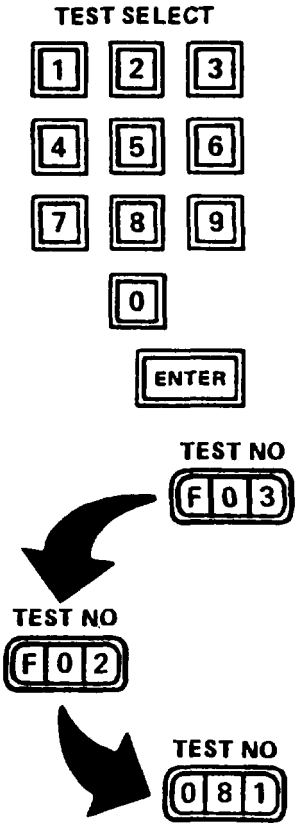
- the cassette tape rewinds and stops.

23

After the cassette tape has stopped, momentarily press, in sequence, TEST SELECT Pushbutton kevs. 0, 8, and 1. and momentarily press the EN"TER" pushbutton switch.

CHECK that - the enter lamp lights-

- the TEST NO indicator momentarily displays F03, and then F02 followed by 081.
- no error messages are displayed.
- the cassette tape moves forward.



NOTE

If for step 24, FOC is NOT displayed on TEST NO indicator within 2 minutes or E07 or E01 IS displayed, press RESET pushbutton switch and repeat steps 21 through 24. If step 24 fails a second time, proceed to section V (troubleshooting) of this chapter.

24

After approximately 2 minutes,

CHECK that - the cassette tape has stopped.

- the TEST NO indicator displays FOC.
- the TEST NO indicator does not display E07 or E01.

25 Press the REWIND pushbutton switch. After the cassette tape has stopped, remove the memory verification program cassette tape from the MTCT. Refer to Chapter 3, Section II, paragraph 3-23 for the cassette removal procedure.

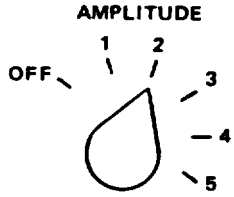
26 Place cassette tape MTC5079654 into cassette assembly C5079658 and close cover.

SIGNAL SELECT TEST

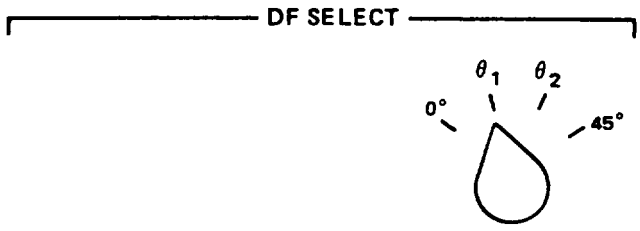
4-18. This paragraph provides you with the instructions required to check the signal generation circuits of the PTS.

1 Press the RESET pushbutton switch.

2 Set SIGNAL SELECT AMPLITUDE switch to 2.

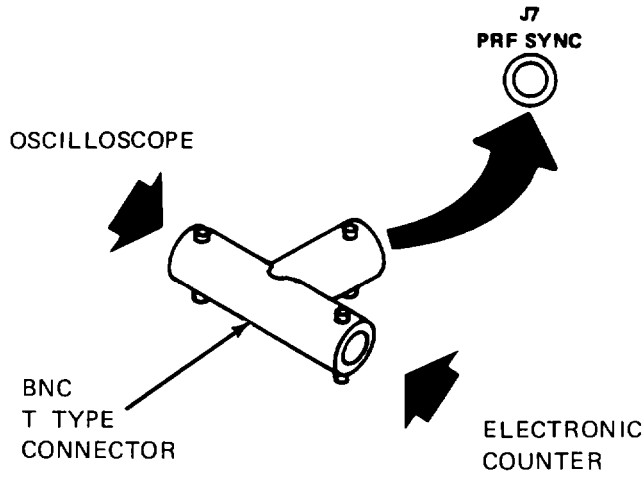


3 Set DF SELECT angle switch to Θ1.



4

Using a BNC T type connector, connect the sync input connector of the oscilloscope and the CHANNEL A INPUT A connector of the electronic counter to the PRF SYNC connector J7 on the PTS.



5

Set oscilloscope controls to the following:

- VOLTS/DIV: 0.5 (CH 1)
- TIME/DIV: 0.1 US
- SOURCE: CH 1
- TRIGGER MODE: NORM
- COUPLING: AC
- SLOPE: - (minus)
- HORIZ DISPLAY: A

6

Set the electronic counter controls to the following:

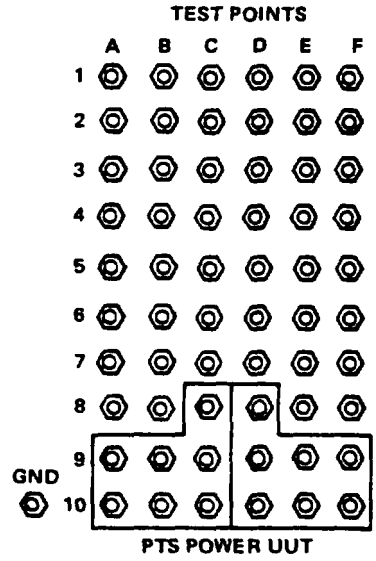
- FUNCTION: PER A
- FREQ RESOLUTION: 0.1 MHZ
- SAMPLE RATE: to mid-point of travel
- CHANNEL A LEVEL A: approximately at mid-point of travel
- CHANNEL A SLOPE: + (plus)
- CHANNEL A ATTEN: 1
- CHANNEL A AC/DC: AC

7

Using the electronic counter, **CHECK** that the Pulse Repetition Interval (PRI) at connector J7 is between 382 and 386 U seconds.

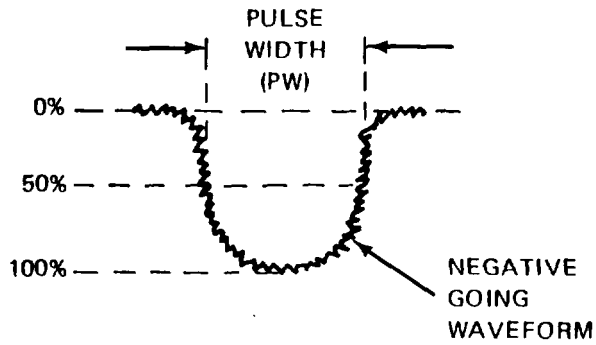
8

Connect channel 1 of the oscilloscope to TEST POINTS A4.



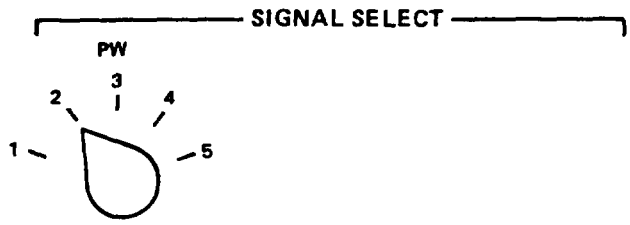
9

CHECK that the pulse width (PW) of the negative-going waveform displayed on channel 1 is between 0.45 and 0.55 U seconds at the 50% point.



10

Set the SIGNAL SELECT PW switch to 2.



11

CHECK that the PW of the negative-going waveform displayed on channel 1 is i s between 0.565 and 0.685 U seconds at the 501% point.

12

Set the SIGNAL SELECT PW switch to 3.

13 **CHECK** that the PW of the negative-going waveform displayed on channel 1 is between 0.680 and 0.820 U seconds at the 50% point.

14 Set the oscilloscope TIME/DIV control to 0.5 US.

15 Set the SIGNAL SELECT PW switch to 4.

16 **CHECK** that the PW of the negative-going waveform displayed on channel 1 is between 1.625 and 2.075 U seconds at the 50% point.

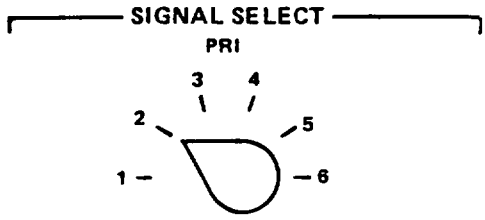
17 Set the oscilloscope TIME/DIV control to 10 US.

18 Set the SIGNAL SELECT PW switch to 5.

19 **CHECK** that the PW of the negative-going waveform displayed on channel 1 is between 43.0 and 53.0 U seconds at the 50% point.

20 Set the SIGNAL SELECT PW switch to 1.

21 Set the SIGNAL SELECT PRI switch to 2.



22 Using the electronic counter, **CHECK** that the PRI at connector J7 is between 508 and 512 U seconds.

23 Set the SIGNAL SELECT PRI switch to 3.

24 Using the electronic counter, **CHECK** that the PRI at connector J7 is between 804 and 808 U seconds.

25 Set the SIGNAL SELECT PRI switch to 4.

26 Using the electronic counter, **CHECK** that the PRI at connector J7 is between 898 and 902 U seconds.

27 Set the SIGNAL SELECT PRI switch to 5.

28 Using the electronic counter, **CHECK** that the PRI at connector J7 is between 958 and 962 U seconds.

29 Set the SIGNAL SELECT PRI switch to 6.

30 Using the electronic counter, **CHECK** that the PRI at connector J7 is between 2,908 and 2,912 U seconds.

31 Set the SIGNAL SELECT PRI switch to 1.

32 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +1.2 and +1.8 V.

33 Set the SIGNAL SELECT AMPLITUDE switch to 1.

34 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +0.4 and +0.6 V.

35 Set the SIGNAL SELECT AMPLITUDE switch to 3.

36 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +1.6 and +2.4 V.

37 Set the SIGNAL SELECT PW switch to 4.

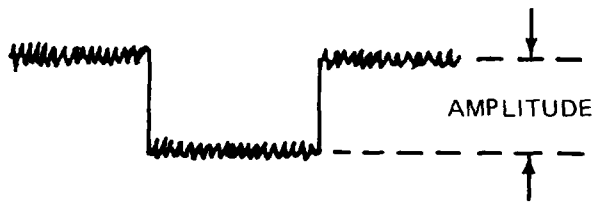
38 Set the SIGNAL SELECT AMPLITUDE switch to 5.

39 Set the oscilloscope SOURCE control to EXT, the CH 1 VOLTS/DIV control to 50 M (50 millivolts) and TIME/DIV control to 2.0 US.

40 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +148 and +188 millivolts. (read this amplitude from the center of the noise on the positive portion of the waveform to the center of the noise on the negative portion of the waveform).

41 Set the SIGNAL SELECT AMPLITUDE switch to 4.

42 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +92 and +132 millivolts (read this amplitude from the center of the noise on the positive portion of the waveform “to the center of the noise on the negative portion of the waveform).



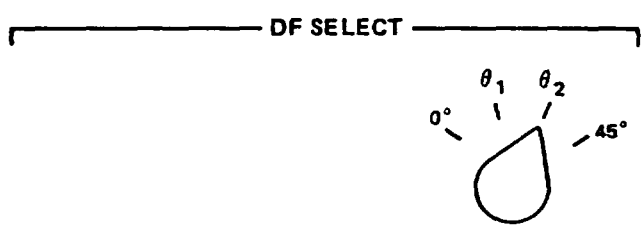
43 Set the SIGNAL SELECT AMPLITUDE switch to 2.

44 Connect channel 1 of the oscilloscope to TEST POINTS D4.

45 Set the oscilloscope CH 1 VOLTS/DIV control to 0.2.

46 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +0.6 and +0.9 V.

47 Set the DF SELECT angle switch to 02



48 **CHECK** that the amplitude of the negative-going waveform displayed on channel 1 is between +0.45 and +0.75 V.

49	Set the DF SELECT angle switch to 0°.
50	Set oscilloscope CH 1 VOLTS/ DIV control to 0.5.
51	**CHECK** that the amplitude of the negative-going waveform displayed on channel is between +1.2 and +1.8 V.
52	Set the DF SELECT angle switch to 45°.
53	Set oscilloscope CH 1 VOLTS/ DIV control to 0.1.

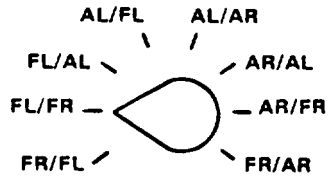
NOTE

For steps 54, 56, 58, and 61, a measurement between -0.15 and +0.1 5 is the same as a "NO WAVEFORM" condition.

54	**CHECK** that the amplitude displayed On channel 1 is between -0.15 and +0.15 V (no waveform is present).
55	Connect channel 1 of the oscilloscope to TEST POINTS B4.
56	**CHECK** that the amplitude displayed On channel 1 is between -0.15 and +0.15 V (no waveform is present).
57	Connect channel 1 of the oscilloscope to TEST POINTS C4.

58 **CHECK** that the amplitude displayed on channel 1 is between -0.15 and +0.15 V (no waveform is present).

59 Set the DF SELECT octant switch to FL/FR.



60 Connect channel 1 of the oscilloscope to TEST POINTS A4.

61 **CHECK** that the amplitude displayed on channel 1 is between -0.15 and +0.15 V (no waveform is present).

62 Set the DF SELECT angle switch to Θ 1.

63 Set oscilloscope controls to the following:

- VERT MODE: ALT
- VOLTS /DIV: 0.5 (CH 2)
- VOLTS/DIV: 0.5 (CH 1)

64 Connect channel 2 of the oscilloscope to TEST POINTS D4.

65 **CHECK** that a waveform is displayed on channel 1 of the oscilloscope.

66 **CHECK** that a waveform is displayed on channel 2 of the oscilloscope.

67	**CHECK** that the amplitude of the waveform displayed on channel 2 is greater than the amplitude of the waveform displayed on channel 1.
68	Set the DF SELECT octant switch to FL/AL.
69	Connect channel 1 of the oscilloscope to TEST POINTS C4.
70	**CHECK** that a waveform is displayed on channel 1 of the oscilloscope.
71	**CHECK** that a waveform is displayed on channel 2 of the oscilloscope.
72	**CHECK** that the amplitude of the waveform displayed on channel 2 is greater than the amplitude of the waveform displayed on channel 1.
73	Set the DF SELECT octant switch to AL/FL.
74	**CHECK** that a waveform is displayed on channel 1 of the oscilloscope,
75	**CHECK** that a waveform is displayed on channel 2 of the oscilloscope
76	**CHECK** that the amplitude of the waveform displayed on channel 1 is greater than the amplitude of the waveform displayed on channel 2.

77	Set the DF SELECT octant switch to AL/AR.
78	Connect channel 2 of the oscilloscope to TEST POINTS B4.
79	**CHECK** that a waveform is displayed on channel 1 of the oscilloscope.
80	**CHECK** that a waveform is displayed on channel 2 of the oscilloscope.
81	**CHECK** that the of the waveform displayed on channel 1 is greater than the amplitude of the waveform displayed on channel 2.
82	Set the DF SELECT octant switch to AR/AL.
83	**CHECK** that a waveform is displayed on channel 1 of the oscilloscope.
84	**CHECK** that a waveform is displayed on channel 2 of the oscilloscope.
85	**CHECK** that the amplitude of the waveform displayed on channel 2 is greater than the amplitude of the waveform displayed on channel 1.
86	Set the DF SELECT octant switch to AR/FR.
87	Connect channel 1 of the oscilloscope to TEST POINTS A4.

88 **CHECK** that a waveform is displayed On channel 1 Of the oscilloscope.

89 **CHECK** that a waveform is displayed on channel 2 of the oscilloscope.

90 **CHECK** that the amplitude of the waveform displayed on channel 2 is greater than the amplitude of the waveform displayed on channel 1.

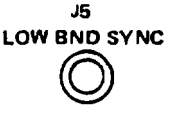
91 Set the DF SELECT octant switch to FR/AR

92 **CHECK** that a waveform is displayed on channel 1 of the oscilloscope.

93 **CHECK** that a waveform is displayed on channel 2 of the oscilloscope.

94 **CHECK** that the amplitude of the waveform displayed on channel 1 is greater than the amplitude of the waveform displayed on channel 2.

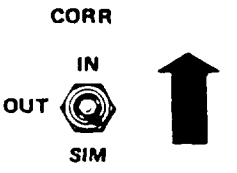
95 Using a BNC cable, connect channel 2 of the oscilloscope to LOW BAND SYNC connector J5.



96 Set oscilloscope controls to the following:

- VOLTS /DIV: 0.5 (CH 1)
- VOLTS /DIV: 5.0 (CH 2)
- TRIG MODE: NORM
- TIME/ DIV: 1.0 US
- SOURCE: CH 2
- SLOPE: + (positive)
- COUPLING: AC

97 Set the SIGNAL SELECT CORR switch to IN.



98 Set the DF SELECT angle switch to 45°.

99 **CHECK** that a waveform is displayed on channel 2 of the oscilloscope.

100 **CHECK** that the amplitude of the waveform displayed on channel 2 is between +11.0 and +15.0 V.

101 **CHECK** that the PW of the waveform displayed on channel 2 is between 1.5 and 2.5 U seconds at the 50%0 point.

NOTE

Step 102 is performed by measuring the time between the leading edge of the waveform displayed on channel 2 to the leading edge of the waveform displayed on channel 1.

102 **CHECK** that the leading edge of the waveform displayed on channel 2 occurs between 3.0 and 4.0 U seconds before the leading edge of the waveform displayed on channel 1.

103 Set oscilloscope controls to the following:

Ž VOLTS/DIV: 0.1 (CH 2)
Ž SOURCE: EXT

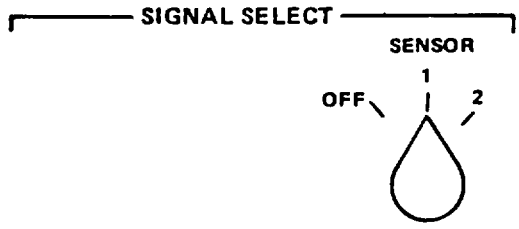
104 Set the SIGNAL SELECT CORR switch to OUT and the DF SELECT angle switch to 0°.

NOTE

For steps 105 and 123, a measurement between -0.15 and +0.15 V is the same as a "NO WAVEFORM" condition.

105 CHECK that the amplitude displayed on channel 2 is between -0.15 and +0.15 V (no waveform is present).

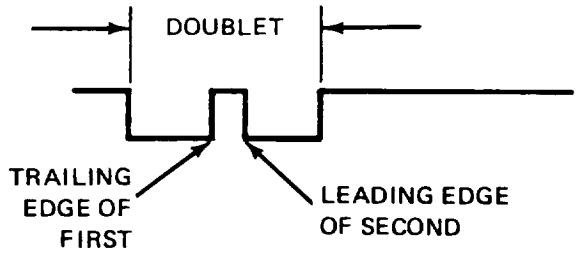
106 Set the SIGNAL SELECT SENSOR switch to 1.



107 Set oscilloscope controls to the following:

- TIME/DIV: 0.5 US
- SLOPE: - (negative)
- SOURCE: CH 1
- VERT MODE: CH 1

108 **CHECK** that the waveform displayed On channel 1 contains two negative-going pulses(doublet).



109 **CHECK** that the pulse spacing of the doublet, as measured from the trailing edge of the first pulse to the leading edge of the second pulse, is between 0.45 and 0.55 U seconds at the 50% point of the doublet.

110 Set the SIGNAL SELECT SENSOR switch to 2.

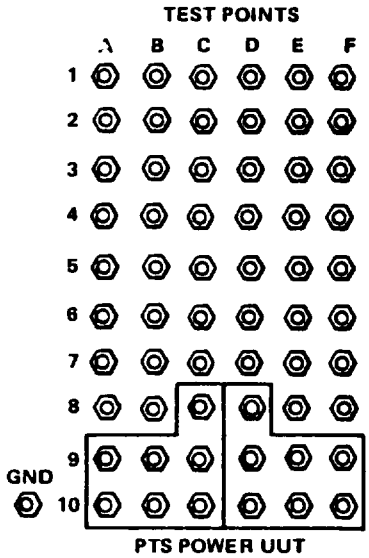
111 **CHECK** that the waveform displayed on channel 1 contains two negative-going pulses (doublet) as shown in step 108.

112 **CHECK** that the pulse spacing of the doublet, as measured from the trailing edge of the first pulse to the leading edge of the second pulse, is between 0.9 to 1.1 U seconds.

113 Set the SIGNAL SELECT SENSOR switch to OFF.

114 Set the SIGNAL SELECT BLANKING switch to NORM.

115 Disconnect channel 2 of the oscilloscope from the LOW BAND SYNC connector J5 and connect channel 2 of the oscilloscope to TEST POINTS B6.



116 Set oscilloscope controls to the following:

- VOLTS/DIV: 0.5 (CH 1)
- VOLTS/DIV: 2.0 (CH 2)
- TRIGGER MODE: NORM
- TIME/DIV: 50 US
- SOURCE: CH 2
- SLOPE: + (positive)
- COUPLING: AC
- VERT MODE: CH 2

117 **CHECK** that a waveform is displayed on channel 2 of the oscilloscope.

118 **CHECK** that the amplitude of the waveform displayed on channel 2 is between +2.8 to +5.2 V.

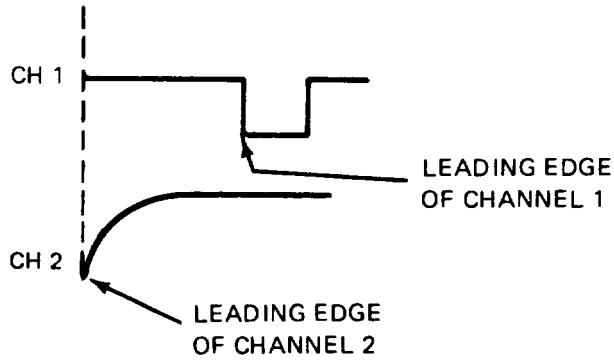
119 **CHECK** that the PW of the waveform displayed on channel 2 is between 100 and 140 U seconds at the 50% point.

120 Set oscilloscope TIME/DIV control to 1.0 US and VERT MODE control to ALT.

NOTE

Step 121 is performed by measuring the time between the leading edge of the waveform displayed on channel 2 to the leading edge of the waveform on channel 1.

121 **CHECK** that the leading edge of the waveform displayed on channel 2 occurs between 3.0 and 4.0 U seconds before the leading edge of the waveform displayed on channel 1.



122 Set the SIGNAL SELECT BLANKING switch to OFF.

Set oscilloscope controls to the following:

- VOLTS/DIV: 0.1 (CH 2)
- VERT MODE: CH 2

124 **CHECK** that the amplitude displayed on channel 2 is between -0.15 and +0.15 V (no waveform is present).

125 Disconnect the oscilloscope, electronic counter and the BNC T type connector from the PTS front panel.

BITE ADDRESS SELECT TEST

4-19. This paragraph provides you with the instructions required to check the BITE address select circuits of the PTS.

1 Set the PTS front panel controls to the following:

- SIGNAL SELECT PW switch to 1.
- SIGNAL SELECT BLANKING switch to OFF.
- SIGNAL SELECT AMPLITUDE switch to OFF.
- DF SELECT octant switch to FR/FL.
- BITE ADDRESS SELECT switch to 0.

2 Set oscilloscope controls to the following:

- VOLT/DIV: 2.0 (CH 1)
- SOURCE: NORM
- COUPLING: AC
- TRIG MODE: NORM
- VERT MODE: CH 1
- SLOPE: + (positive)
- TIME/DIV: 1.0 US

3 Press the RESET pushbutton switch.

4 Connect channel 1 of the oscilloscope to TEST POINTS D7 and the ground lead to TEST POINTS GND.

NOTE

For all following check steps, a logic low level is between 0.0 and +0.4 V, and a logic high level is between +2.4 and +5.2 V.

5 **CHECK** that channel 1 of the oscilloscope displays a logic high level.

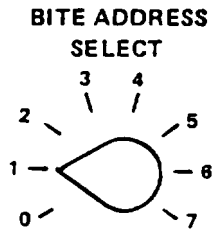
6 Connect channel 1 of the oscilloscope to TEST POINTS E7.

7 **CHECK** that channel 1 of the oscilloscope displays a logic high level.

8 Connect channel 1 of the oscilloscope to TEST POINTS F7.

9 **CHECK** that channel 1 of the oscilloscope displays a logic high level.

10 Set BITE ADDRESS SELECT switch to 1.



11	Connect channel of the oscilloscope to TEST POINTS D7.
12	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
13	Connect channel 1 of the oscilloscope to TEST POINTS E7.
14	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
15	Connect channel 1 of the oscilloscope to TEST POINTS F7.
16	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
17	Set BITE ADDRESS SELECT switch to 2.
18	Connect channel 1 of the oscilloscope to TEST POINTS D7.
19	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
20	Connect channel 1 of the oscilloscope to TEST POINTS E7.

21	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
22	Connect channel 1 of the oscilloscope to TEST POINTS F7.
23	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
24	Set BITE ADDRESS SELECT switch to 3.
25	Connect channel 1 of the oscilloscope to TEST POINTS D7.
26	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
27	Connect channel 1 of the oscilloscope to TEST POINTS E7.
28	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
29	Connect channel 1 of the oscilloscope to TEST POINTS F7.
30	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
31	Set BITE ADDRESS SELECT switch to 4.

32	Connect channel 1 of the oscilloscope to TEST POINTS D7.
33	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
34	Connect channel 1 of the oscilloscope to TEST POINTS E7.
35	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
36	Connect channel 1 of the oscilloscope to TEST POINTS F7.
37	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
38	Set BITE ADDRESS SELECT switch to 5.
39	Connect channel 1 of the oscilloscope to TEST POINTS D7.
40	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
41	Connect channel 1 of the oscilloscope to TEST POINTS E7.
42	**CHECK** that channel 1 of the oscilloscope displays a logic high level.

43	Connect channel 1 of the oscilloscope to TEST POINTS F7.
44	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
45	Set BITE ADDRESS SELECT switch to 6.
46	Connect channel 1 of the oscilloscope to TEST POINTS D7.
47	**CHECK** that channel 1 of the oscilloscope displays a logic high level.
48	Connect channel 1 of the oscilloscope to TEST POINTS E7.
49	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
50	Connect channel 1 of the oscilloscope to TEST POINTS F7.
51	**CHECK** that channel 1 of the oscilloscope displays a logic low level.
52	Set BITE ADDRESS SELECT switch to 7.
53	Connect channel 1 of the oscilloscope to TEST POINTS D7.
54	**CHECK** that channel 1 of the oscilloscope displays a logic low level.

55 Connect channel 1 of the oscilloscope to TEST POINTS E7.

56 **CHECK** that channel 1 of the oscilloscope displays a logic low level.

57 Connect channel 1 of the oscilloscope to TEST POINTS F7.

58 **CHECK** that channel 1 of the oscilloscope displays a logic low level.

59 Disconnect the oscilloscope from the PTS front panel.

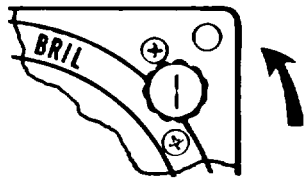
60 Set BITE ADDRESS SELECT switch to 0.

DISPLAY PROTECT TEST

4-20. This paragraph provides you the instructions required to check the display protect circuits of the PTS.

1 Turn the CONTROL UNIT SIM AUDIO control to the full counterclockwise position.

2 Set the BRIL control on the radar signal indicator to the full counterclockwise position.

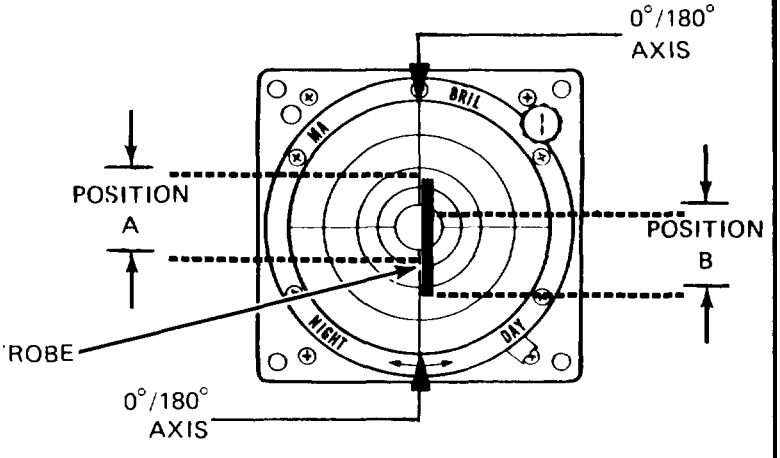


3 pushbutton switch and observe that the SEL lamp lights.

NOTE

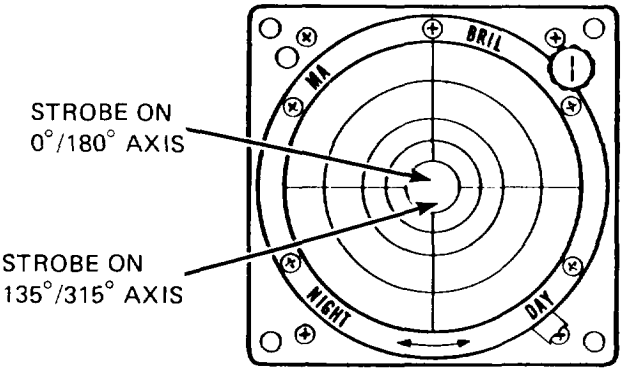
The PTS will now go through the self test routine as performed previously in paragraph 4-17. Disregard all PTS front panel indications until the TEST NO indicator displays FFF.

4 On the PTS radar signal indicator, turn the BRIL control clockwise and observe that a strobe is displayed which continually shifts up and down along the 0°/180° axis, approximately between positions A and B.



5 Perform the external power supply to PTS connections as specified in chapter 3, section II, paragraph 3-24.

6 On the radar signal indicator, observe that a strobe continually shifts back and forth between the 0°/180° axis, and the 135°/315° axis.



7 Connect a multimeter across the DC+ and G output terminals of the external supply.

8 Turn on the external power supply and SLOWLY increase the output voltage; STOP increasing the voltage when the strobe DISAPPEARS.

NOTE

The appearance of the strobe will change as the voltage is increased.

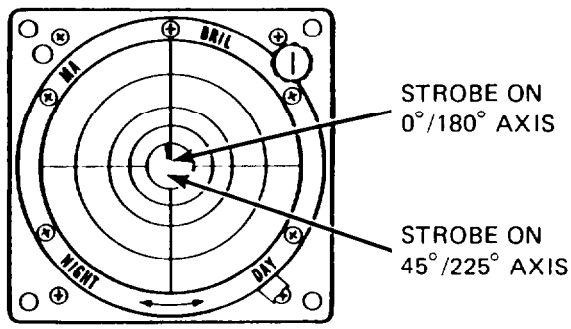
9 **CHECK** that the multimeter indicates between +1.3 V and +2.6 V.

10 Reduce the output voltage of the external power supply to zero volts and then turn off the supply.

11 Disconnect the DC+ wire from TEST POINTS B5 and press the RESET pushbutton switch to reinitiate the PTS self test routine.

12 When the TEST NO indicator displays FFF, connect the DC+ wire from the external power supply to TEST POINTS D5.

13 On the radar signal indicator, observe that a strobe continually shifts back and forth between the 0°/180° axis, and the 45°/225° axis.



14 Turn on the external power supply and SLOWLY increase the output voltage; STOP increasing the voltage when the stobe DISAPPEARS.

NOTE

The appearance of the strobe will change as the voltage is increased.

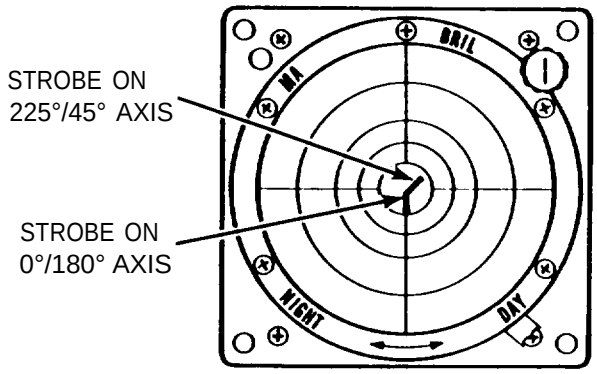
15 **CHECK** that the multimeter indicates between +1.3 V and +2.6 V.

16 Reduce the output voltage of the external power supply to zero volts and then turn off the supply.

17 Disconnect the DC+ wire from TEST POINTS D5 and press the RESET pushbutton switch to reinitiate the PTS self test routine.

18 When the TEST NO indicator displays FFF, connect the DC+ wire from the external power supply to TEST POINTS C5.

19 On the radar signal indicator, observe that a strobe continually shifts back and forth between the 0°/180° axis, and the 225°/45° axis.



20 Turn on the external power supply and SLOWLY increase the output voltage; STOP increasing the voltage when the strobe DISAPPEARS.

NOTE

The appearance of the strobe will change as the voltage is increased.

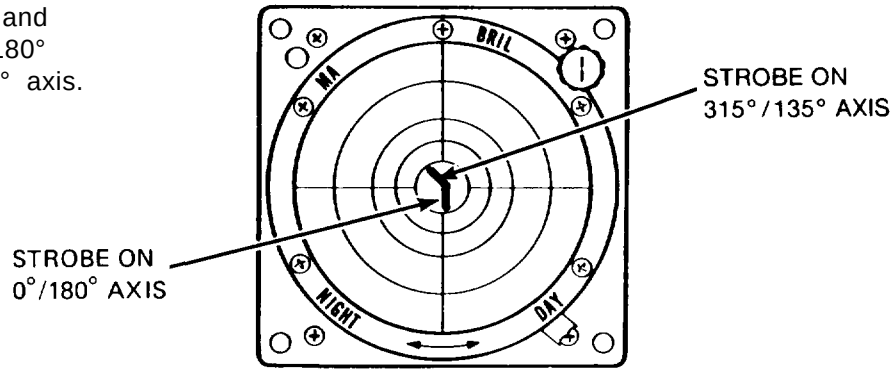
21 **CHECK** that the multimeter indicates between +1.3 V and +2.6 V.

22 Reduce the output voltage of the external power supply to zero volts and then turn off the supply.

23 Disconnect the DC+ wire from TEST POINTS C5 and press the RESET pushbutton switch to reinitiate the PTS self test routine.

24 When the TEST NO indicator displays FFF, connect the DC+ wire from the external power supply to TEST POINTS A5.

25 On the radar signal indicator, observe that a strobe continually shifts back and forth between the 0°/180° axis. and the 315°/135° axis.



26 Turn on the external power supply and SLOWLY increase the output voltage; STOP increasing the voltage when the strobe DISAPPEARS.

NOTE

The appearance of the strobe will change as the voltage is increased.

27 **CHECK** that the multimeter indicates between +1.3 V and +2.6 V.

28 Reduce the output voltage of the external power supply to zero volts and then turn off the

29 Disconnect the DC+ wire from TEST POINTS A5 and the G wire from TEST POINTS GND.

30 Disconnect the multimeter from the DC+ and G output terminals of the external power supply.

31 Press the SELF TEST SEL pushbutton switch and observe that the SEL lamp goes out.

SERIAL DATA TEST

4-21. This paragraph provides you with the instructions required to check the ALQ-162 interface circuits of the PTS.

1 Press the RESET pushbutton switch.

2 Observe that the TEST NO indictor displays F00.

3

Momentarily press, in sequence, TEST SELECT pushbutton keys, 0, 8, and 7, and then press the ENTER pushbutton switch

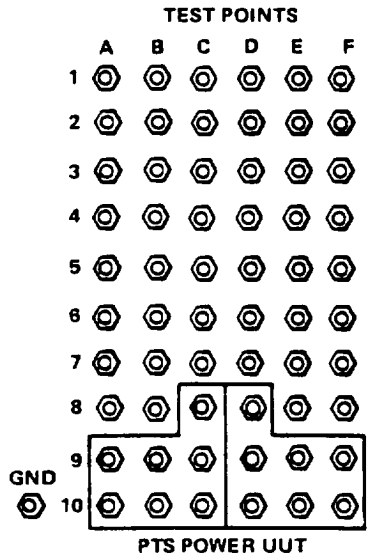
4

Observe that the TEST NO indicator momentarily displays F03, and then displays 087.

5

Connect the oscilloscope to the TEST POINTS as follows:

- connect channel 1 to TEST POINTS B1.
- connect channel 2 to TEST POINTS B2.
- ground the oscilloscope to TEST POINT GND.



6

Set oscilloscope controls to the following:

- TIME/DIV: 0.2 MSEC
- TRIG MODE: AUTO
- SLOPE: - (negative)
- SOURCE: CH 1
- VOLTS/DIV: 2.0 (CH 1)
- VOLTS/DIV: 2.0 (CH 2)
- VERT MODE: ALT
- HORIZ DISPLAY: A

NOTE

For steps 7 and 8, waveforms are asynchronous and therefore will appear to flash (on and off) on the oscilloscope.

7 **CHECK** that channel 1 of the oscilloscope displays a toggling waveform (high to low to high transitions).

8 **CHECK** that channel 2 of the oscilloscope displays a toggling waveform (low to high to low transitions).

9 Set oscilloscope controls to the following:
- VOLTS /DIV: GND (CH 1)
- VOLTS/DIV: GND (CH 2)
- VERT MODE: ADD

10 Set oscilloscope controls to the following:
- VOLTS/DIV: DC (CH 1)
- VOLTS/DIV: DC (CH 2)

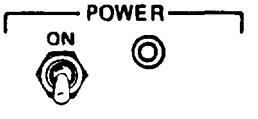
11 **CHECK** that the oscilloscope displays a constant high logic level (between 2.4 and 5.0 v).

12 Disconnect the oscilloscope from TEST POINTS B1, B2 and GND.

POWER SUPPLY MONITOR TEST

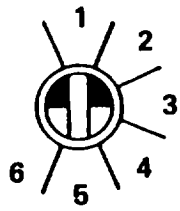
4-22. This paragraph provides you with the instructions required to check the power supply monitor circuits of the PTS. These circuits can only be checked by connecting a known working processor unit to the PTS.

1 Set the PTS POWER ON/OFF switch to OFF and observe that the POWER indicator is off.



2 Connect a known working processor unit to the PTS front panel as specified in the PTS to processor unit cable harness connections of chapter 3, section II, paragraph 3-20.

3 Set the theatre switch on the processor unit to 1.



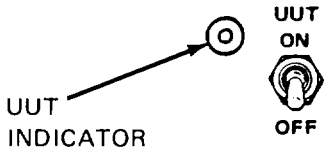
4 Set the PTS POWER ON/OFF switch to ON and observe that the POWER indictor lights.

5 Press the RESET pushbutton switch.

6 After approximately 3 seconds, **CHECK** that the CARD FAIL PS1 indicator is lit

7 Set the UUT ON/OFF switch to ON.

8 **CHECK** that the UUT indicator is lit.



9 Press the RESET pushbutton switch.

10 After approximately 3 seconds, **CHECK** that the CARD FAIL PS1 indicator is off.

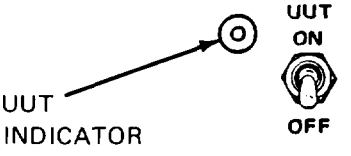
PROCESSOR INTERFACE TEST

4-23. This paragraph provides you with the instructions required to check the processor interface circuits of the PTS. These circuits can only be checked by connecting a known working processor unit to the PTS.

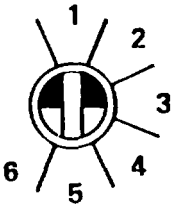
1 Connect a known working processor unit to the PTS front panel as specified in the PTS to processor unit cable harness connections of chapter 3, section II, paragraph 3-20.

2 Set the UUT ON/OFF switch to ON.

3 **CHECK** that the UUT indicator is lit.



4 Set the theatre switch on the processor unit to 1.



5 Set the PTS front panel controls to the following:

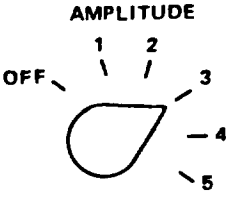
- DF SELECT octant switch to AR/AL.
- SIGNAL SELECT PRI switch to 2.
- SIGNAL SELECT CORR switch to SIM.

6 Press the RESET pushbutton switch.

7 Momentarily press, in sequence, TEST SELECT pushbutton keys 0, 7, and 9, and then momentarily press the ENTER pushbutton switch.

8 Observe that the TEST NO indicator momentarily displays F03, then displays 079.

9 Set SIGNAL SELECT AMPLITUDE switch to 3.



10 Press RESET pushbutton switch and observe that the TEST NO indicator displays F00.

11 Connect the sync input connector of the oscilloscope to the PRF SYNC connector J7 on the PTS.

12 Set oscilloscope controls to the following:

- VOLT/DIV: 0.2 (CH 1) (AC)
- SOURCE:EXT
- TIM E/ DIV: 2.0 US
- COUPLING: AC
- TRIG MODE: NORM
- VERT MODE: CH 1
- SLOPE: -(negative)

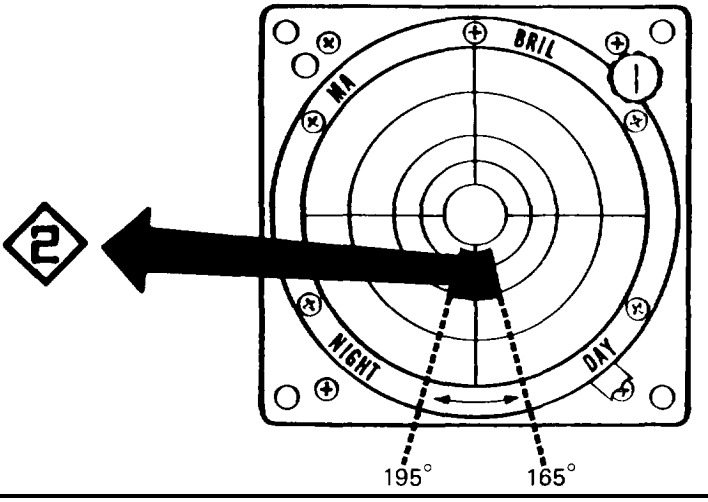
13 Connect channel 1 of the oscilloscope to TEST POINTS A2 and the ground lead to TEST POINTS GND.

14 **CHECK** that channel 1 of the oscilloscope displays a negative-going waveform whose amplitude is between 0.4 and 0.8 volt.

15 **CHECK** that the radar signal indicator displays a 2 symbol surrounded by a diamond symbol in the indicated area, between 165° and 195°. Center of 2 symbol MUST be within indicated area.

NOTE

Disregard the MA lamp and presence of alert tones.



16 Set SIGNAL SELECT BLANKING switch to NORM.

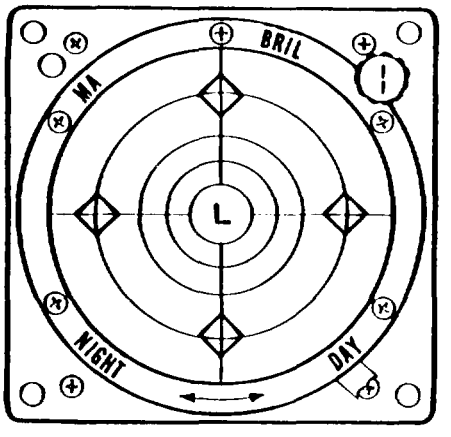
17 **CHECK** that

- the radar signal indicator displays a no signal pattern.
- an L symbol is present in the center of the no signal pattern.

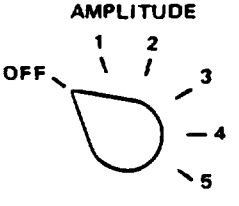
NOTE

The location of symbols displayed on the radar signal indicator are NOT critical; each symbol may vary slightly in position.

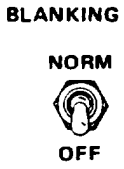
NO SIGNAL PATTERN



18 Set SIGNAL SELECT AMPLITUDE switch to OFF.



19 Set SIGNAL SELECT BLANKING switch to OFF.



20 Set SIGNAL SELECT CORR switch

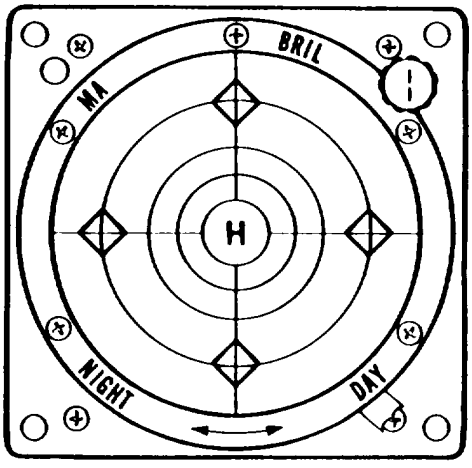
21 Set CONTROL UNIT SIM ALT HI/LOW switch to HI.

22 **CHECK** that an H symbol is displayed in the center of the no signal pattern.

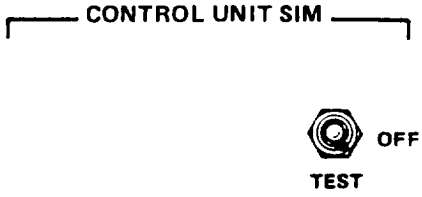
N O T E

The location of symbols displayed on the radar signal indicator are NOT critical; each symbol may vary slightly in position.

NO SIGNAL PATTERN



23 Set and hold CONTROL UNIT SIM TEST switch to the up position.

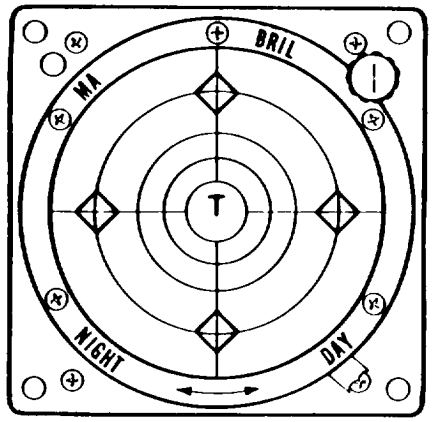


24 **CHECK** that the radar signal indicator displays the null pattern.

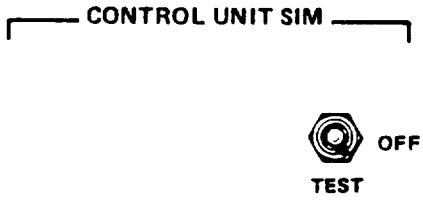
NOTE

The location of symbols displayed on the radar signal indicator are NOT critical; each symbol may vary slightly in position.

NULL PATTERN



25 Momentarily set CONTROL UNIT SIM TEST switch to the TEST position.



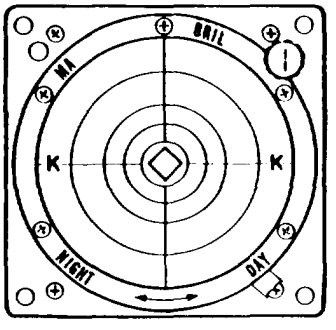
26

that

- the radar signal indicator displays the processor unit self test patterns as indicated.
- an audio tone is present during the display of pattern no. 1, 2 and 3 by adjusting the CONTROL UNIT SIM AUDIO control.

NOTE

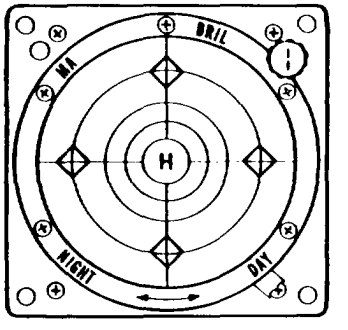
Disregard the flashing of the MA lamp during display of pattern no. 3.



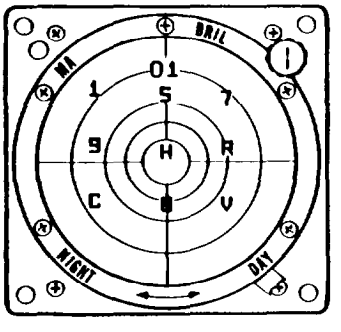
PATTERN NO. 1

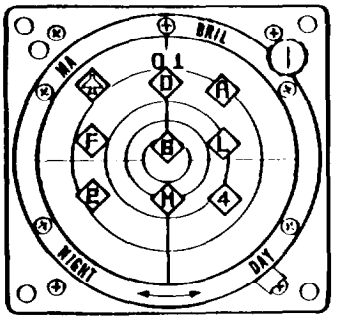
NOTE

The location of symbols displayed on the radar signal indicator are NOT critical; each symbol may vary slightly in position.



NO SIGNAL PATTERN



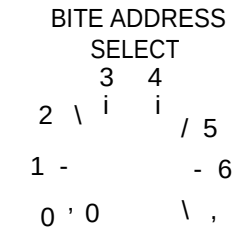


27

Set oscilloscope controls to the following:

- VOLTS/DIV: 2.0 (CH 1)
- TIME/DIV: 0.2 USEC
- SOURCE: CH 1
- COUPLING: AC
- TRIG MODE: NORM
- VERT MODE: CH 1
- SLOPE+ (positive)

28 Set BITE ADDRESS SELECT switch to 5.



29 Connect channel 1 of the oscilloscope to TEST POINTS E2 and the ground lead to TEST POINTS GND.

30 **CHECK** that channel 1 of the oscilloscope displays a 2 MHz free-running clock waveform (period is approximately 0.5 microsecond).

31 Set BITE ADDRESS SELECT switch to 7.

32 Connect channel 1 of the oscilloscope to TEST POINTS A3.

33 Set oscilloscope TIME/DIV control to 0.2 SEC.

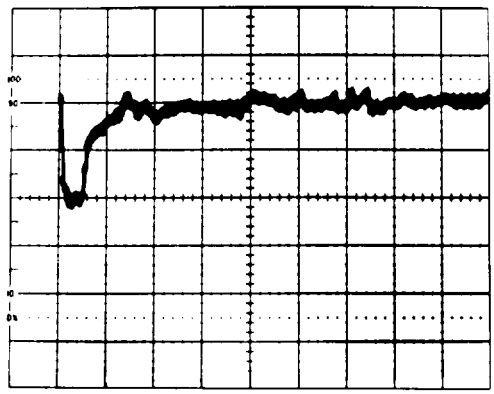
34 **CHECK** that channel 1 of the oscilloscope displays a 2.4 Hz free-running square wave (period is approximately 0,4 second).

35 Set BITE ADDRESS SELECT switch to 3.

36 Connect channel 1 of the oscilloscope to TEST POINTS B3.

37 Set oscilloscope controls to the following:
l TIM E/ DIV: 0.2 USEC
. TRIG MODE: AUTO
l SLOPE: - (negative)

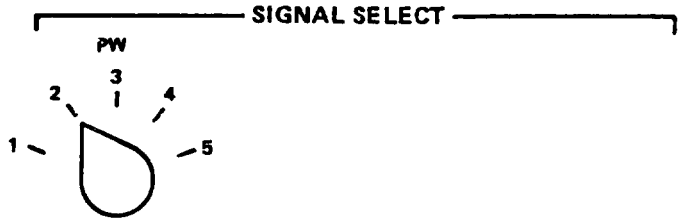
38 **CHECK** that channel 1 of the oscilloscope displays the following waveform:



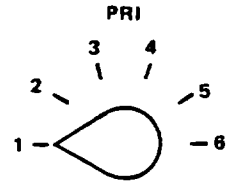
39 Connect the sync input connector of the oscilloscope to the PRF SYNC connector J7 on

40 Set BITE ADDRESS SELECT switch to O.

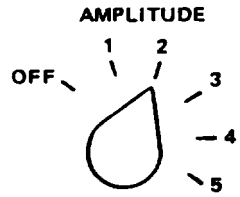
41 Set SIGNAL SELECT PW switch to 2



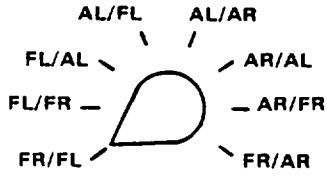
42 Set SIGNAL SELECT PRI switch to 1.



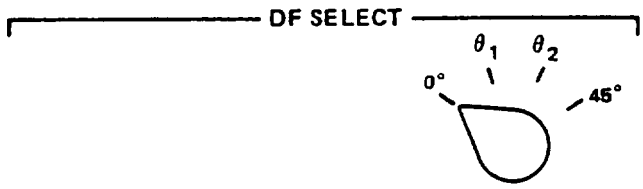
43 Set SIGNAL SELECT AMPLITUDE switch to 2.



44 Set DF SELECT octant switch to



45 Set DF SELECT angle switch to O°.

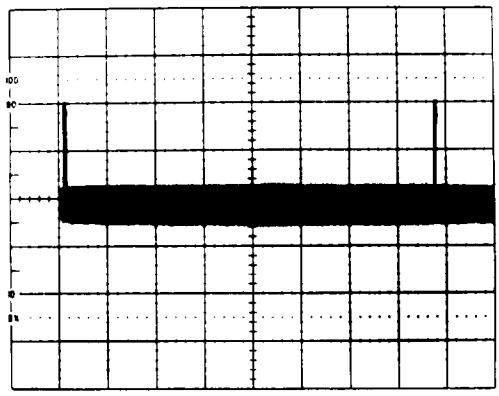


46 Connect channel 1 of the oscilloscope to TEST POINTS F2.

47 Set oscilloscope controls to the following:

- TIME/DIV: 50 USEC
- TRIG MODE: NORM
- SLOPE: + (positive)
- SOURCE: EXT

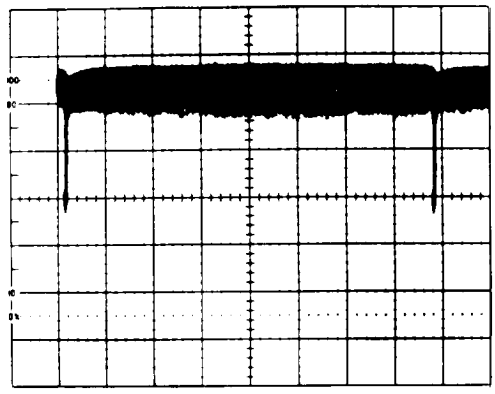
48 **CHECK** that channel 1 of the oscilloscope displays the following waveform:



49 Set BITE ADDRESS SELECT switch to 6.

50 Connect channel 1 of oscilloscope to TEST POINTS C3.

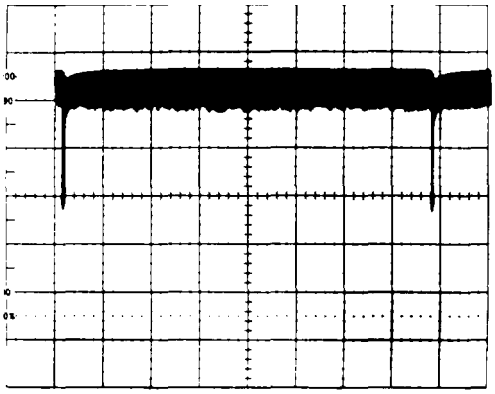
51 **CHECK** that channel 1 of the oscilloscope displays the following waveform:



52 Set BITE ADDRESS SELECT switch to 5.

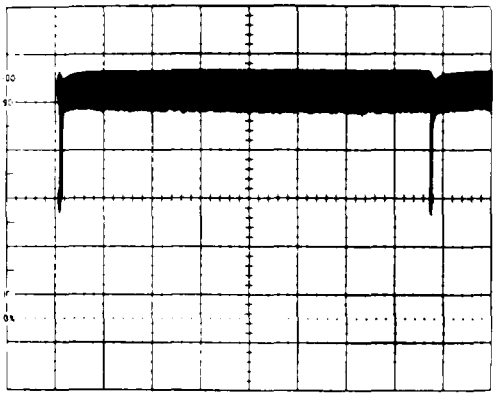
53 Connect channel 1 of oscilloscope to TEST POINTS F3.

54 **CHECK** that channel 1 of the oscilloscope displays the following waveform:



55 Connect channel 1 of oscilloscope to TEST POINTS E3.

56 CHECK that channel 1 of the ossilloscope displays the following waveform:



57 Set BITE ADDRESS SELECT switch to 4.

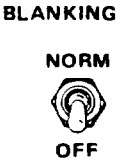
58 Connect channel 1 of oscilloscope to TEST POINTS D2.

59 **CHECK** that channel 1 of the oscilloscope displays a waveform with high to low to high

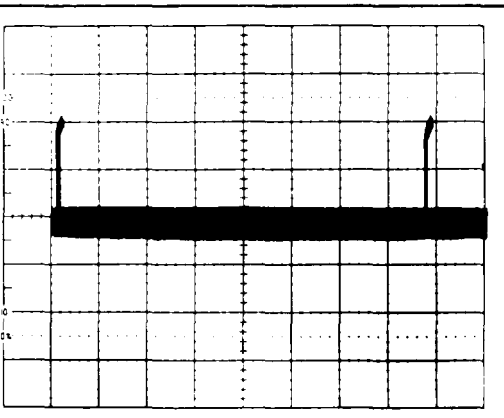
60 Set BITE ADDRESS SELECT switch to 2.

61 Connect channel 1 of the oscilloscope to TEST POINTS A3.

62 Set SIGNAL SELECT BLANKING switch to NORM.



63 **CHECK** that channel 1 of the oscilloscope displays the following waveform:

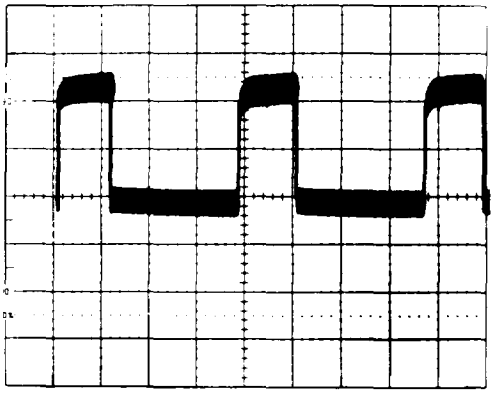


64 Set BITE ADDRESS SELECT switch to 1.

65 Connect channel 1 of oscilloscope to TEST POINTS D3.

66 Set oscilloscope TIME/DIV control at 0.1 millisecond.

67 **CHECK** that channel 1 of the oscilloscope displays the following waveform:



68 Disconnect the oscilloscope from the PTS front panel.

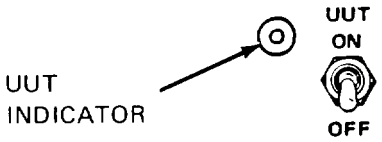
COMPUTER INTERFACE TEST

4-24. This paragraph provides you with the instructions required to check the computer interface circuits of the PTS.

NOTE

The working processor unit should still be connected to the PTS.

1 Observe that the UUT indicator is still lit.



2 With the exception of the POWER ON/OFF switch and the UUT ON/OFF switch, set all other PTS front panel controls to their initial control settings as shown in chapter 3, section 11, paragraph 3-18. Leave POWER ON/OFF switch at ON and UUT ON/OFF switch at ON.

3 Press the RESET pushbutton switch.

4 Observe that the TEST NO indicator displays FOO.

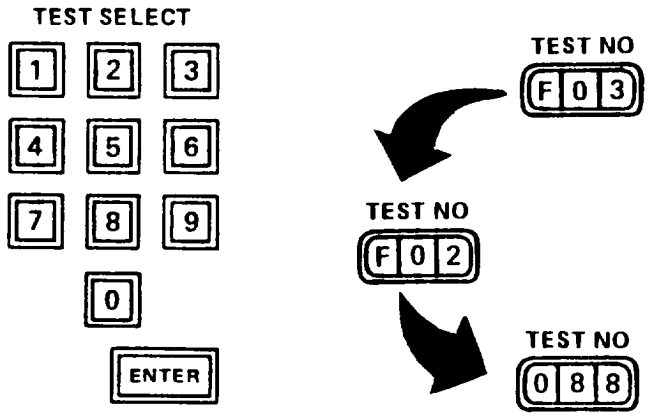
5 Open cassette assembly C5079579 and insert the PTS PUT diagnostic program cassette tape MTC5079655 into the MTCT. Refer to chapter 3, section II, paragraph 3-22 for the cassette loading procedure.

6 Press the REWIND pushbutton switch and observe that the REWIND lamp is lit for as long as the REWIND pushbutton switch is pressed.

7 Observe that the TEST NO indicator displays F02 and the cassette tape rewinds and stops.

8 After the cassette tape has stopped, momentarily press, in sequence, TEST SELECT pushbutton keys O, 8, and 8, and momentarily press the ENTER pushbutton switch. Observe that

- the ENTER lamp lights.
- the TEST NO indicator momentarily displays F03, and then F02 followed by 088.
- no error messages are displayed.
- the cassette tape moves forward.



NOTE

If for step 9, FOC is NOT displayed on TEST NO indicator within 2 minutes or E04 IS displayed, press RESET pushbutton switch and repeat steps 6 through 9. If step 9 fails a second time, proceed to section V (troubleshooting) of this chapter.

9 After the cassette tape has stopped, CHECK that

- the TEST NO indicator displays FOC within 2 minutes.
- the TEST NO indicator does not display E04.

10 Press the REWIND pushbutton switch. After the cassette tape has stopped, remove the PTS PUT diagnostic program cassette tape from the MTCT. Refer to chapter 3, section 11, paragraph 3-23 for the cassette removal procedure,

11 Place cassette tape MTC5079655 into cassette assembly C5079579 and close cover.

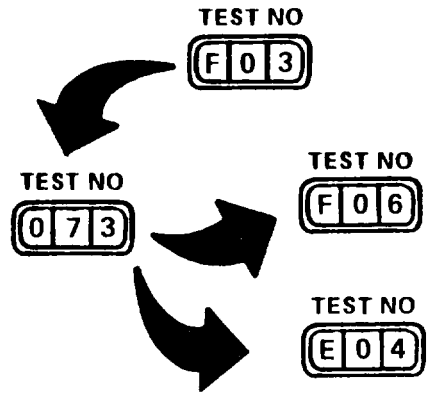
NOTE

If for step 12, E04 is displayed on TEST NO indicator instead of F06, repeat steps 3 through 12. If step 12 fails a second time, proceed to section V (troubleshooting) of this chapter.

12 Momentarily press, in sequence, TEST SELECT pushbutton keys, O, 7, and 3, and then momentarily press the ENTER pushbutton switch.

CHECK that

- the TEST NO indicator momentarily displays F03, and then 073 followed by F06.
- the TEST NO indicator does not display E04.



AUTO/MAN MODE TEST

4-25. This paragraph provides you with the instructions required to check the automatic/manual mode lock-out circuits of the PTS.

NOTE

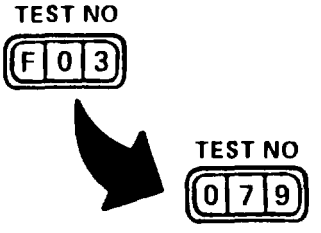
The working processor unit should still be connected to the PTS.

1 Set CONTROL UNIT SIM ALT Hi/LOW switch to HI.

2 Press the RESET pushbutton switch.

3 Observe that the TEST NO indicator displays FOO.

4 Momentarily press, in sequence, TEST SELECT pushbutton keys, O, 7. and 9, and then momentarily press the ENTER pushbutton switch. Observe that the TEST NO indicator momentarily displays F03, followed by 079.

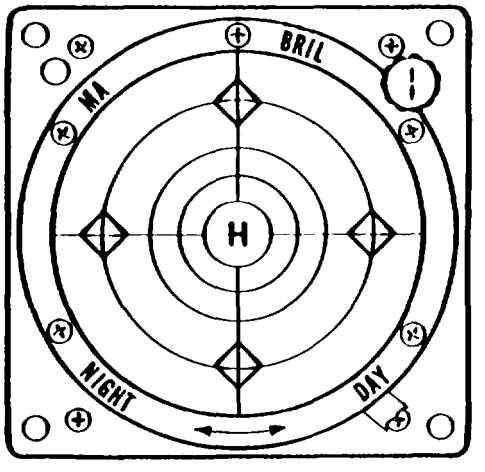


5 Observe that the no signal pattern is displayed on the radar signal indicator.

NOTE

The location of symbols displayed on the radar signal indicator are NOT critical; each symbol may vary slightly in position.

NO SIGNAL PATTERN



6 Press the AUTO/MAN MODE pushbutton switch and **CHECK** that

- the MAN lamp goes out.
- the AUTO lamp goes on.

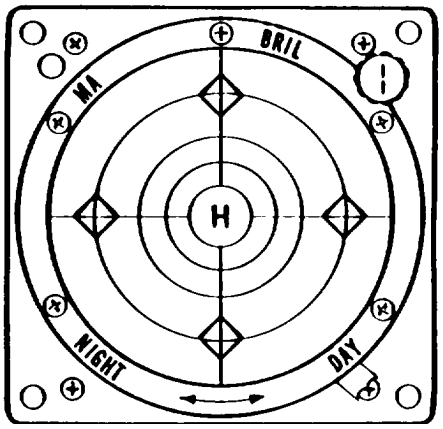
7 Momentarily set CONTROL UNIT SIM TEST switch to the TEST position.

8 **CHECK** that the radar signal indicator continues to display the no signal pattern (no other pattern(s) are displayed).

NOTE

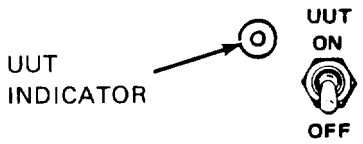
The location of symbols displayed on the radar signal indicator are NOT critical; each symbol may vary slightly in position,

NO SIGNAL PATTERN



9 Press the AUTO/MAN MODE pushbutton switch and observe that the AUTO lamp goes out and the MAN lamp goes on.

10 Set UUT ON/OFF switch to OFF and observe that the UUT indicator goes out.

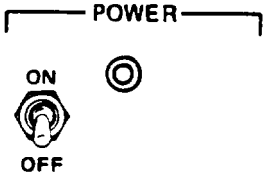


11 Disconnect the processor unit from the PTS front panel by removing cables W2, W4 and W5. Store cables back into the top cover of PTS case.

CONTROL UNIT STIMULI TEST

4-26. This paragraph provides you with the instructions required to check the control unit stimulation circuits of the PTS. These circuits can only be checked by connecting a known working control unit to the PTS.

1 Set the PTS POWER ON/OFF switch to OFF and observe that POWER indicator is off.



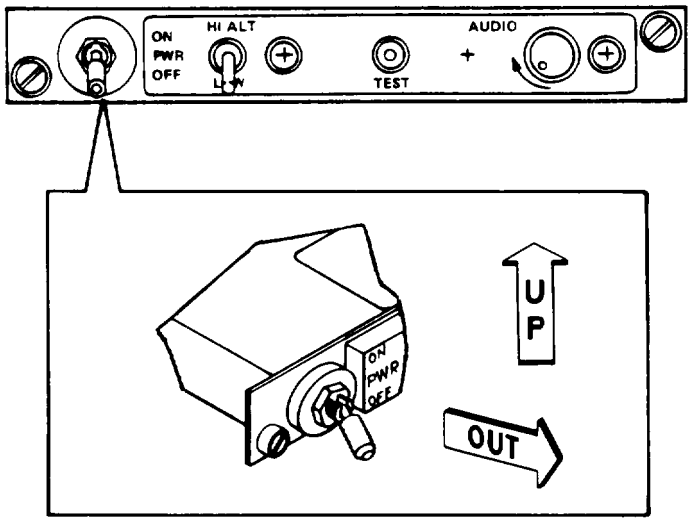
2 Connect a known working control unit to the PTS front panel as specified in the PTS to control unit cable harness connections of chapter 3, section II, paragraph 3-21.

3 Set the PTS POWER ON/OFF switch to ON and observe that the POWER indicator

4 Set control unit PWR ON/OFF switch to ON.

NOTE

The switch must be pulled out, then up to be set to the ON position.



5 Using a multimeter, connect the negative lead to TEST POINTS GND and the positive lead to TEST POINTS D6.

6 **CHECK** that multimeter indicates between +25.0 and +27.0 V.

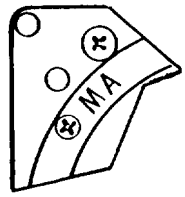
7 Disconnect multimeter from TEST POINTS D6 and GND.

8 Press the RESET pushbutton switch.

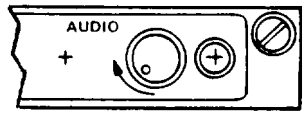
9 Observe that the TEST NO indicator displays FOO.

10 Set the CONTROL UNIT AUDIO/MA ON/OFF switch to ON.

11 **CHECK** that the MA indicator on the radar signal indicator is flashing on and off.



12 Slowly turn the control unit AUDIO control from the full counterclockwise position to full clockwise position and **CHECK** the following:



. that a beeping audio tone is heard.
l that the tone increases in volume as the AUDIO control is turned clockwise.

13 Turn the control unit AUDIO control back to full counterclockwise position.

14 Set the CONTROL UNIT AUDIO/MA ON/OFF switch to OFF.

15 Observe that the MA indicator on the radar signal indicator remains lit.

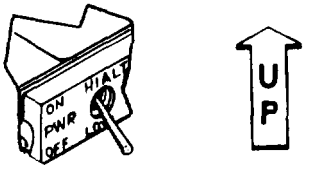
CONTROL UNIT INDICATORS TEST

4-27. This paragraph provides you with the instructions required to check the control unit response circuits of the PTS.

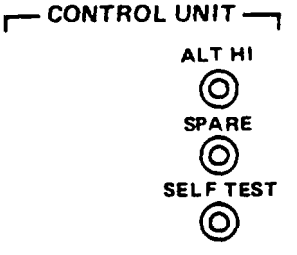
NOTE

The working control unit should still be connected to the PTS.

1 Set the control unit HI ALT/LOW switch to HI ALT.



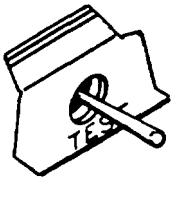
2 Observe that the PTS CONTROL UNIT ALT HI indicator is lit.



3 Set the control unit HI ALT/LOW switch to LOW.

4 **CHECK** that the PTS CONTROL UNIT ALT HI indicator is off.

5 Set and hold the control unit TEST switch to up position.



6 Observe that the PTS CONTROL UNIT SPARE indicator is lit.

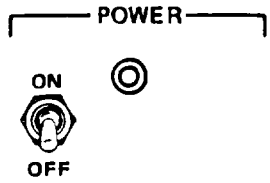
7 Set and hold control unit TEST switch to TEST position.

8 Observe that the PTS CONTROL UNIT SPARE indicator is off and the SELF TEST indicator is lit.

9 Release the control unit TEST switch and observe that the PTS CONTROL UNIT SELF TEST indicator is off.

10 Set control unit PWR ON/OFF switch to OFF.

11 Set the PTS POWER ON/OFF switch to OFF and observe that POWER indicator is off.



12 Disconnect the control unit from the PTS front panel by removing cable W3. Store cable back into the top cover of the PTS case.

NOTE

If, during the performance of this electrical check procedure, at least one hour has elapsed, perform step 13. Non-performance of step 13, IN NO WAY, detracts from determing that the PTS has met minimum performance standards established by the successful completion of these electrical check procedures.

13 **CHECK** that the HOURS ELAPSED TIME meter has increased in value from that recorded in step 1 of paragraph 4-16.

SECTION V
TROUBLESHOOTING PROCEDURES

SECTION CONTENTS PAGE

GENERAL

4-28. Troubleshooting of the PTS at the AVIM level is defined by the Maintenance Allocation Chart (MAC) contained in appendix B. Troubleshooting is accomplished by following the troubleshooting sequence, troubleshooting cross-reference index, and troubleshooting flow charts provided in subsequent paragraphs. After a fault has been isolated and repaired, you must perform the PTS electrical check procedures provided in section IV of this chapter to make sure that the PTS is operational.

TROUBLESHOOTING SEQUENCE

4-29. This paragraph provides you with the sequence in which troubleshooting of the PTS is performed. This sequence MUST be followed to ensure that the malfunctioning assembly or front panel piece part component is correctly identified.

NOTE

To have reached this troubleshooting sequence, a failure must have occurred at a specific check step of the electrical check procedures contained in section IV of this chapter. If you have not performed the PTS electrical check procedure, refer to Section IV of this chapter. If you were performing these procedures and a failure occurred, proceed to the TROUBLESHOOTING SEQUENCE provided below.

A. Using the Paragraph Reference and Step Reference columns of the troubleshooting cross-reference index, locate your fault indication in the Fault column.

B. Check the Entry Point/Corrective Action column opposite your fault indication to determine the next instruction.

- If you are directed in this column to replace a specific assembly or piece part component, perform troubleshooting sequences C through D and F.

- If you are directed to a flow chart entry point, locate the appropriate PTS flow chart within this section. Then perform the procedures contained within that flow chart.

NOTE

Do not change the setting of any PTS control or switch.

C. To replace an assembly or piece part component, you MUST: shut down power to the PTS; then refer to the removal procedures contained in section VI of this chapter.

D. Install a new assembly or piece part component according to the installation procedures contained in section VI of this chapter. After installation, turn on power to the PTS and press the RESET pushbutton on the PTS front panel.

E. Rerun the specific test paragraph (that failed) of the PTS electrical check procedure contained in Section IV of this chapter to determine whether the replaced assembly or piece part component is in fact defective.

- If the test paragraph now passes, you have found the defective assembly or piece part component; therefore send that defective assembly to the next higher level of maintenance or throw away the defective piece part component. Set POWER ON/OFF switch at OFF and return to paragraph 4-16, step 2. I

- If the test paragraph fails again, return to the instruction box of the PTS troubleshooting flow chart that you left and continue troubleshooting as indicated.

F. Rerun the specific test paragraph (that failed) of the PTS electrical check procedure contained in Section IV of this chapter to determine whether the replaced assembly or piece part component is in fact defective.

- If the test paragraph now passes, you have found the defective assembly or piece part component; therefore send that defective assembly to the next higher level of maintenance or throw away the defective piece part component. Set POWER ON/OFF switch at OFF and return to paragraph 4-16, step 2.

- If the test paragraph fails again, proceed to troubleshooting sequence G.

G. The cause of the malfunction MUST either be: a short or open exists in the wiring (interconnections of the circuit cards in the card cage or interconnections between the front panel piece part components and the card cage) or a loading problem exists, where one of the input stages of connected circuit card(s) is loading down the output stage of the originating circuit card. To further isolate the malfunction, proceed to troubleshooting sequence H.

H. Replace the card cage assembly by performing troubleshooting sequences C and D; then proceed to troubleshooting sequence 1.

I. Rerun the specific test paragraph (that failed) of the PTS electrical check procedure contained in Section IV of this chapter to determine whether the replaced card cage assembly is in fact defective.

- If the test paragraph now passes, the card cage assembly you have just replaced is defective. Therefore, send that defective card cage assembly to the next higher level of maintenance. Set POWER ON/OFF switch at OFF and return to paragraph 4-16, step 2.

- If that test paragraph fails again after card cage replacement, proceed to troubleshooting sequence J.

J. The cause of the malfunction could be that a short or open exists in the PTS wiring, which interconnects front panel piece part components with the card cage, power supply, choke assembly and the RFI enclosure. In order to determine where the short or open exists, continuity checks of the wiring MUST be performed. You will find at the rear of this section a PTS electrical schematic diagram and associated PTS wiring information (paragraph 4-32) containing wiring harness diagrams and wire run lists. Refer to paragraph 4-32, and use these wiring harness diagrams and wire run lists to perform continuity checks of associated PTS wiring; it may be necessary to perform disassembly of mechanical/electrical assemblies which interfere with making some of these continuity checks. Refer to the removal procedures contained in Section VI of this chapter, when disassembly is necessary.

- If a short or open is found in the wiring, repair the wire(s) and return to paragraph 4-16, step 2.

- If no shorts or opens can be found in the wiring, proceed to troubleshooting sequence K.

K. The malfunction MUST be a loading problem caused by one of the circuit cards in the card cage. In order to determine which circuit card is loading down the output stage of an associated circuit card, perform the following:

1. Set POWER ON/OFF switch to OFF and remove circuit card Al from the card cage (refer to the removal procedure in Section VI of this chapter).

2. Install a new Al circuit card into the card cage (refer to the installation procedure in Section VI of this chapter).

3. Set POWER ON/OFF switch to ON and press the RESET pushbutton switch.

4. Rerun the specific test paragraph (that failed) of the PTS electrical check procedure contained in Section IV of this chapter to determine whether the replaced circuit card is in fact defective.

   - If the test paragraph now passes, the circuit card you have just replaced is defective. Therefore, send that defective circuit card to the next higher level of maintenance. Set POWER ON/OFF switch to OFF and return to paragraph 4-16, step 2.

   - If the test paragraph fails again after circuit card replacement, repeat steps 1 through 4 for the next circuit card in the card cage until the defective circuit card is found.

TROUBLESHOOTING CROSS-REFERENCE INDEX

4-30. The following chart contains the troubleshooting cross-reference index for the processor test set.

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
PTS POWER ON TEST			
● POWER ON indicator is not lit.	4-16	3	Entry Point A
● Cooling fan is not operating.	4-16	4	Entry Point B
● SEL lamp is lit.	4-16	6	Entry Point C
● AUTO lamp is lit or MAN lamp is not lit.	4-16	8	Entry Point D
● CARD FAIL PSI indicator is not lit.	4-16	10	Entry Point E
● One or more digits of TEST NO indicator are blank.	4-16	11	Entry Point F
● TEST NO indicator does not display F00.	4-16	11	Entry Point G
● CONTROL UNIT ALT HI indicator is not lit.	4-16	12	Entry Point H
● Any CARD FAIL indicator (Al thru A8) is lit.	4-16	13	Entry Point I

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST			
● TEST NO indicator does not display a 1 in rightmost digit.	4-17	1	Entry Point J
● TEST NO indicator does not display a O in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a 2 in rightmost digit.	4-17	1	Entry Point L
● TEST NO indicator does not display a 1 in centermost digit.	4-17	1	Entry Point M
● TEST NO indicator does not display a 3 in rightmost digit.	4-17	1	Entry Point N
● TEST NO indicator does not display a 2 in centermost digit.	4-17	1	Entry Point O
● TEST NO indicator does not display a 1 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a 4 in rightmost digit.	4-17	1	Entry Point P
● TEST NO indicator does not display a 3 in centermost digit.	4-17	1	Entry Point Q
● TEST NO indicator does not display a 2 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a 5 in rightmost digit.	4-17	1	Entry Point R
● TEST NO indicator does not display a 4 in centermost digit.	4-17	1	Entry Point S
● TEST NO indicator does not display a 3 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a 6 in rightmost digit.	4-17	1	Entry Point T
● TEST NO indicator does not display a 5 in centermost digit.	4-17	1	Entry Point U
● TEST NO indicator does not display a 4 in leftmost digit.	4-17	1	Entry Point K

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST - Continued			
● TEST NO indicator does not display a 7 in rightmost digit.	4-17	1	Entry Point V
● TEST NO indicator does not display a 6 in centermost digit.	4-17	1	Entry Point W
● TEST NO indicator does not display a 5 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display an 8 in rightmost digit.	4-17	1	Entry Point X
● TEST NO indicator does not display a 7 in centermost digit.	4-17	1	Entry Point Y
● TEST NO indicator does not display a 6 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a 9 in rightmost digit.	4-17	1	Entry Point Z
● TEST NO indicator does not display an 8 in centermost digit.	4-17	1	Entry Point AA
● TEST NO indicator does not display a 7 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a O in rightmost digit.	4-17	1	Entry Point AB
● TEST NO indicator does not display a 9 in centermost digit.	4-17	1	Entry Point AC
● TEST NO indicator does not display a 8 in leftmost digit.	4-17	1	Entry Point K
● TEST NO indicator does not display a 9 in leftmost digit.	4-17	1	Entry Point K
● SEL lamp does not light.	4-17	2	Entry Point AD
● SEL lamp does not go out.	4-17	3	Replace S8
● CONTROL UNIT ALT HI indicator does not go off and then relight.	4-17	4	Entry Point AE
● CONTROL UNIT ALT HI indicator does not go out.	4-17	4	Entry Point AF

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST - Continued			
● CONTROL UNIT SELF TEST indicator does not light.	4-17	4,5	Entry Point AG
● TEST NO indicator displays E50.	4-17	4,5	Entry Point AH
● TEST NO indicator displays E51.	4-17	4,5	Entry Point Al
● TEST NO indicator displays E52.	4-17	4,5	Entry Point Al
● TEST NO indicator displays E53.	4-17	4,5	Entry Point Al
● TEST NO indicator displays E54.	4-17	4,5	Entry Point AJ
● TEST NO indicator displays E55.	4-17	4,5	Entry Point AK
● TEST NO indicator displays E56.	4-17	4,5	Entry Point AL
● TEST NO indicator displays E57.	4-17	4,5	Entry Point AL
● TEST NO indicator displays E58.	4-17	4,5	Entry Point AM
● TEST NO indicator displays E59.	4-17	4,5	Entry Point AM
● TEST NO indicator displays E5A.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E5B.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E5C.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E5D.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E5E.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E5F.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E60.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E61.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E62.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E63.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E64.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E65.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E66.	4-17	4,5	Entry Point AN

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST - Continued			
● TEST NO indicator displays E67.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E68.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E69.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E6A.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E6B.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E6C.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E6D.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E6E.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E6F.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E70.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E71.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E72.	4-17	5	Entry Point AN
● TEST NO indicator displays E73.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E74.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E75.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E76.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E77.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E78.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E79.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E7A.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E7B.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E7C.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E7D.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E7E.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E7F.	4-17	4,5	Entry Point AN

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST - Continued			
● TEST NO indicator displays E80.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E81.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E82.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E83.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E84.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E85.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E86.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E87.	4-17	4,5	Entry Point AN
● TEST NO indicator displays E89.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E8A.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E8B.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E8C.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E8D.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E8E.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E8F.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E90.	4-17	4,5	Entry Point AO
● TEST NO indicator displays E91.	4-17	4,5	Entry Point AP
● TEST NO indicator displays E92.	4-17	4,5	Entry Point AP
● TEST NO indicator displays E93.	4-17	4,5	Entry Point AP
● TEST NO indicator displays E94.	4-17	4,5	Entry Point AP
● CONTROL UNIT SELF TEST indicator does not go out at FFF.	4-17	5	Entry Point AQ
● PASS indicator does not flash on and off.	4-17	6	Entry Point AR
● FAIL indicator is lit.	4-17	6	Entry Point AS

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST - Continued			
● CARD FAIL PSI indicator does not flicker.	4-17	7	Entry Point AT
● CARD FAIL indicators Al thru A8 do not light and then go out.	4-17	8	Entry Point AU
● CONTROL UNIT ALT HI indicator does not light and then go out.	4-17	8	Replace circuit card Al
● CONTROL UNIT SPARE indicator does not light and then go out.	4-17	8	Entry Point AV
● SELF TEST PASS indicator does not light and then go out.	4-17	8	Replace circuit card Al
● SELF TEST FAIL indicator does not light and then go out.	4-17	8	Entry Point AW
● No waveform is displayed.	4-17	10	Entry Point AX
● Waveform does not flash on and off at 250 msec rate.	4-17	10	Replace circuit card A4
● PRI of waveform is not between 450 and 550 usec.	4-17	11	Replace circuit card A4
● MA indicator does not flash on and off.	4-17	12	Entry Point AY
● Beeping audio tone is not heard.	4-17	13	Entry Point AZ
● Audio tone does not increase in voulume.	4-17	13	Entry Point BA
● No strobe is displayed.	4-17	15	Entry Point BB
● Strobe does not shift up and down along the 0°/1800 axis.	4-17	15	Entry Point BC
● Strobe does not shift up and down between positions A and B.	4-17	15	Entry Point BC
● BRIL control does not increase or decrease the brilliance of the display.	4-17	16	Replace Radar Signal Indicator AI0
● REWIND lamp does not light when REWIND pushbutton switch is pressed.	4-17	21	Replace switch S23

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SELF TEST - Continued			
● TEST NO indicator does not display F02.	4-17	22	Entry Point BD
● TEST NO indicator displays E00.	4-17	22	Entry Point BE
● TEST NO indicator displays E01.	4-17	22	Entry Point BE
● TEST NO indicator displays E06.	4-17	22	Entry Point BE
● Cassette tape does not rewind.	4-17	22	Entry Point BE
● Cassette tape does not stop rewinding.	4-17	22	Entry Point BE
● ENTER lamp does not light when ENTER push button switch is pressed.	4-17	23	Replace switch S22
● TEST NO indicator does not display F03, then F02, followed by 081.	4-17	23	Entry Point BF
● TEST NO indicator displays E02.	4-17	23	Entry Point BE
● TEST NO indicator displays E03.	4-17	23	Entry Point BE
● TEST NO indicator displays E09.	4-17	23	Entry Point BE
● Cassette tape does not move forward.	4-17	23	Entry Point BG
● Cassette tape does not stop within 2 minutes.	4-17	24	Entry Point BG
● TEST NO indicator does not display FOC.	4-17	24	Entry Point BG
● TEST NO indicator displays E07.	4-17	24	Entry Point BH
● TEST NO indicator displays EO1.	4-17	24	Entry Point BE
SIGNAL SELECT TEST			
● No waveform is present at connector J7.	4-18	7	Entry Point BI
● PRI of waveform is not between 382 and 386 usec.	4-18	7	Entry Point BI

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SIGNAL SELECT TEST - Continued			
l No waveform is present at TEST POINTS A4.	4-18	9	Entry Point BJ
● PW of waveform is not between 0.45 and 0.55 usec.	4-18	9	Entry Point BK
● PW of waveform is not between 0.565 and 0.685 usec.	4-18	11	Entry Point BK
● PW of waveform is not between 0.680 and 0.820 usec.	4-18	13	Entry Point BK
● PW of waveform is not between 1.625 and 2.075 usec.	4-18	16	Entry Point BK
● PW of waveform is not between 43.0 and 53.0 usec.	4-18	19	Entry Point BK
● PRI of waveform is not between 508 and 512 usec.	4-18	22	Entry Point BL
● PRI of waveform is not between 804 and 808 usec.	4-18	24	Entry Point BL
● PRI of waveform is not between 898 and 902 usec.	4-18	26	Entry Point BL
● PRI of waveform is not between 958 and 962 usec.	4-18	28	Entry Point BL
● PRI of waveform is not between 2,908 and 2,912 usec.	4-18	**30**	Entry Point BL
● Amplitude of waveform is not between +1.2 and +1.8 V.	4-18	**32**	Entry Point BM
● Amplitude of waveform is not between +0.4 and +0.6 V.	4-18	**34**	Entry Point BM
● Amplitude of waveform is not between +1.6 and +2.4 V.	4-18	**36**	Entry Point BM
● Amplitude of waveform is not between +148 and +188 mV.	4-18	**40**	Entry Point BM
● Amplitude of waveform is not between +92 and +132 mV.	4-18	**42**	Entry Point BM

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SIGNAL SELECT TEST - Continued			
● No waveform is displayed at TEST POINTS D4.	4-18	46	Entry Point BN
● Amplitude of waveform is not between +0,6 and +0.9 V.	4-18	46	Entry Point BO
● Amplitude of waveform is not between +0.45 and +0.75 V.	4-18	48	Entry Point BP
● Amplitude of waveform is not between +1.2 and +1.8 V.	4-18	51	Entry Point BP
● A waveform is present at TEST POINTS D4.	4-18	54	Entry Point BP
● A waveform is present at TEST POINTS B4.	4-18	56	Entry Point BJ
● A waveform is present at TEST POINTS C4.	4-18	58	Entry Point BJ
● A waveform is present at TEST POINTS A4.	4-18	61	Entry Point BJ
● No waveform is displayed on channel 1 at TEST POINTS A4.	4-18	65	Entry Point BJ
● No waveform is displayed on channel 2 at TEST POINTS D4.	4-18	66	Entry Point BJ
● Amplitude of waveform on channel 1 is greater than amplitude of waveform on channel 2.	4-18	67	Entry Point BJ
● No waveform is displayed on channel 1 at TEST POINTS C4.	4-18	70	Entry Point BQ
● No waveform is displayed on channel 2 at TEST POINTS D4.	4-18	71	Entry Point BJ
● Amplitude of waveform on channel 1 is greater than amplitude of waveform on channel 2.	4-18	72	Entry Point BJ
● No waveform is displayed on channel 1 at TEST POINTS C4.	4-18	74	Entry Point BJ
● No waveform is displayed on channel 2 at TEST POINTS D4.	4-18	75	Entry Point BJ

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SIGNAL SELECT TEST - Continued			
● Amplitude of waveform on channel 2 is greater than amplitude of waveform on channel 1.	4-18	76	Entry Point BJ
● No waveform is displayed on channel 1 at TEST POINTS C4.	4-18	79	Entry Point BJ
● No waveform is displayed on channel 2 at TEST POINTS B4.	4-18	80	Entry Point BR
● Amplitude of waveform on channel 2 is greater than amplitude of waveform on channel 1.	4-18	81	Entry Point BJ
● No waveform is displayed on channel 1 at TEST POINTS C4.	4-18	83	Entry Point BJ
● No waveform is displayed on channel 2 at TEST POINTS B4.	4-18	84	Entry Point BJ
● Amplitude of waveform on channel 1 is greater than amplitude of waveform on channel 2.	4-18	85	Entry Point BJ
● No waveform is displayed on channel 1 at TEST POINTS A4.	4-18	88	Entry Point BS
● No waveform is displayed on channel 2 at TEST POINTS B4.	4-18	89	Entry Point BS
● Amplitude of waveform on channel 1 is greater than amplitude of waveform on channel 2.	4-18	90	Entry Point BS
● No waveform is displayed on channel 1 at TEST POINTS A4.	4-18	92	Entry Point BS
● No waveform is displayed on channel 2 at TEST POINTS B4.	4-18	93	Entry Point BS
● Amplitude of waveform on channel 2 is greater than amplitude of waveform on channel 1.	4-18	94	Entry Point BS
● No waveform is displayed on channel 2 at J5.	4-18	99	Entry Point BT
● Amplitude of waveform on channel 2 is not between +11.0 and +15.0 v.	4-18	100	Replace circuit card A7

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SIGNAL SELECT TEST - Continued			
● PW of waveform on channel 2 is not between 1.5 and 2.5 usec.	4-18	101	Replace circuit card A7
● Leading edge of waveform on channel 2 does not occur between 3.0 and 4.0 usec before leading edge of waveform on channel 1.	4-18	102	Replace circuit card A4
● A waveform is displayed on channel 2 at J5.	4-18	105	Entry Point BU
● Waveform on channel 1 does not contain doublet pulses.	4-18	108	Entry Point BV
● Pulse spacing of doublet pulses is not between 0.45 and 0.55 usec.	4-18	109	Entry Point BV
● Waveform on channel 1 does not contain doublet pulses.	4-18	111	Entry Point BV
● Pulse spacing of doublet pulses is not between 0.9 and 1.1 usec.	4-18	112	Entry Point BV
● No waveform is displayed on channel 2 at TEST POINTS B6.	4-18	117	Entry Point BW
● Amplitude of waveform on channel 2 is not between +2.8 and +5.2 V.	4-18	118	Replace circuit card A7
● PW of waveform on channel 2 is not between 100 and 140 usec.	4-18	119	Replace circuit card A7
● Leading edge of waveform on channel 2 does not occur between 3.0 and 4.0 usec before leading edge of waveform on channel 1.	4-18	121	Replace circuit card A4
● A waveform is displayed on channel 2 at TEST POINTS B6.	4-18	124	Entry Point BX
BITE ADDRESS SELECT TEST			
● Logic high level is not present at TEST POINTS D7.	4-19	5	Entry Point BY
● Logic high level is not present at TEST POINTS E7.	4-19	7	Entry Point BZ

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
SIGNAL SELECT TEST - Continued			
● Logic high level is not present at TEST POINTS F7.	4-19	9	Entry Point CA
● Logic low level is not present at TEST POINTS D7.	4-19	12	Entry Point CB
● Logic high level is not present at TEST POINTS E7.	4-19	14	Replace switch S28
● Logic high level is not present at TEST POINTS F7.	4-19	16	Replace switch S28
● Logic high level is not present at TEST POINTS D7.	4-19	19	Replace switch S28
● Logic low level is not present at TEST POINTS E7.	4-19	21	Entry Point CC
● Logic high level is not present at TEST POINTS F7.	4-19	23	Replace switch S28
● Logic low level is not present at TEST POINTS D7.	4-19	26	Replace switch S28
● Logic low level is not present at TEST POINTS E7.	4-19	28	Replace switch S28
● Logic high level is not present at TEST POINTS F7.	4-19	30	Replace switch S28
● Logic high level is not present at TEST POINTS D7.	4-19	33	Replace switch S28
● Logic high level is not present at TEST POINTS E7.	4-19	35	Replace switch S28
● Logic low level is not present at TEST POINTS F7.	4-19	37	Entry Point CD
● Logic low level is not present at TEST POINTS D7.	4-19	40	Replace switch S28
● Logic high level is not present at TEST POINTS E7.	4-19	42	Replace switch S28
● Logic low level is not present at TEST POINTS F7.	4-19	44	Replace switch S28

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
BITE ADDRESS SELECT TEST - Continued			
● Logic high level is not present at TEST POINTS D7.	4-19	47	Replace switch S28
● Logic low level is not present at TEST POINTS E7.	4-19	49	Replace switch S28
● Logic low level is not present at TEST POINTS F7.	4-19	51	Replace switch S28
● Logic low level is not present at TEST POINTS D7.	4-19	54	Replace switch S28
● Logic low level is not present at TEST POINTS E7.	4-19	56	Replace switch S28
● Logic low level is not present at TEST POINTS F7.	4-19	58	Replace switch S28
DISPLAY PROTECT TEST			
● Voltage is not between +1.3V and +2.6 V at TEST POINTS B5.	4-20	9	Replace circuit card A8
● Voltage is not between +1.3 and +2.6 V at TEST POINTS D5.	4-20	15	Replace circuit card A8
● Voltage is not between +1.3 and +2.6 V at TEST POINTS C5.	4-20	21	Replace circuit card A8
● Voltage is not between +1.3 and +2.6 V at TEST POINTS A5.	4-20	27	Replace circuit card A8
SERIAL DATA TEST			
● Toggling waveform is not displayed on channel 1 at TEST POINTS 61.	4-21	7	Replace circuit card A5
● Toggling waveform is not displayed on channel 2 at TEST POINTS 62.	4-21	8	Replace circuit card A5
● Constant high logic level (between 2.4 and 5.0 V) is not displayed.	4-21	11	Replace circuit card A5
POWER SUPPLY MONITOR TEST			
● CARD FAIL PS1 indicator is off.	4-22	6	Entry Point E
● UUT indicator is off.	4-22	8	Entry Point CE
● CARD FAIL PSI indicator is on.	4-22	10	Entry Point CF

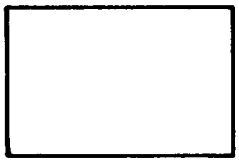
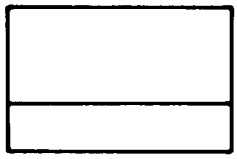
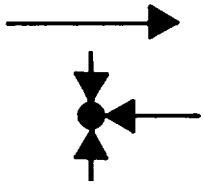
Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
PROCESSOR INTERFACE TEST			
● UUT indicator is not lit.	4-23	3	Entry Point CE
● No waveform is displayed on channel 1 at TEST POINTS A2.	4-23	14	Entry Point CG
● Amplitude of waveform is not between 0.4 and 0.8 volt.	4-23	14	Entry Point CG
● Blank display (all portions of both the diamond and 2 symbol are missing).	4-23	15	Entry Point CH
● Incomplete display (both the diamond and 2 symbol have missing portions).	4-23	15	Entry Point CH
● Diamond symbol is missing.	4-23	15	Entry Point CH
● Center of 2 symbol is not within indicated area.	4-23	15	Entry Point CH
● No signal pattern is not displayed.	4-23	17	Entry Point Cl
● L symbol is not displayed in center of no signal pattern.	4-23	17	Entry Point CJ
● H symbol is not displayed in center of no signal pattern.	4-23	22	Entry Point CK
● Null pattern is not displayed.	4-23	24	Entry Point CL
● Processor unit self test patterns are not displayed.	4-23	26	Entry Point CL
● Audio tones are not heard during display of any of the first three self test patterns.	4-23	26	Entry Point CM
● No waveform is displayed on channel 1 at TEST POINTS E2.	4-23	30	Entry Point CN
● Period of waveform is not approximately 0.5 usec.	4-23	30	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS A3.	4-23	34	Entry Point CN

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
PROCESSOR INTERFACE TEST - Continued			
● Period of waveform is not approximately 0.4 second.	4-23	34	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS B3.	4-23	38	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	38	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS F2.	4-23	48	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	48	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS C3.	4-23	51	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	51	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS F3.	4-23	54	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	54	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS E3.	4-23	56	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	56	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS D2.	4-23	59	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS A3.	4-23	63	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	63	Entry Point CN
● No waveform is displayed on channel 1 at TEST POINTS D3.	4-23	67	Entry Point CN
● Waveform displayed on channel 1 is incorrect.	4-23	67	Entry Point CN

Fault	Paragraph Reference	Step Reference	Entry Point/ Corrective Action
COMPUTER INTERFACE TEST			
● TEST NO indicator does not display FOC.	4-24	9	Replace PUT diagnostic program cassette tape MTC5079655
● TEST NO indicator displays E04.	4-24	9	Entry Point CO
● TEST NO indicator does not display F03, then 073, followed by F06.	4-24	12	Entry Point CO
● TEST NO indicator displays E04.	4-24	12	Entry Point CO
AUTO/MAN MODE TEST			
● MAN lamp does not go out.	4-25	6	Entry Point D
● AUTO lamp does not go on.	4-25	6	Entry Point D
● Any pattern, except the no signal pattern, is displayed.	4-25	8	Entry Point CP
CONTROL UNIT STIMULI TEST			
● Voltage is not between +25.0 and +27.0 at TEST POINTS D6.	4-26	6	Entry Point CQ
● MA indicator does not flash on and off.	4-26	11	Entry Point CR
● No beeping audio tone is heard.	4-26	12	Entry Point CS
● The beeping audio tone does not increase in volume.	4-26	12	Entry Point CS
CONTROL UNIT INDICATORS TEST			
● PTS CONTROL UNIT ALT HI indicator is not off.	4-27	4	Entry Point CT
● HOURS ELAPSED TIME meter has not increased in value (count) after one hour.	4-27	13	Replace meter M1

TROUBLESHOOTING FLOW CHARTS

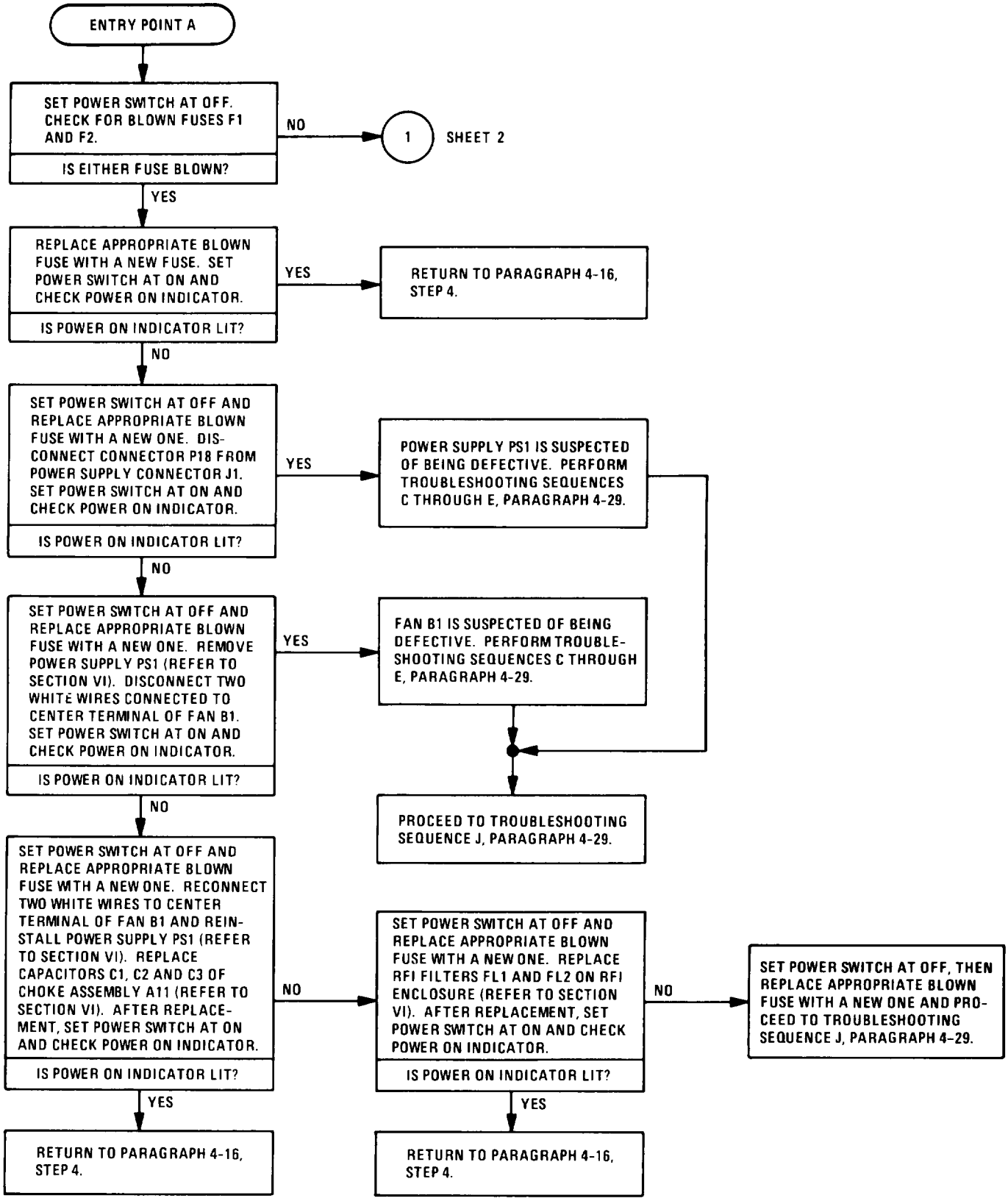
4-31. The troubleshooting flow charts are provided on the following pages. These troubleshooting flow charts have been structured with a minimum use of symbology for ease of maintenance personnel convenience and understanding. The symbols are defined as follows:

Symbol	Definition
	Entry point start symbol. Contains a letter indicating the starting point of a specific troubleshooting procedure. The letter inside this symbol is keyed to the troubleshooting cross-reference index which is keyed to the appropriate check step of the processor unit check procedure.
	Instruction symbol. Contains text indicating specific instructions to be performed.
	Instruction/decision symbol, Contains text indicating the instruction to be performed and directs personnel to the appropriate path (yes or no) based on the result of the given instruction. All instruction/decision boxes of each flow chart contain signal name mnemonics, logic level readings, or test number indications.
	Arrowhead symbol. Indicates direction of flow.
	Junction point symbol. Indicates a point where two or more paths join to produce a common path.
	Continuation symbol. Contains a number inside the symbol, indicating the continuation point of a specific troubleshooting procedure. A reference to the sheet number of the flow chart containing the corresponding continuation point is provided near the symbol.

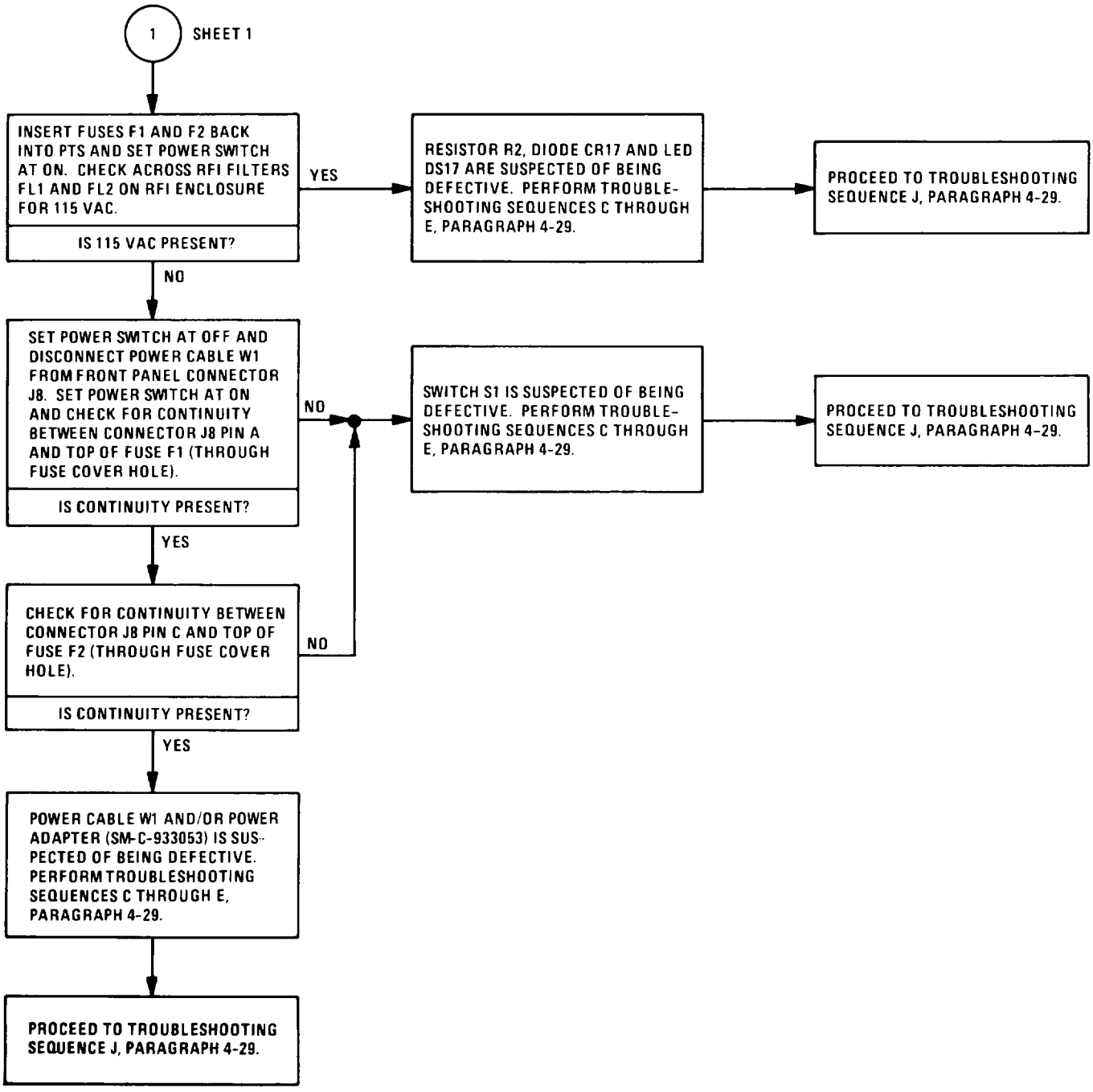
NOTE

Unless otherwise stated, all controls, switches and indicators mentioned within the flow charts are contained on the PTS.

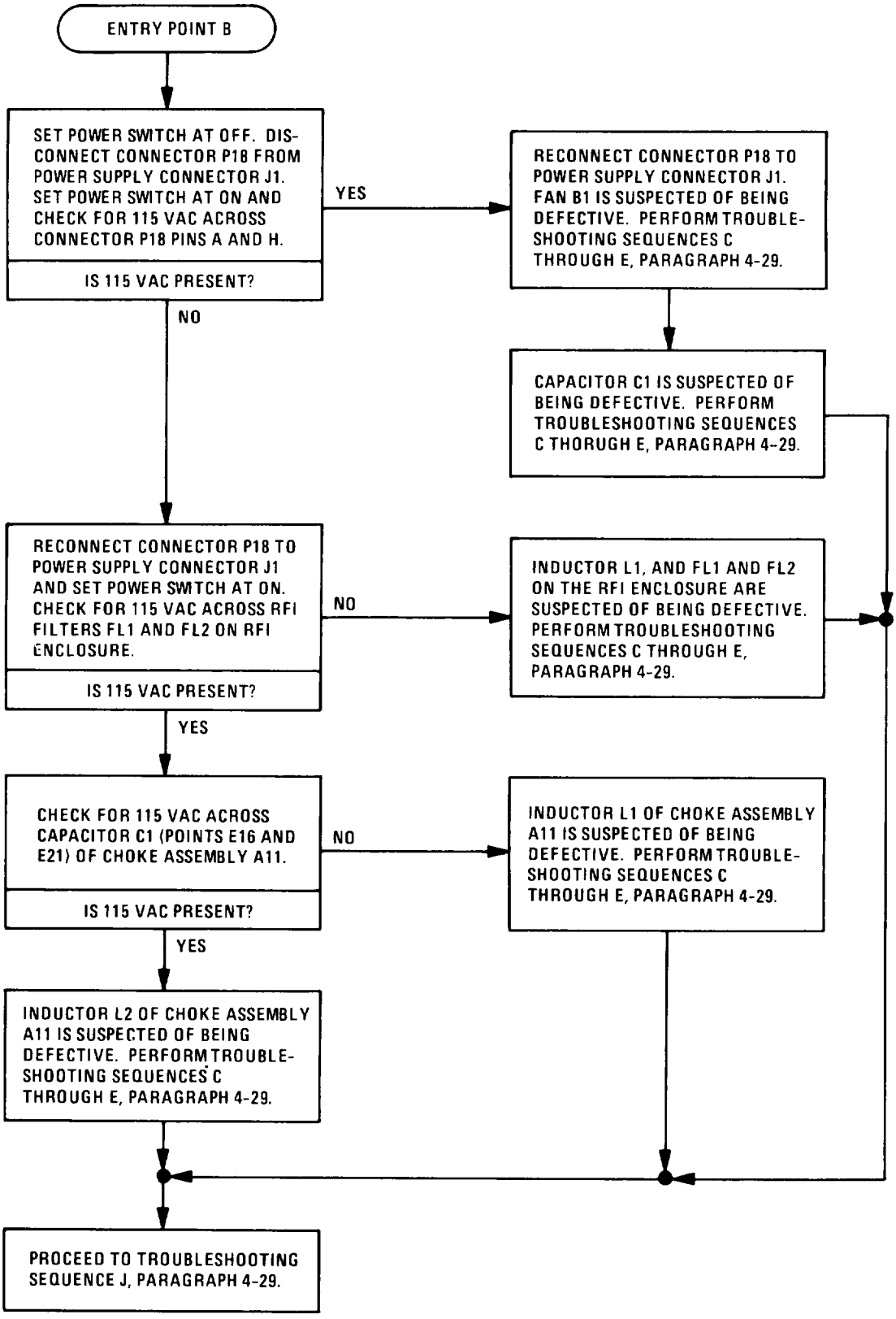
During the course of troubleshooting, you may be instructed to monitor either test point (TP) locations on circuit cards A3 thru A5 or A7 thru A9, or pin numbers on numerical display A13, toggle switch S8 or pushbutton switch S30. Refer to paragraph 4-32 for illustrations pertaining to either test point or pin number layout on these components.



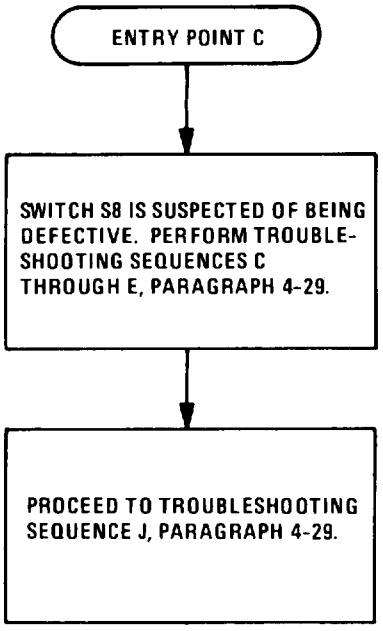
Troubleshooting Flow Chart - Entry Point A (Sheet 1 of 2)



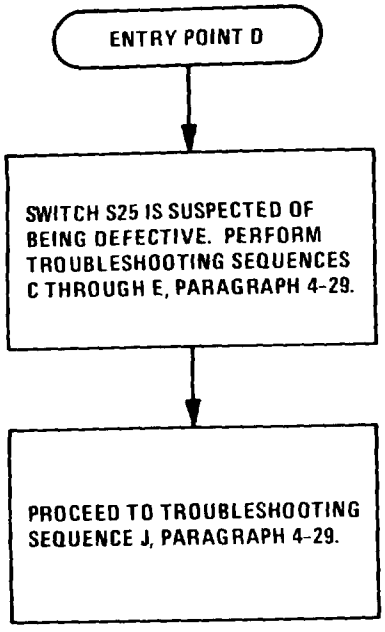
Troubleshooting Flow Chart - Entry Point A (Sheet 2 of 2)



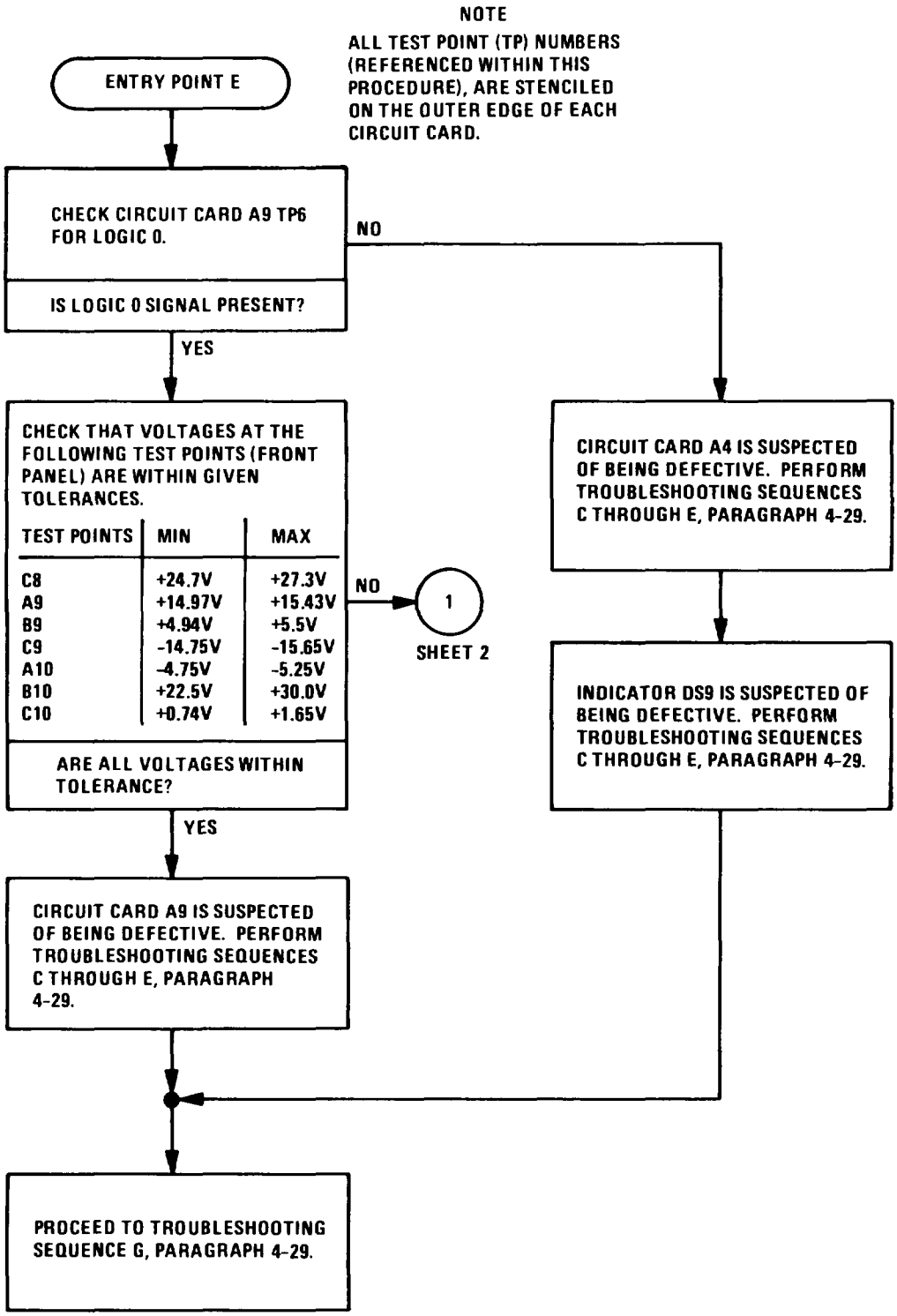
Troubleshooting Flow Chart - Entry Point B



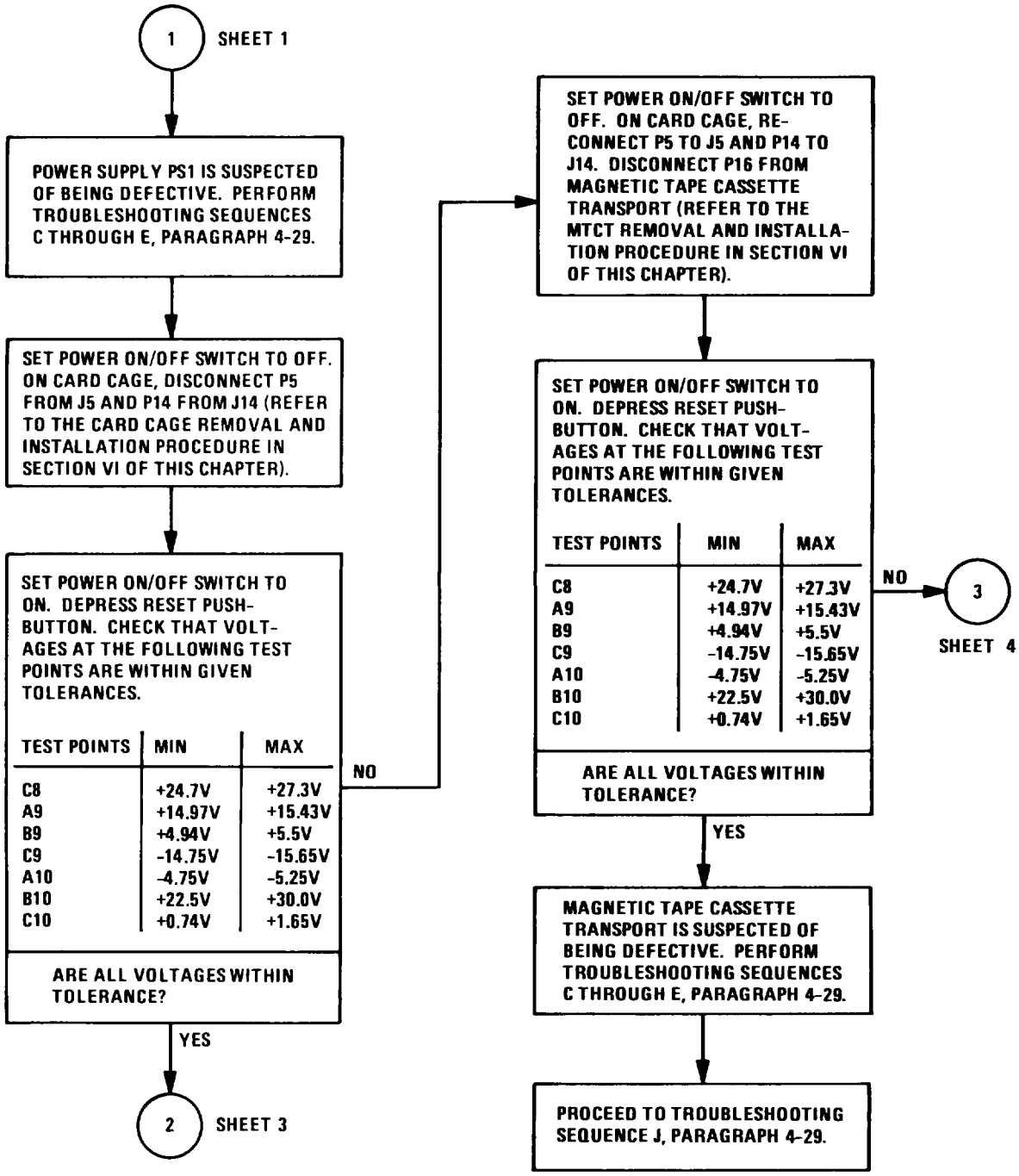
Troubleshooting Flow Chart - Entry Point C



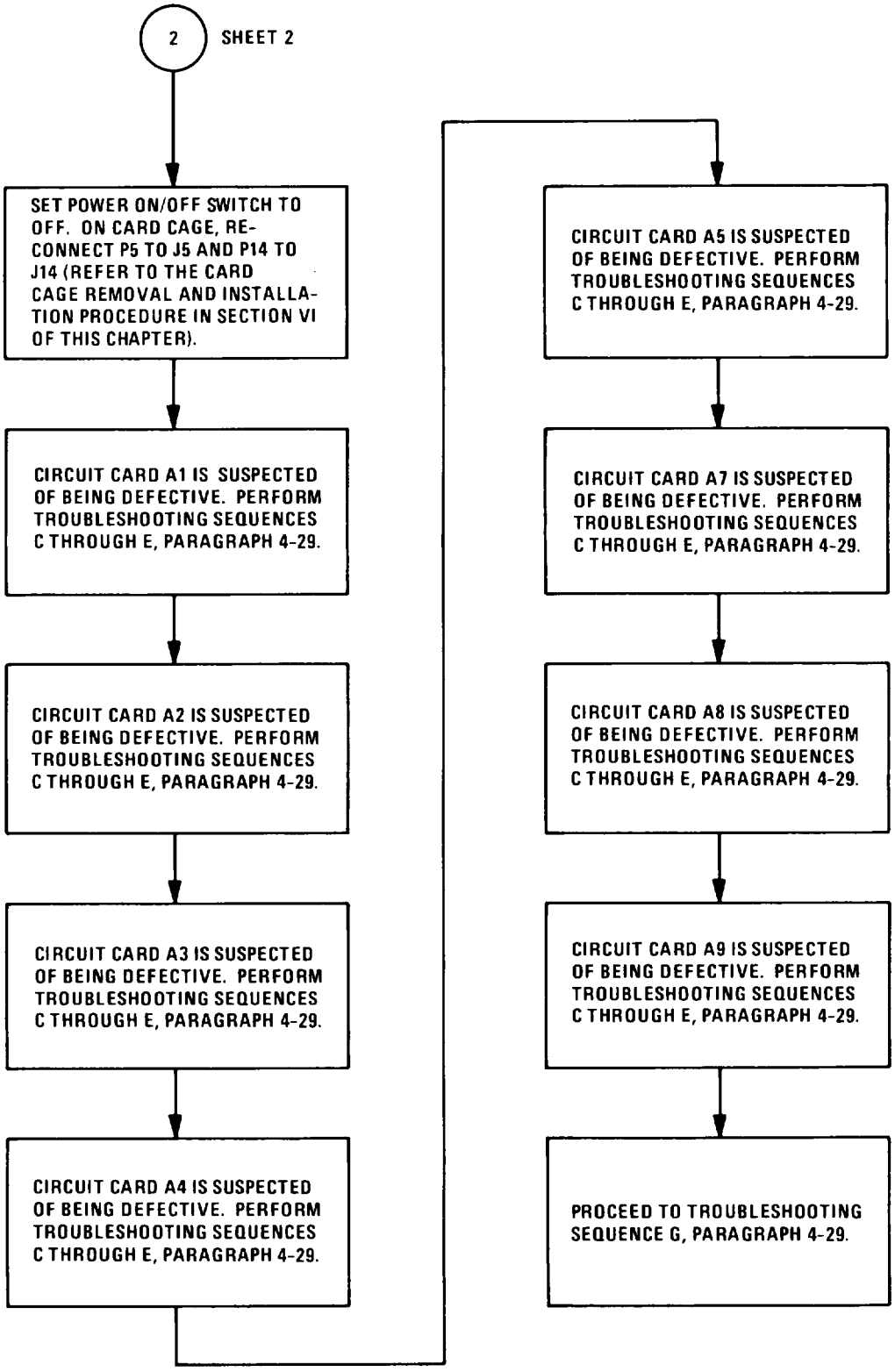
Troubleshooting Flow Chart - Entry Point D



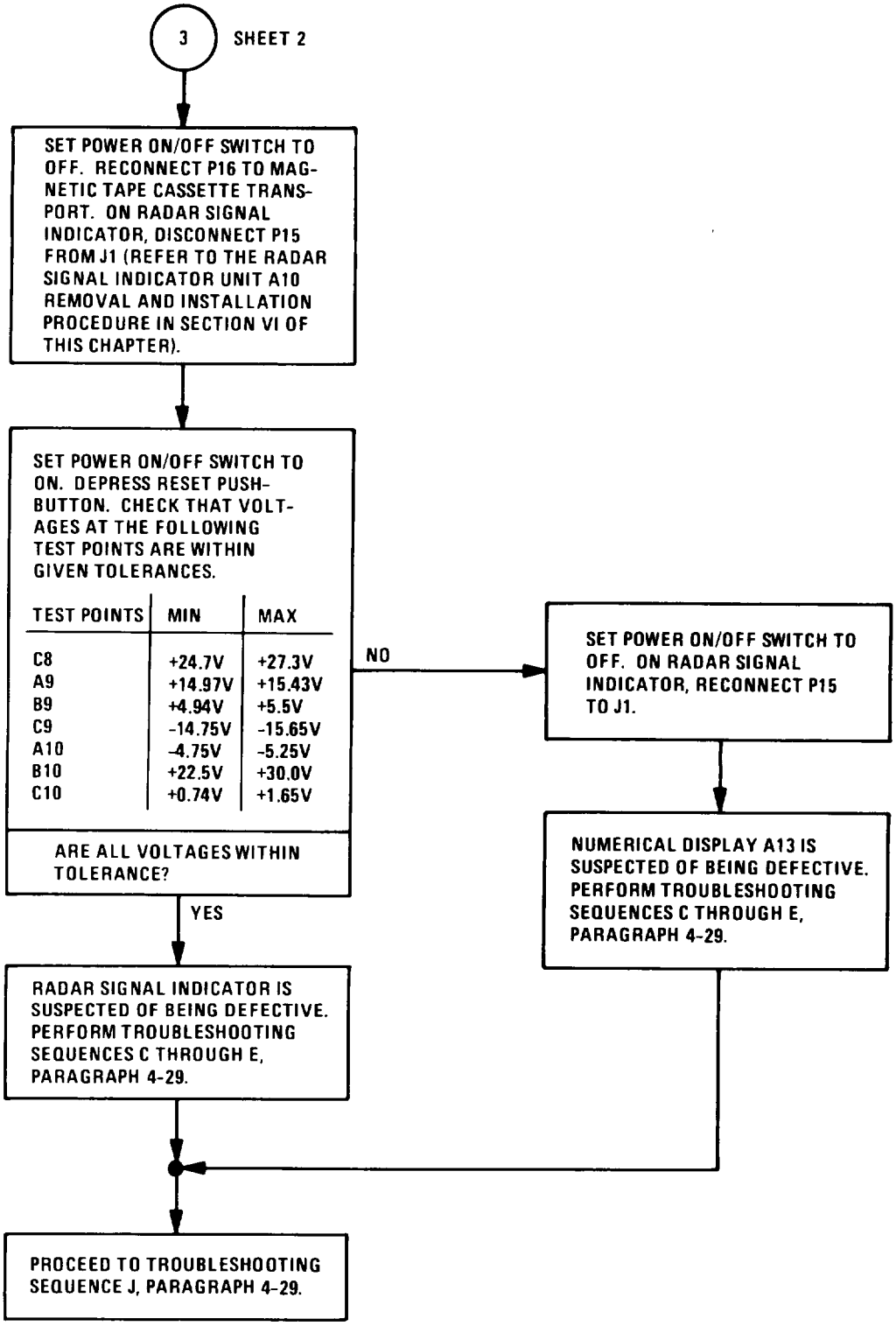
Troubleshooting Flow Chart - Entry Point E (Sheet 1 of 4)



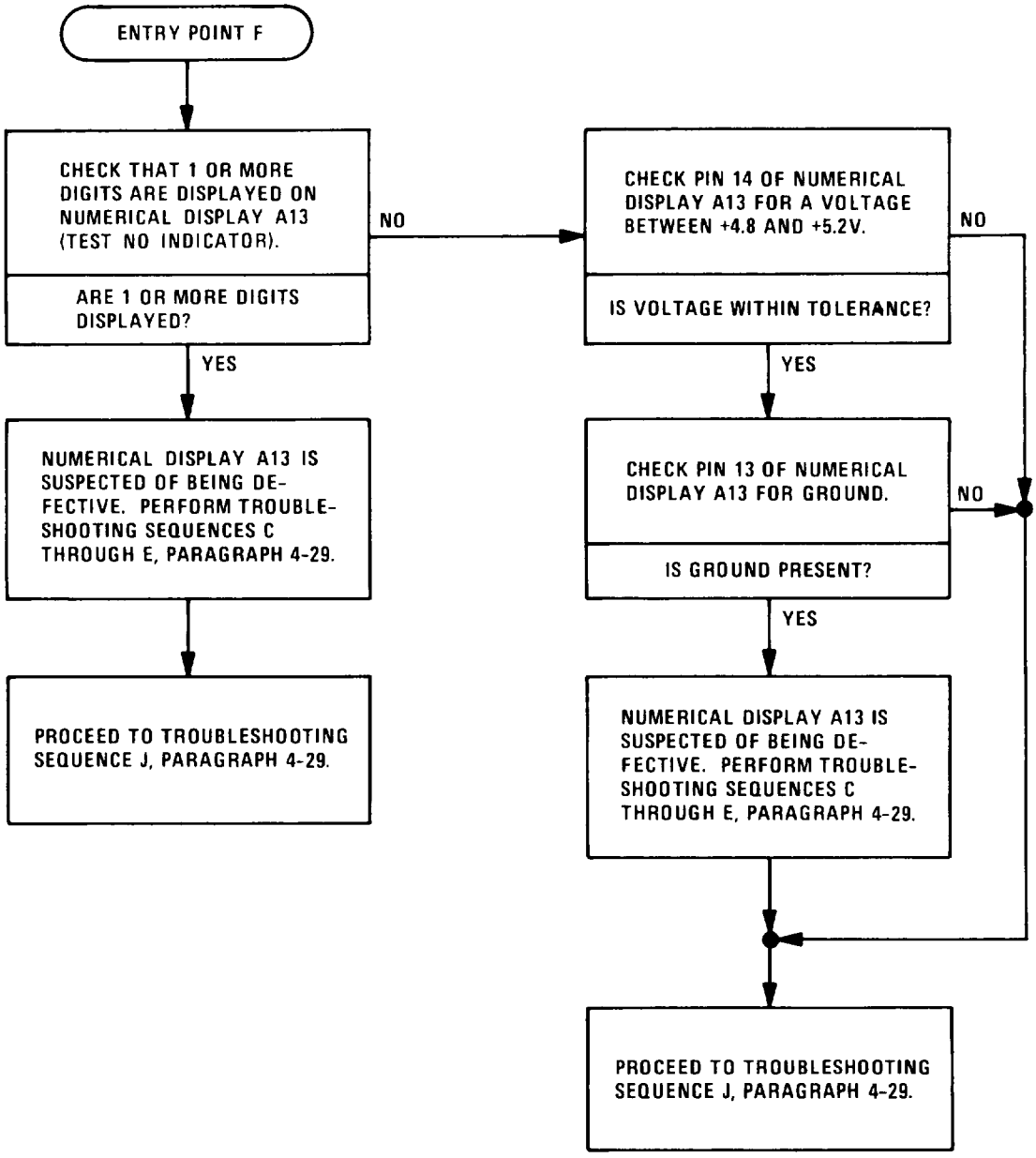
Troubleshooting Flow Chart - Entry Point E (Sheet 2 of 4)



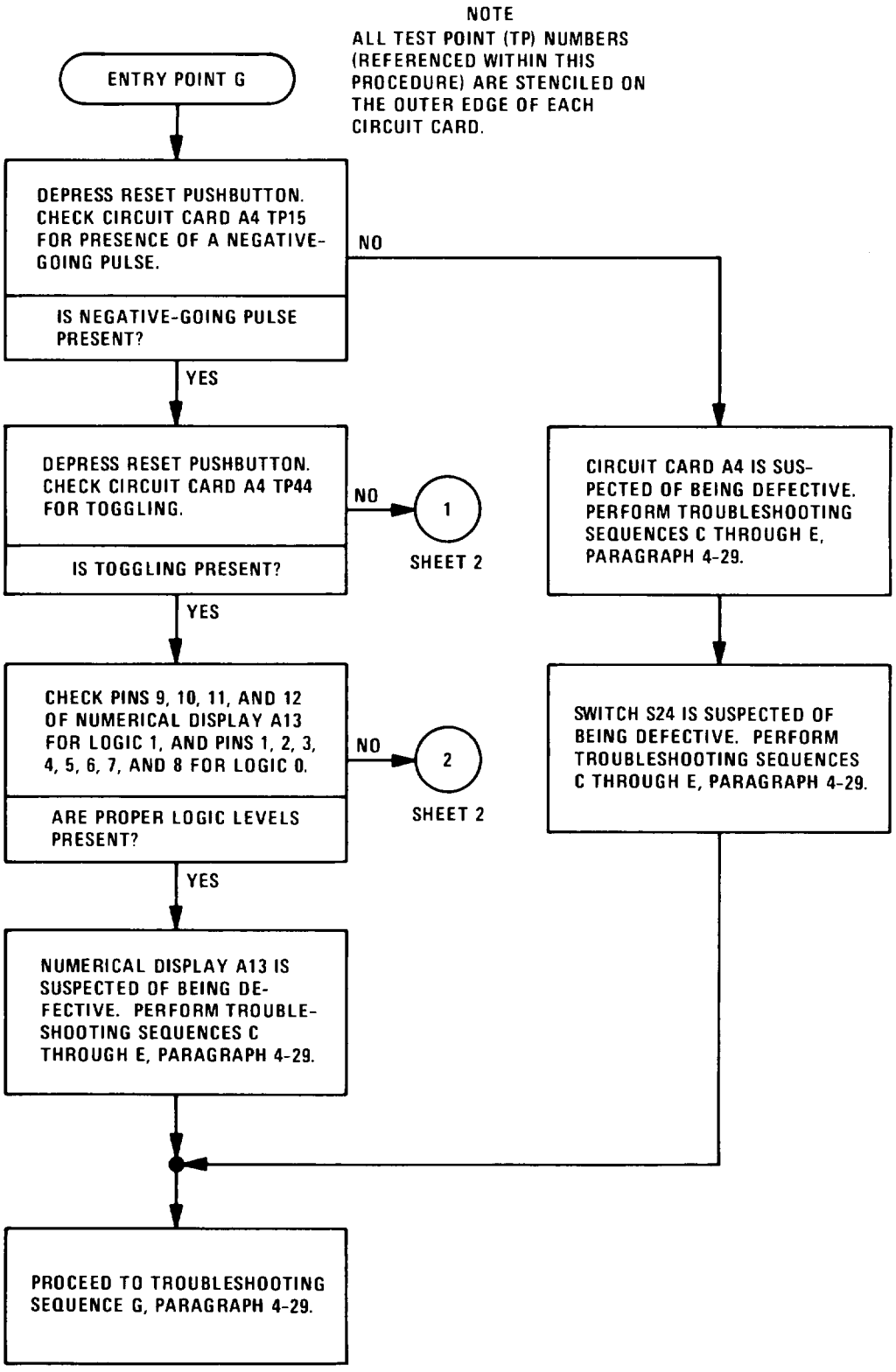
Troubleshooting Flow Chart - Entry Point E (Sheet 3 of 4)



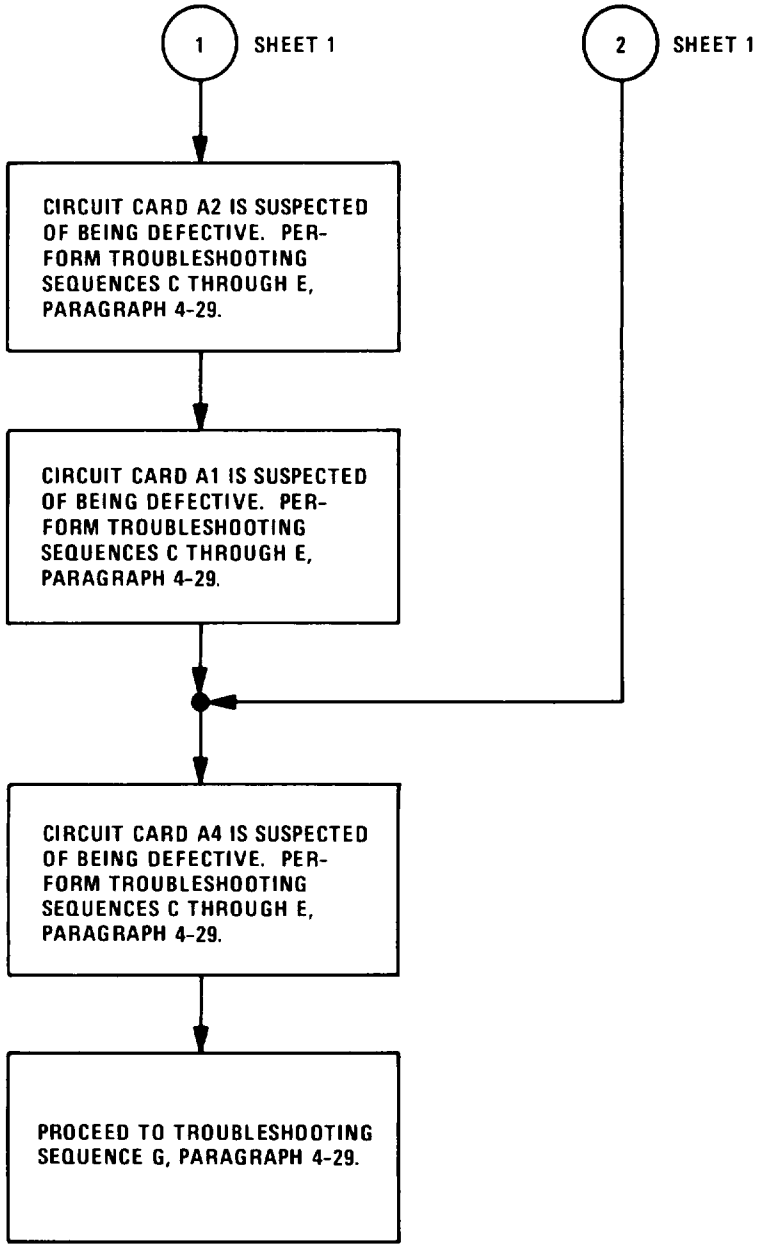
Troubleshooting Flow Chart - Entry Point E (Sheet 4 of 4)



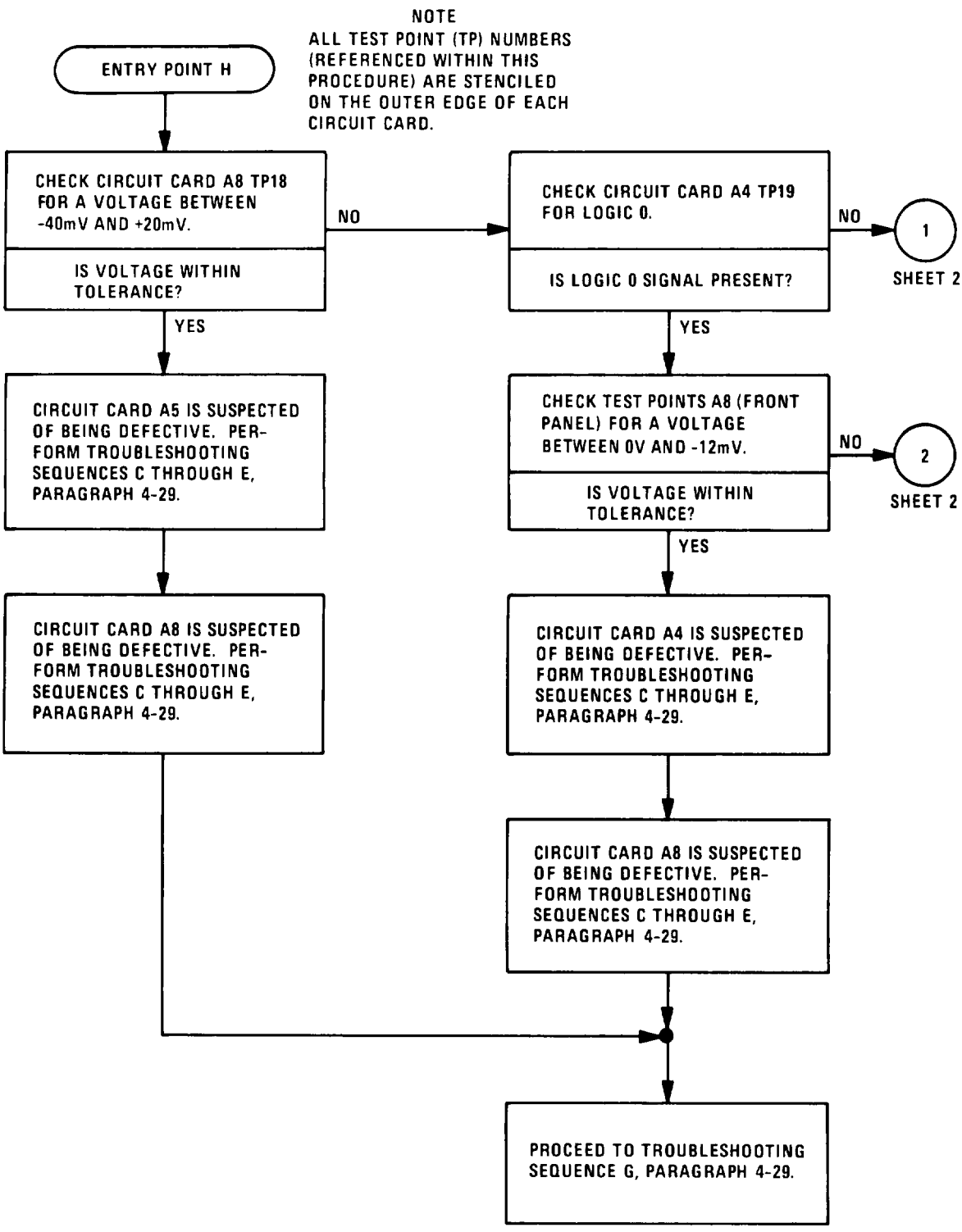
Troubleshooting Flow Chart - Entry Point F



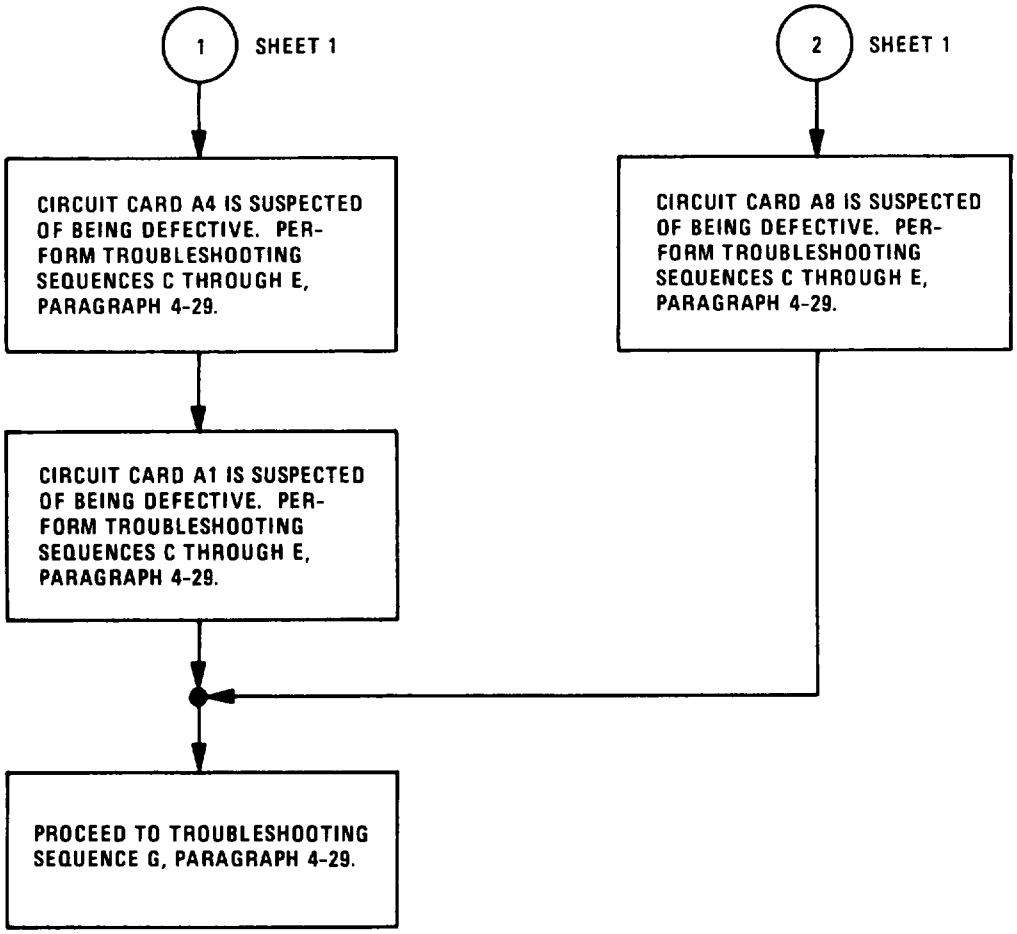
Troubleshooting Flow Chart - Entry Point G (Sheet 1 of 2)



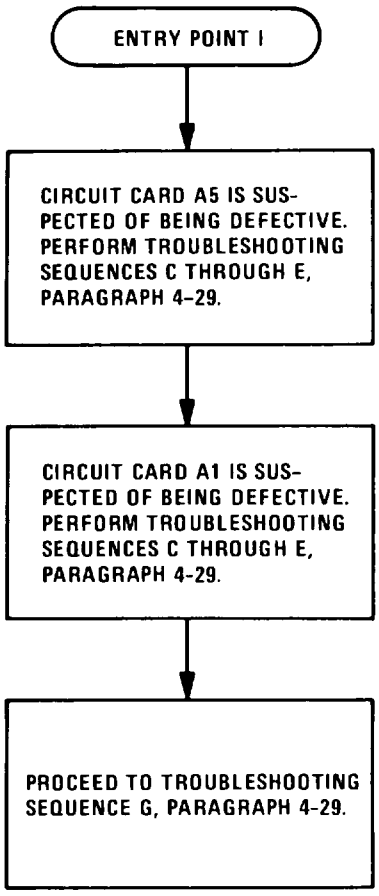
Troubleshooting Flow Chart - Entry Point G (Sheet 2 of 2)



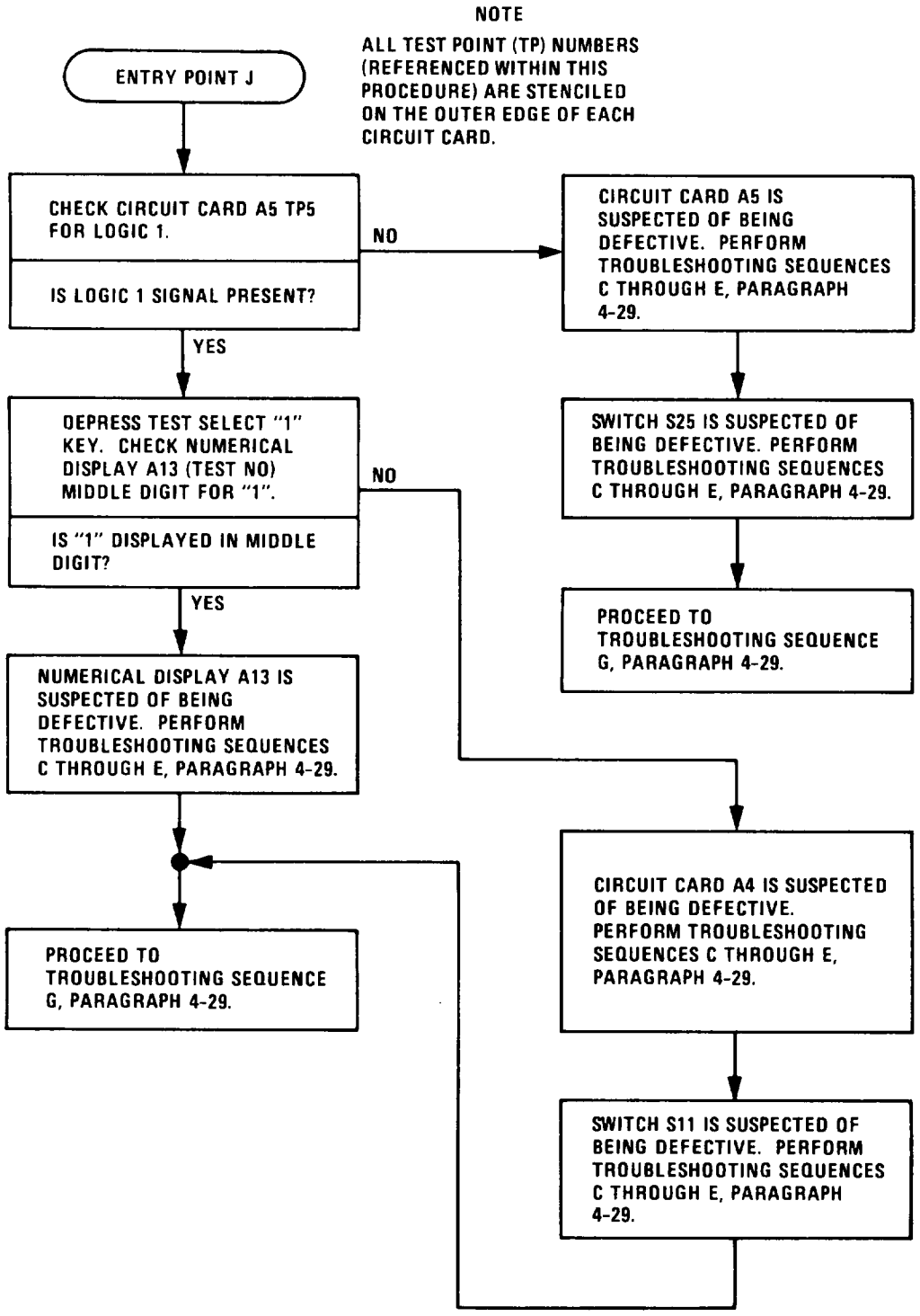
Troubleshooting Flow Chart - Entry Point H (Sheet 1 of 2)



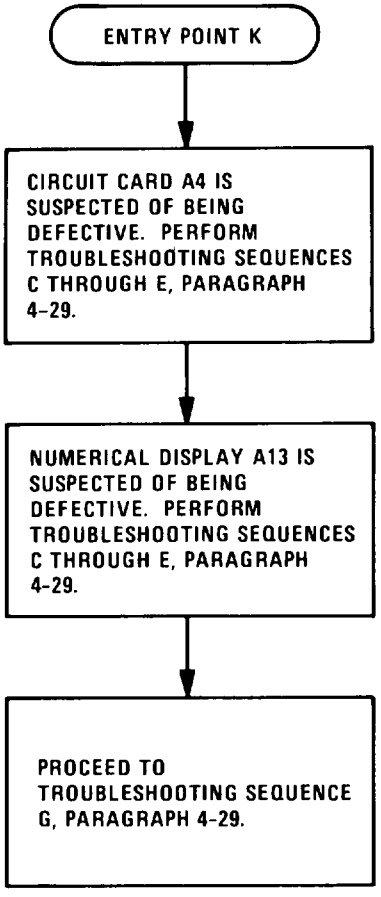
Troubleshooting Flow Chart - Entry Point H (Sheet 2 of 2)



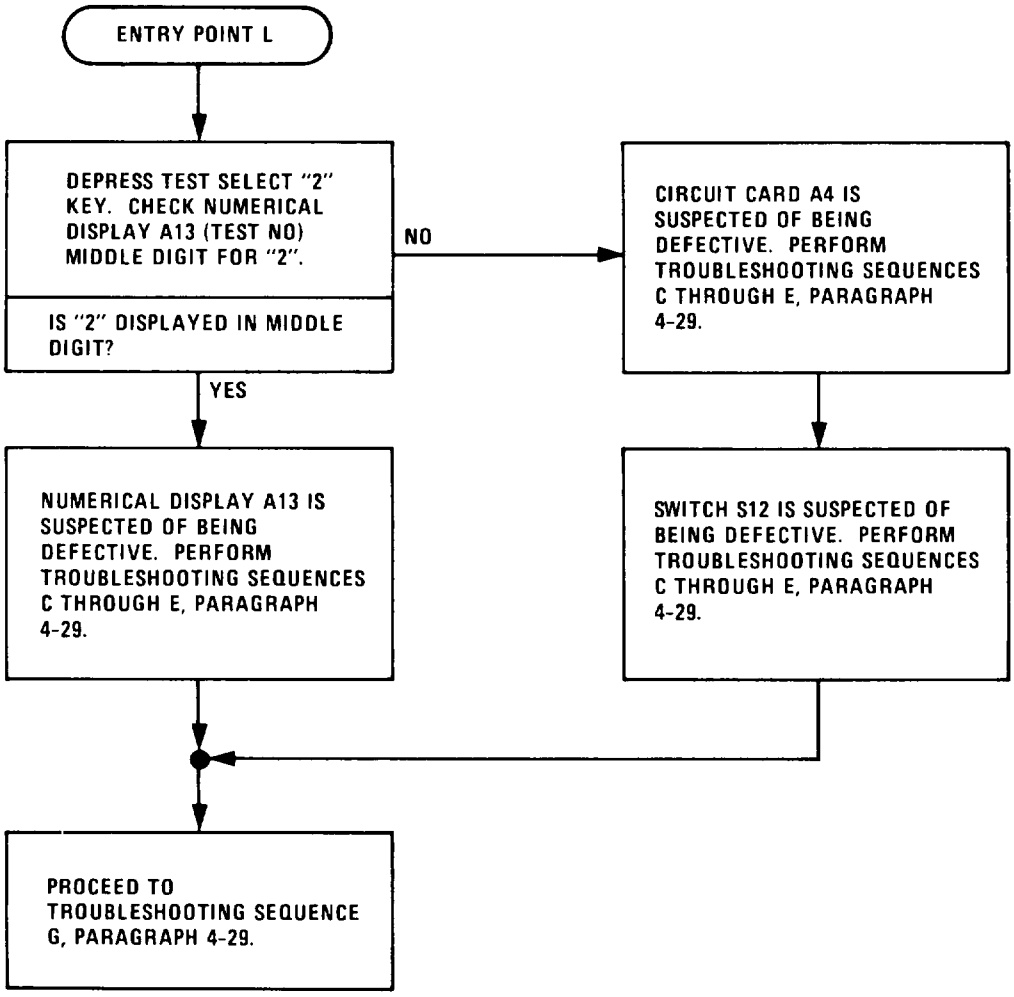
Troubleshooting Flow Chart - Entry Point I



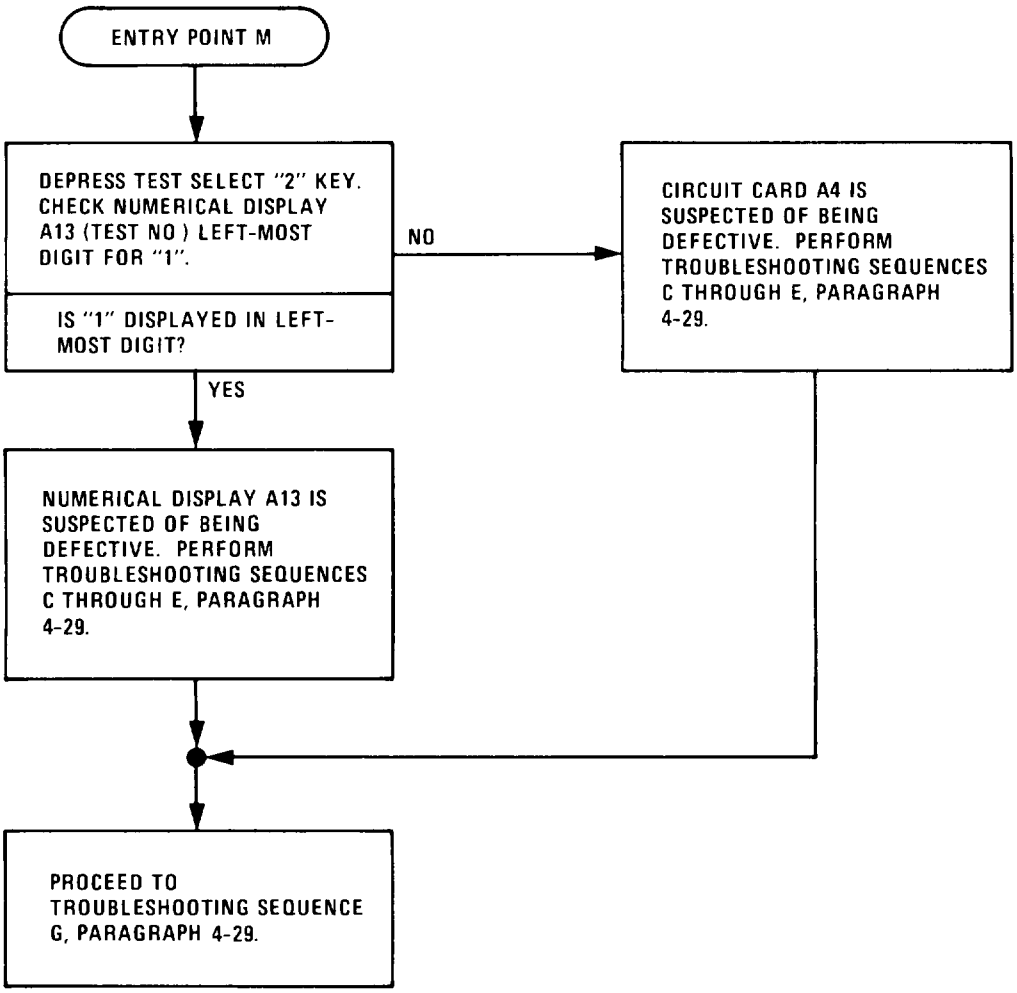
Troubleshooting Flow Chart - Entry Point J



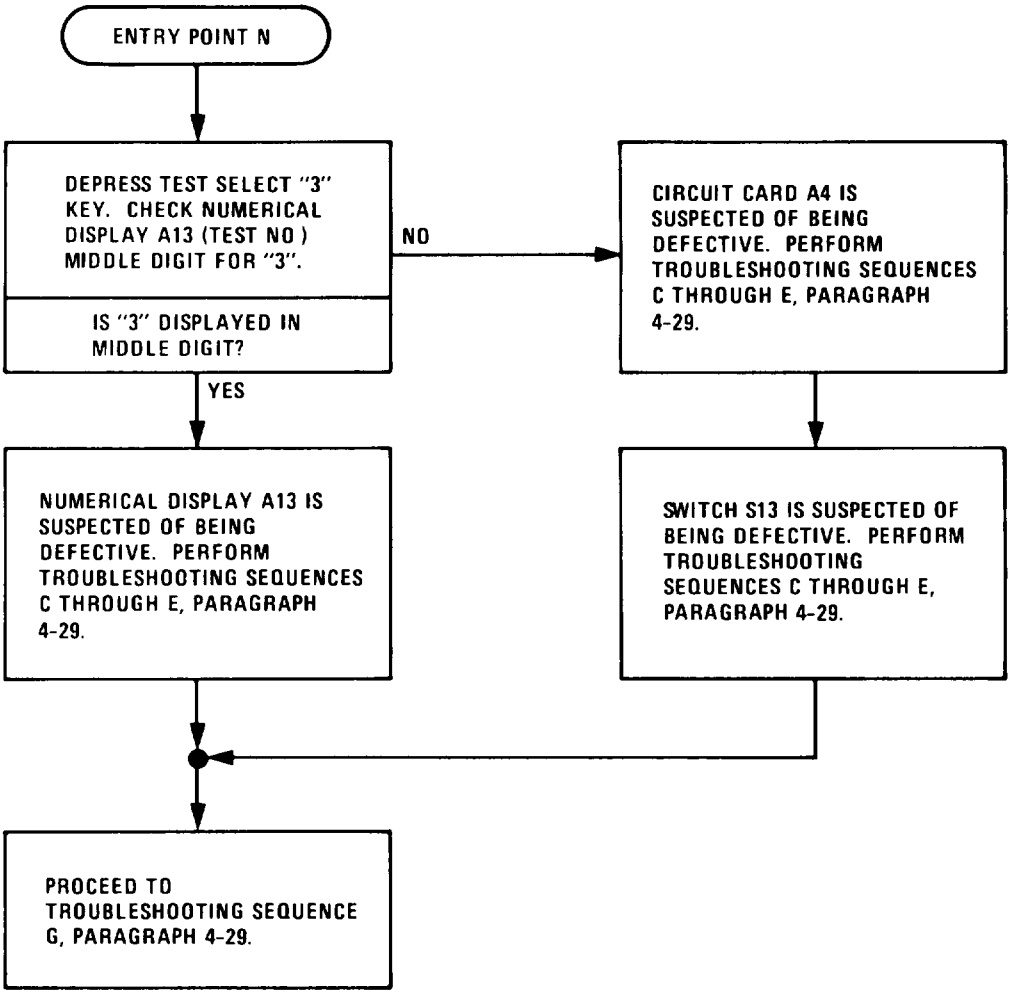
Troubleshooting Flow Chart - Entry Point K



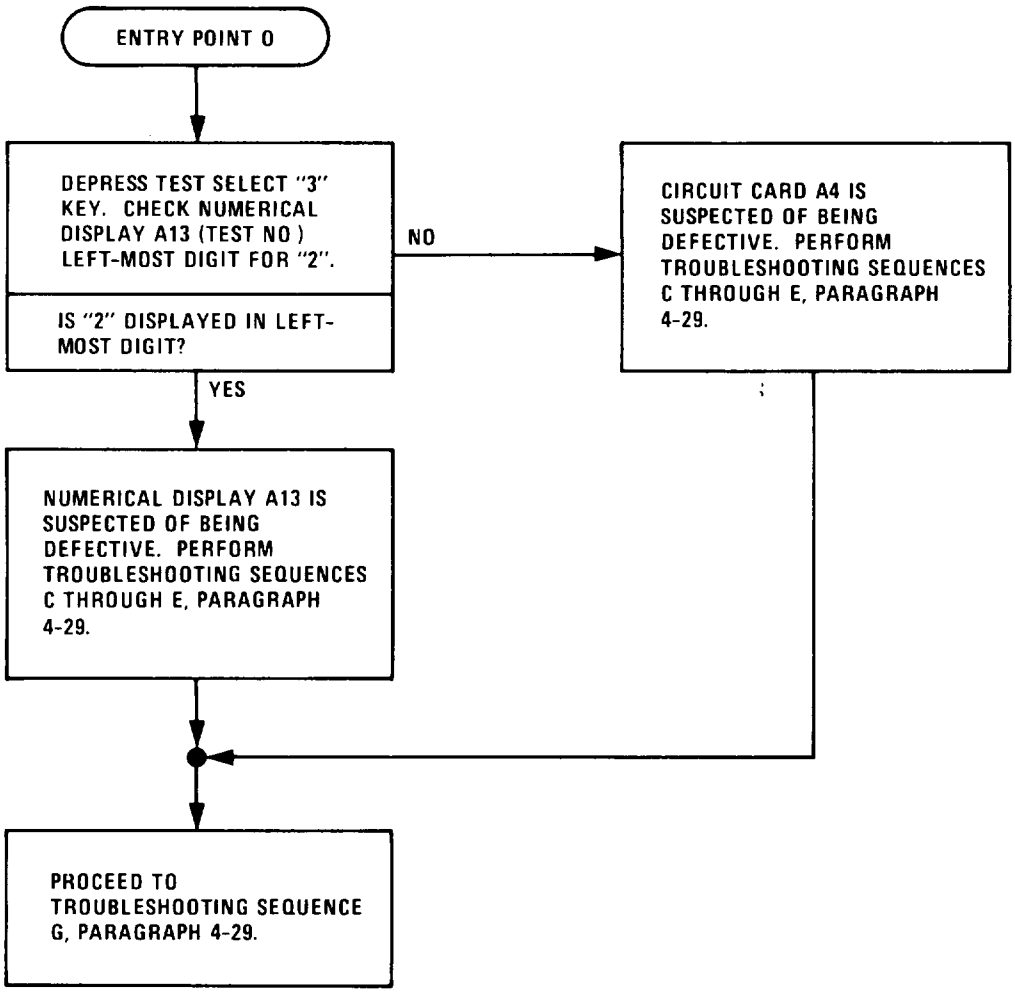
Troubleshooting Flow Chart - Entry Point L



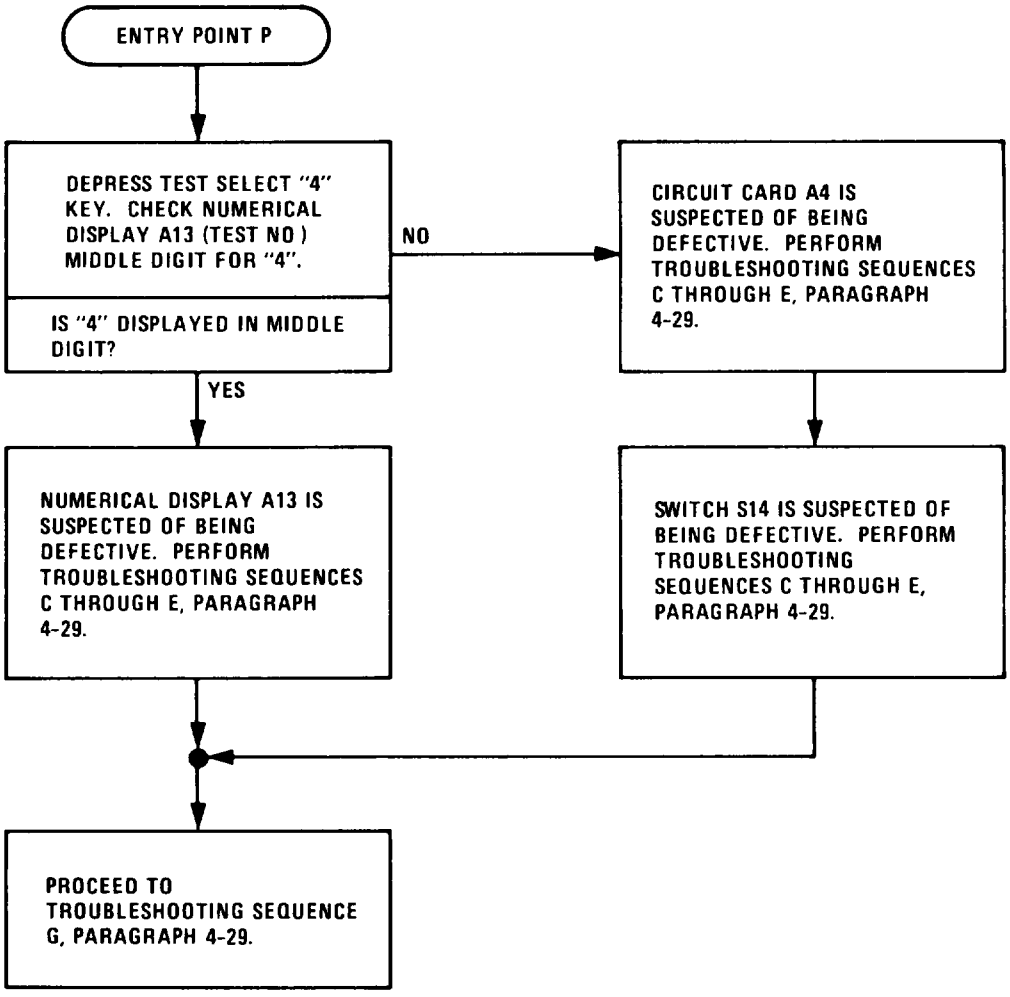
Troubleshooting Flow Chart - Entry Point M



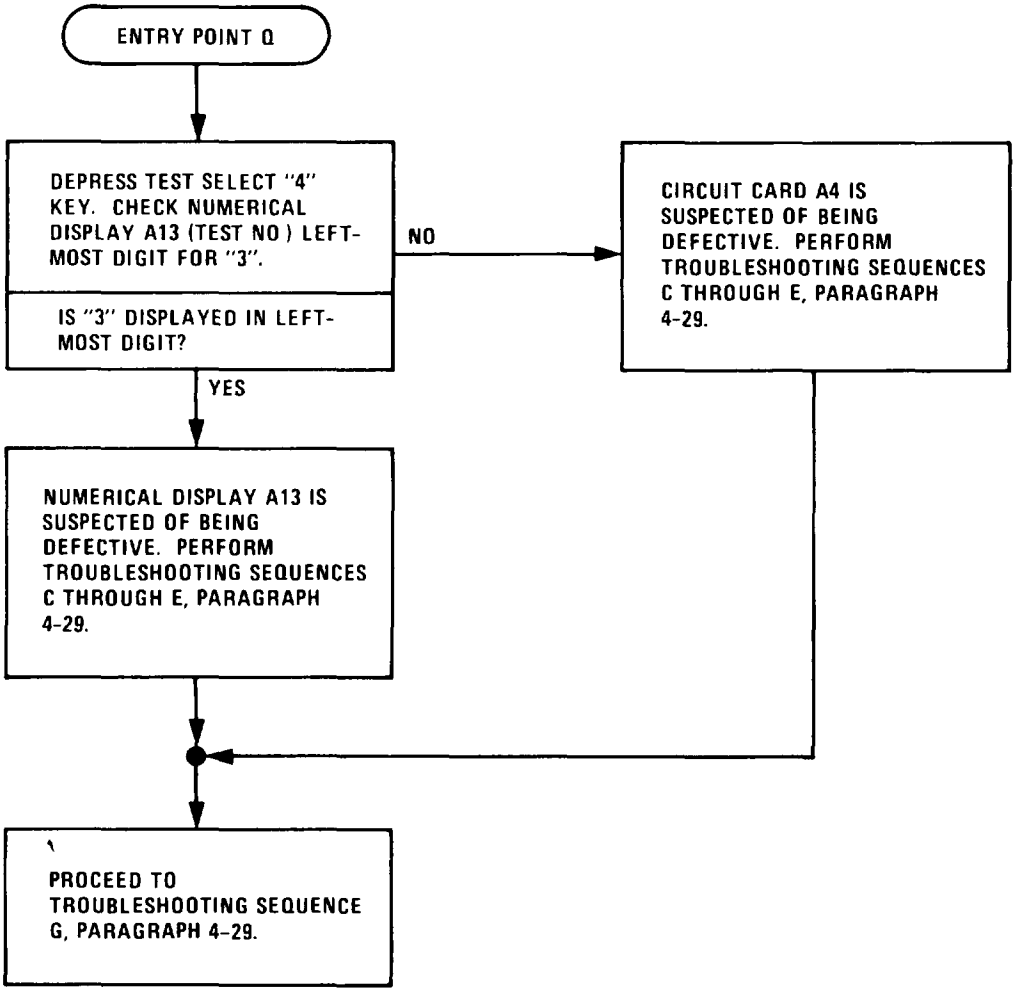
Troubleshooting Flow Chart - Entry Point N



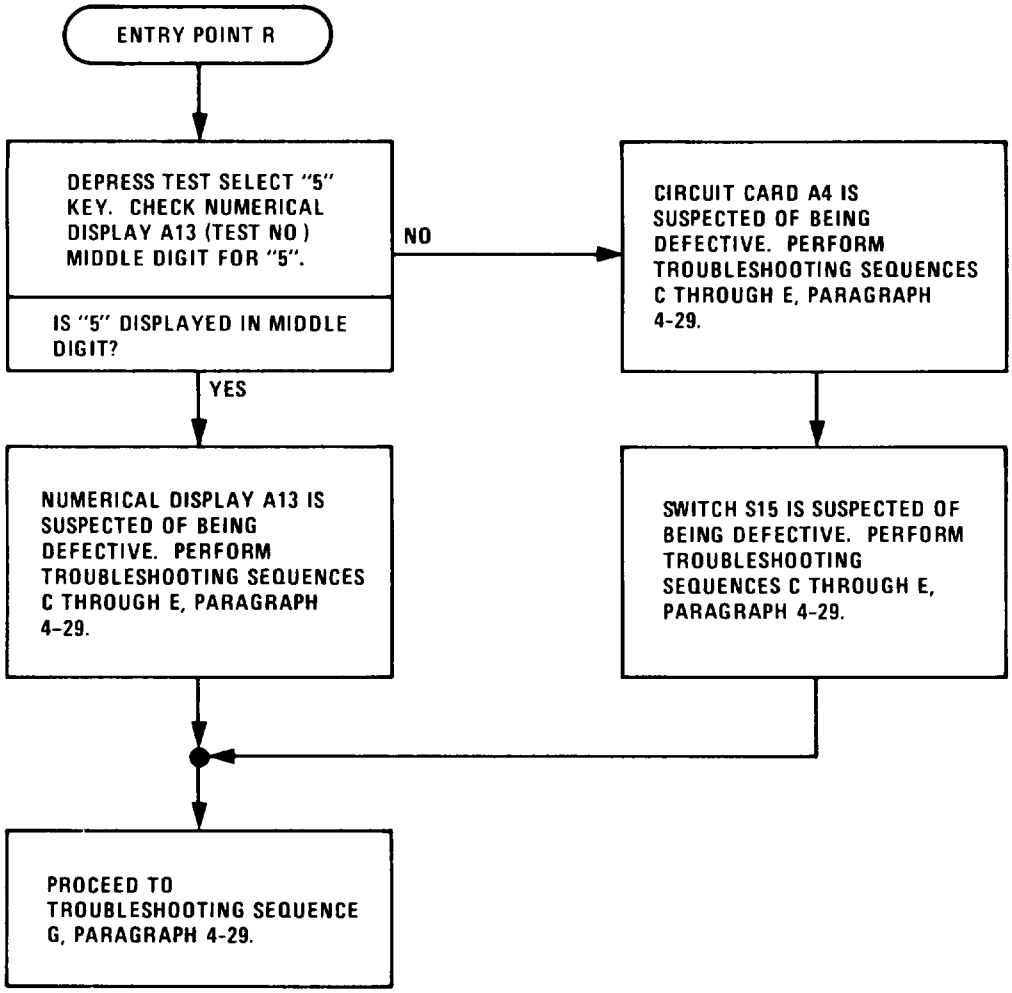
Troubleshooting Flow Chart - Entry Point O



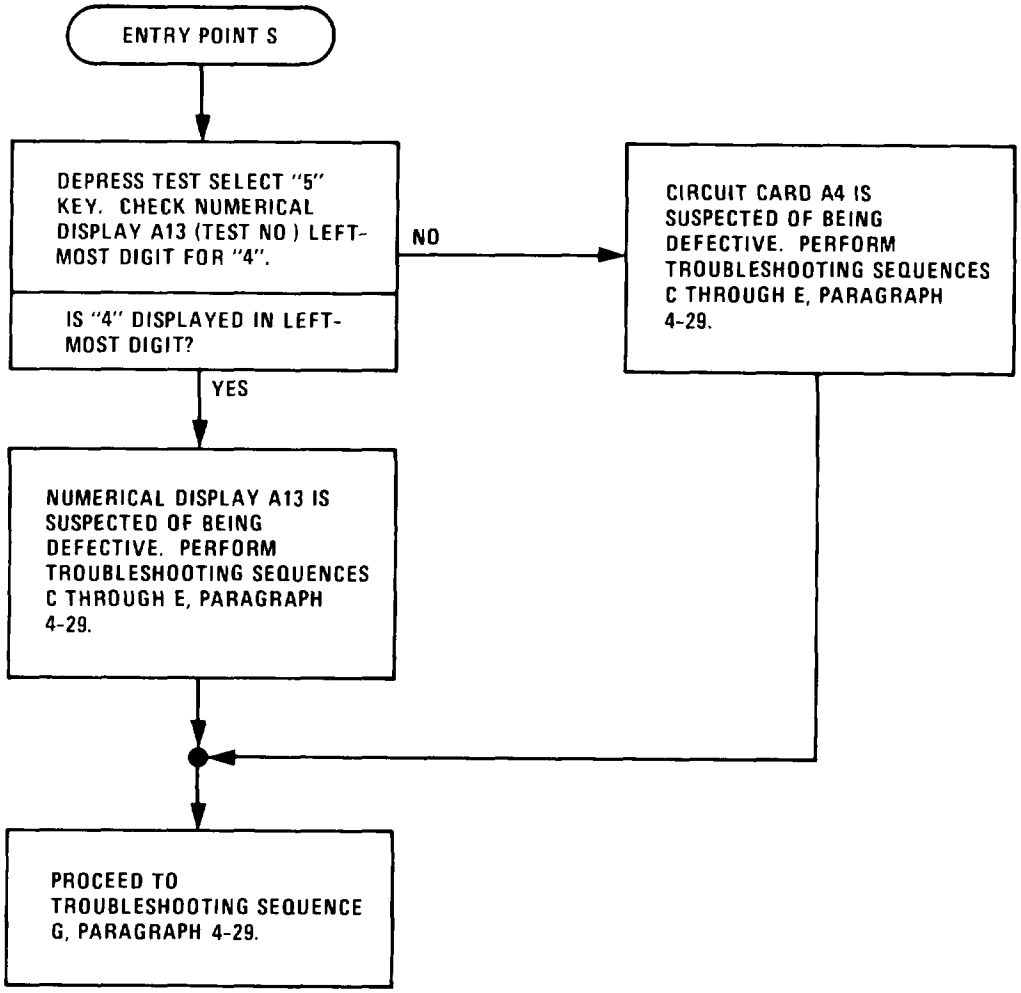
Troubleshooting Flow Chart - Entry Point P



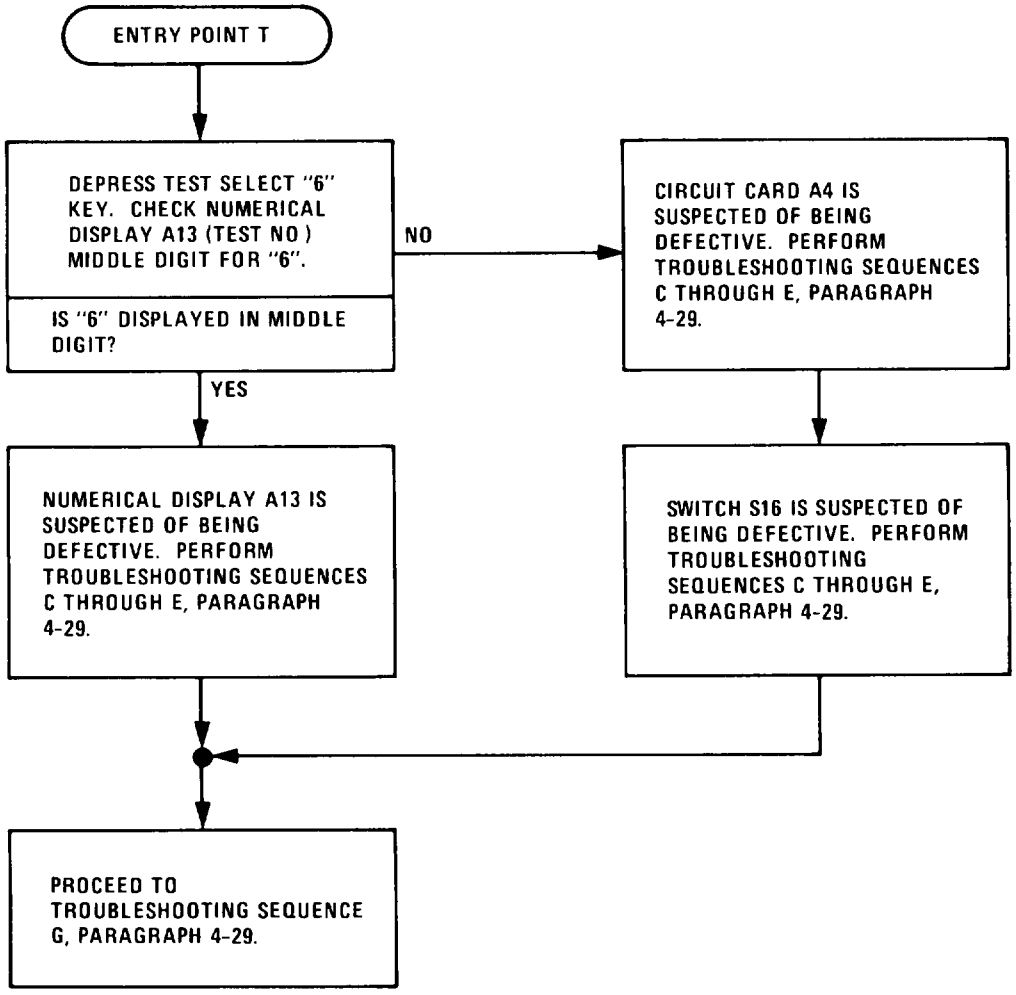
Troubleshooting Flow Chart - Entry Point Q



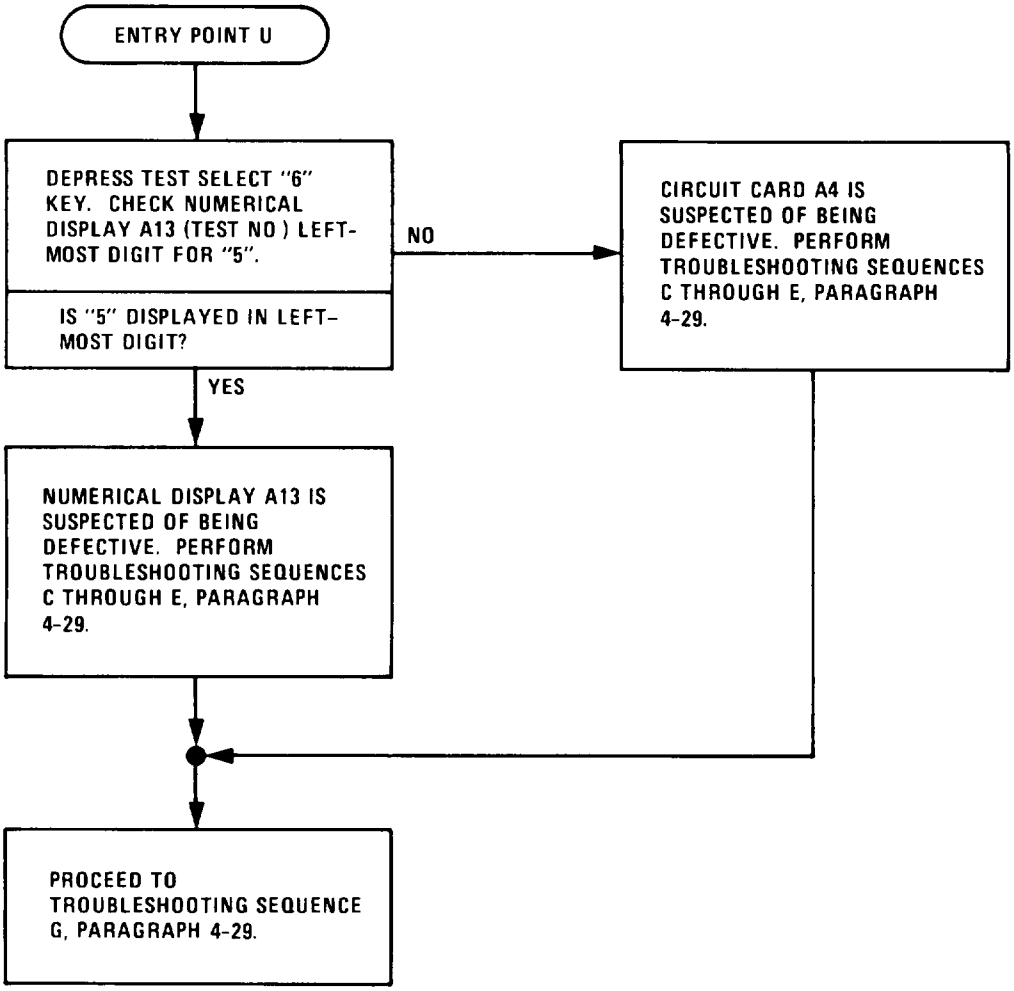
Troubleshooting Flow Chart - Entry Point R



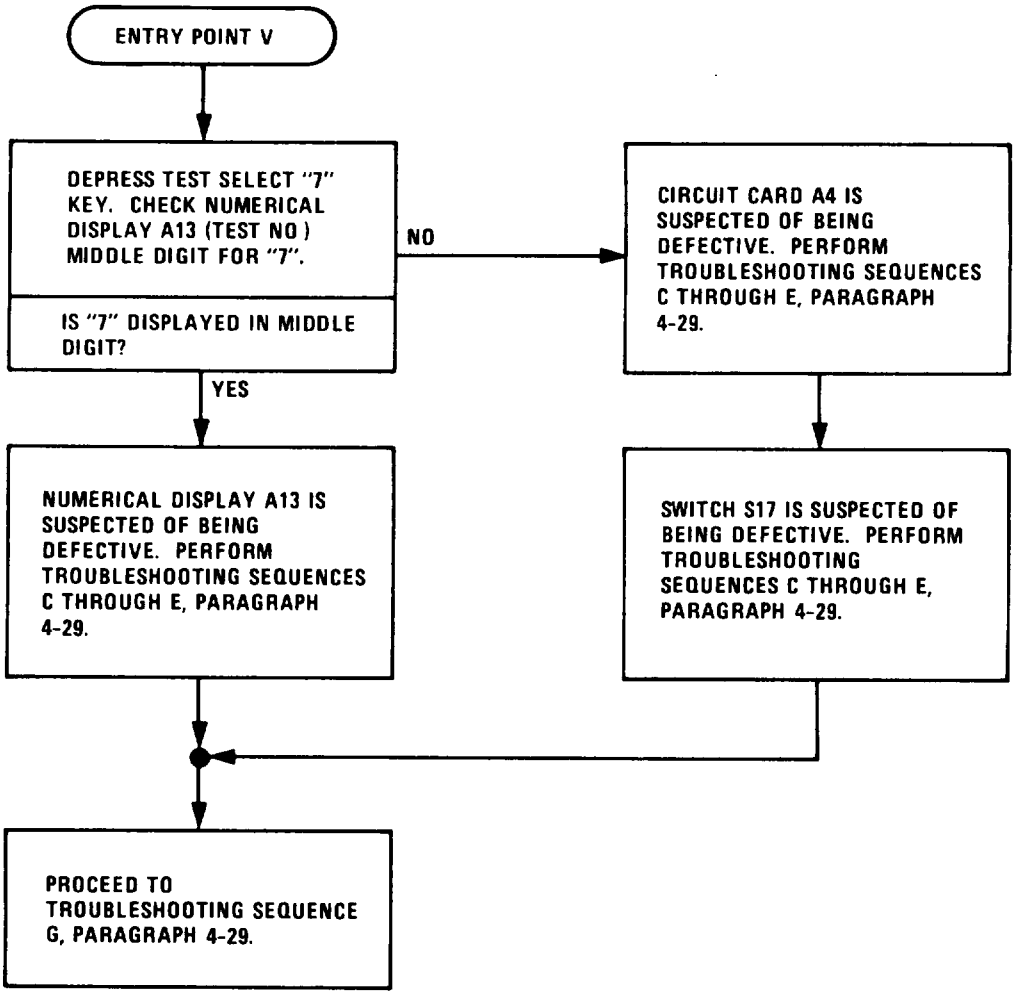
Troubleshooting Flow Chart - Entry Point S



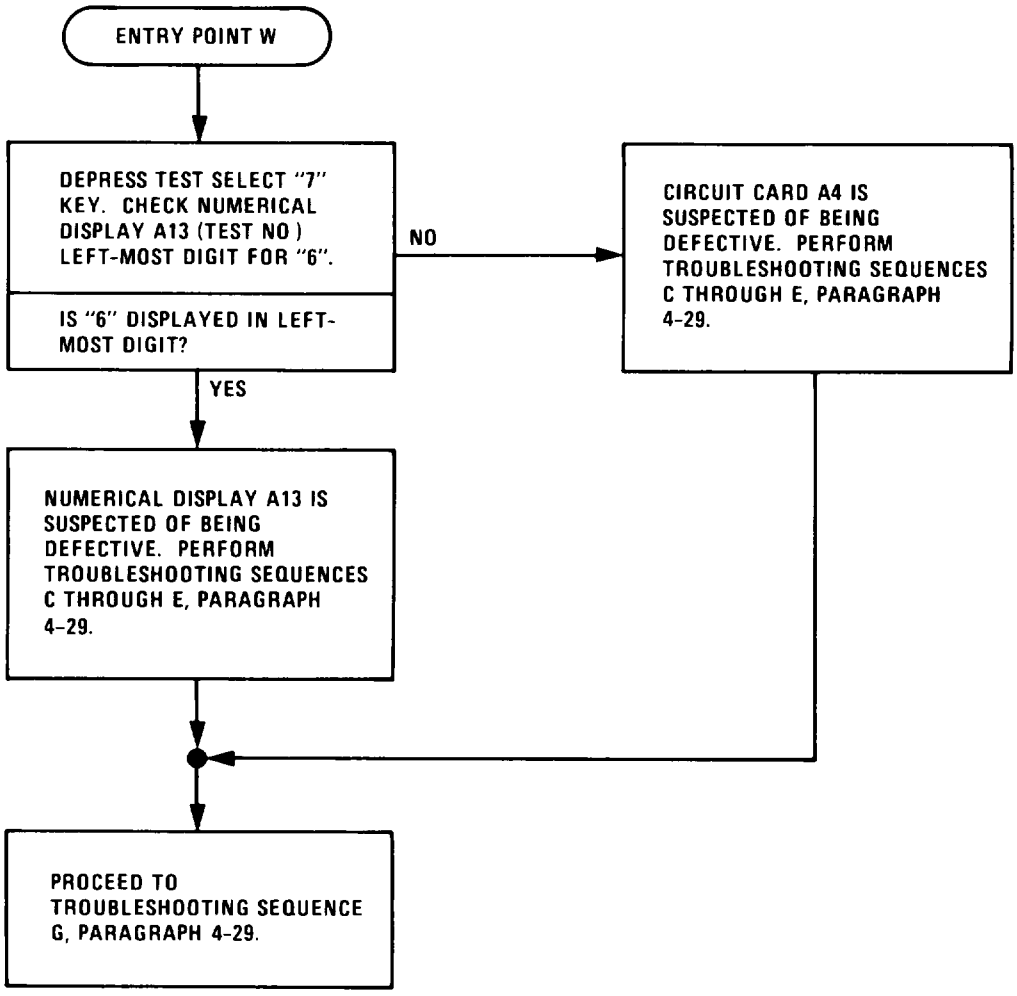
Troubleshooting Flow Chart - Entry Point T



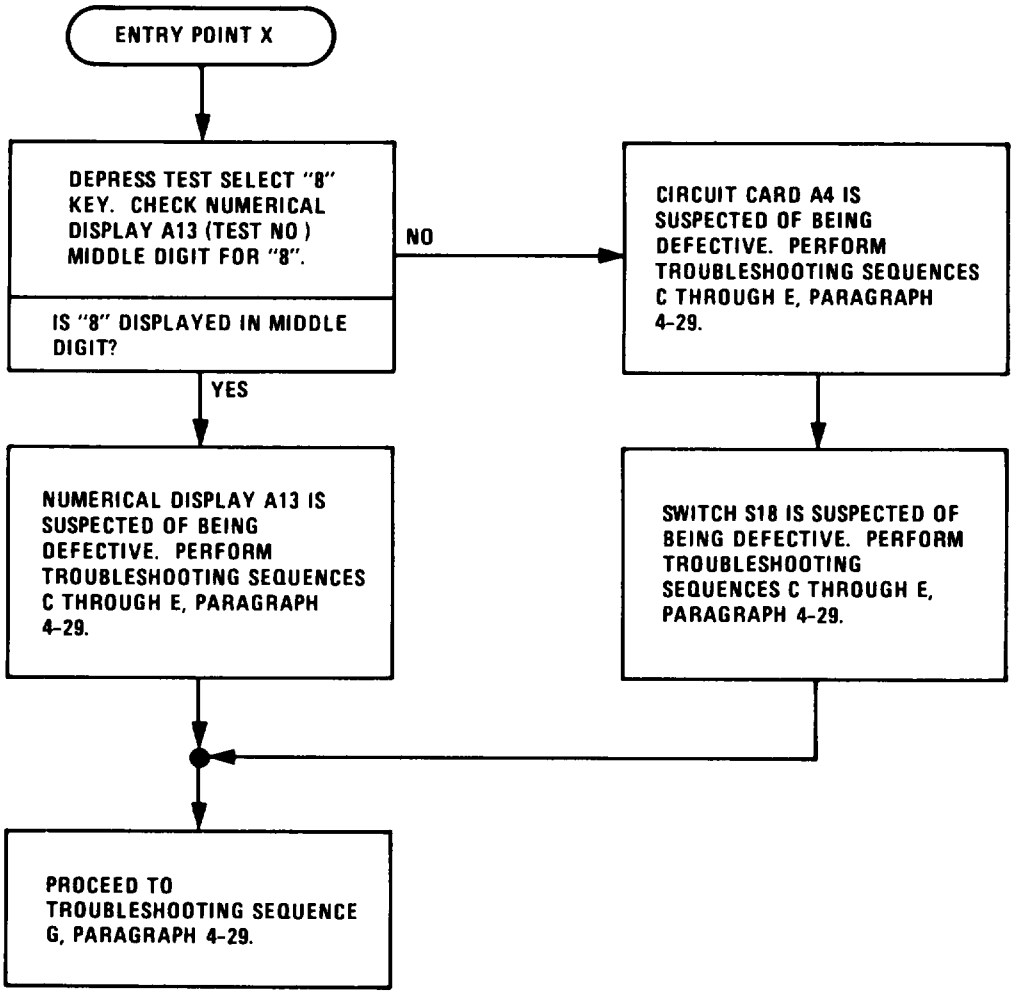
Troubleshooting Flow Chart - Entry Point U



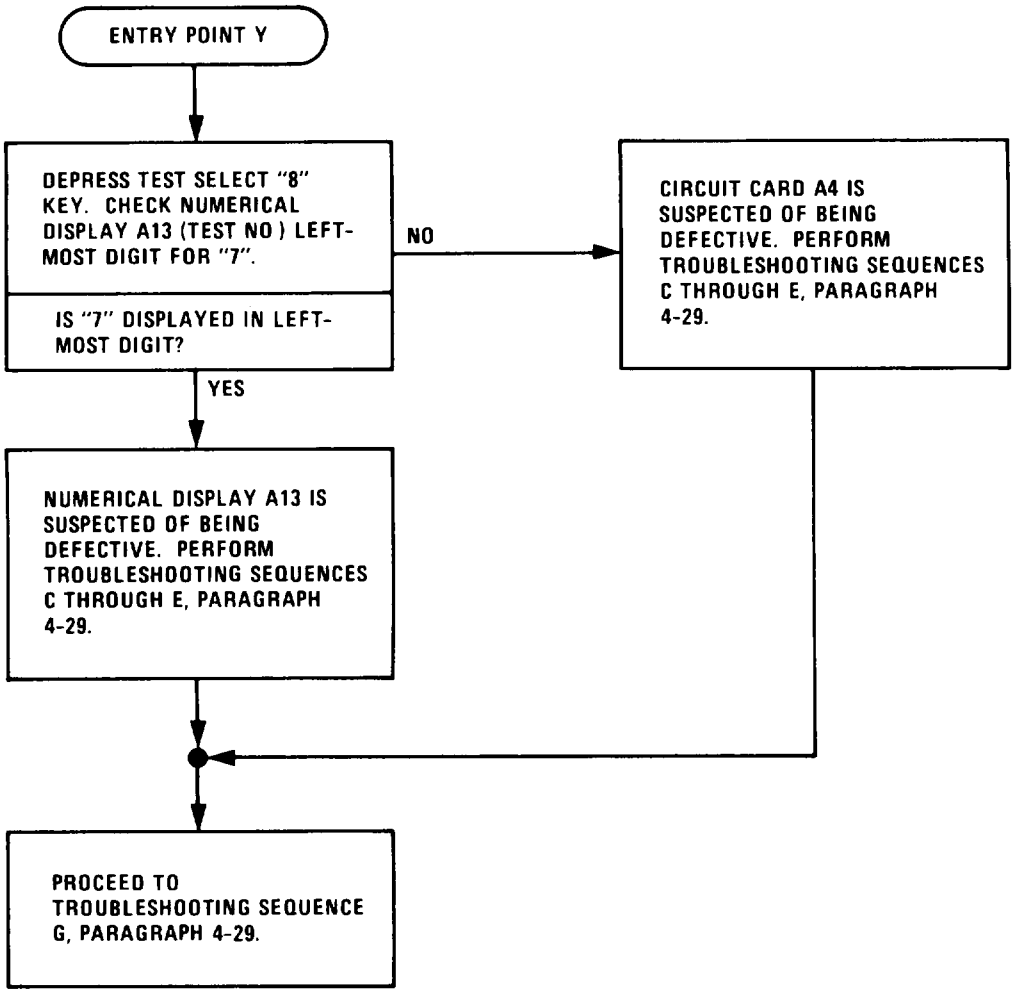
Troubleshooting Flow Chart - Entry Point V



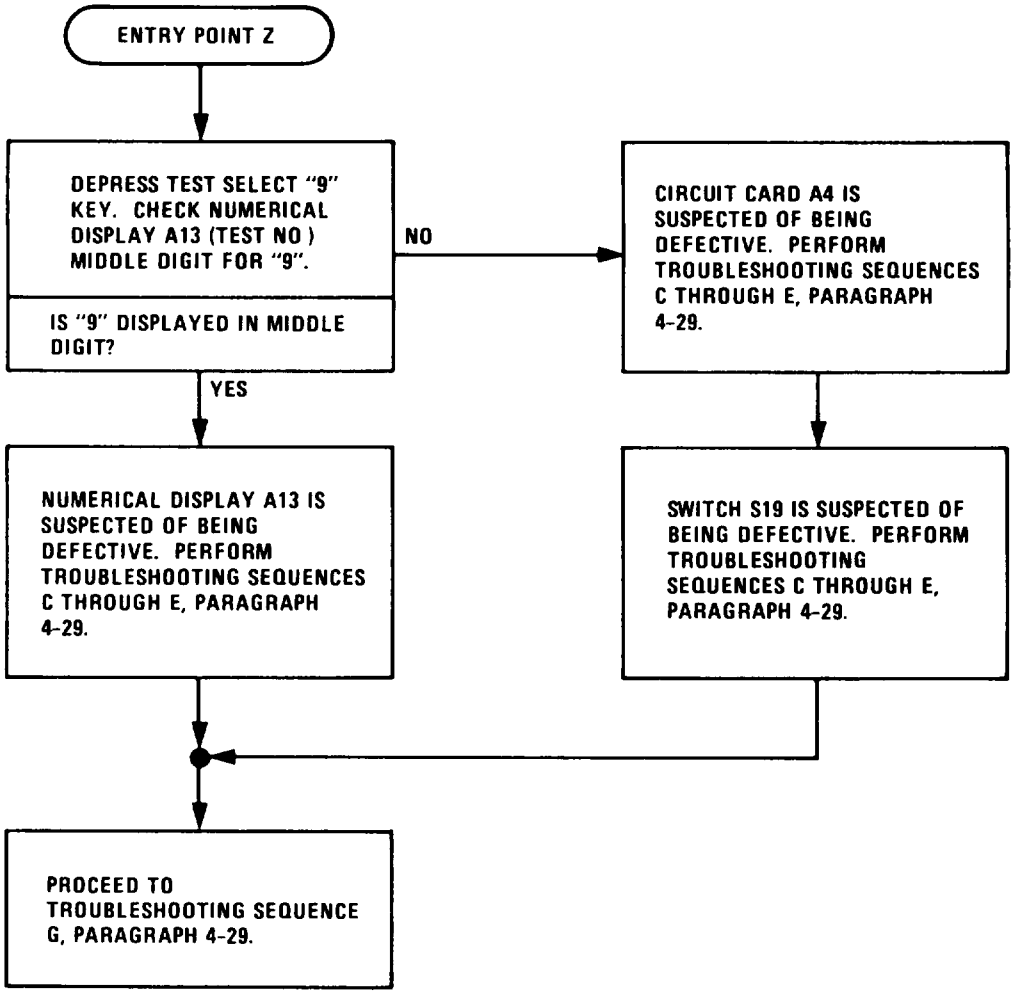
Troubleshooting Flow Chart - Entry Point W



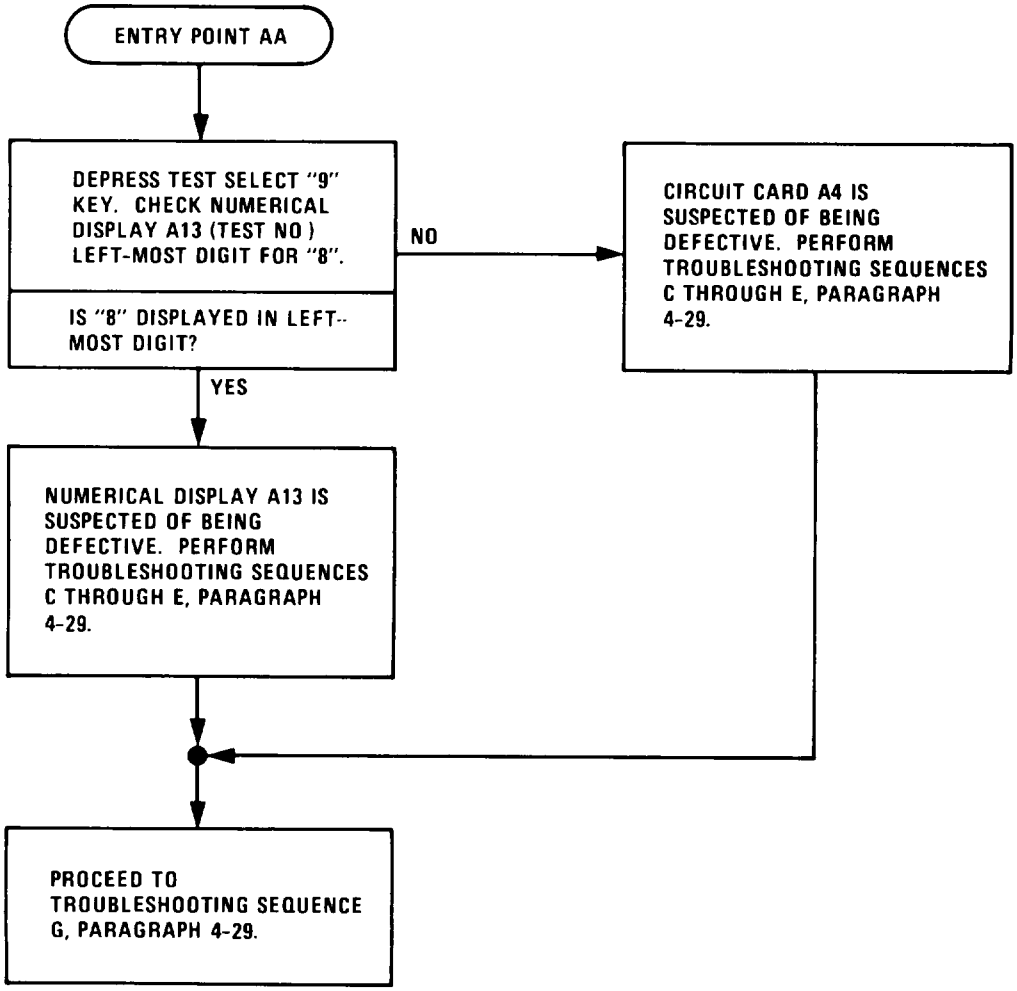
Troubleshooting Flow Chart - Entry Point X



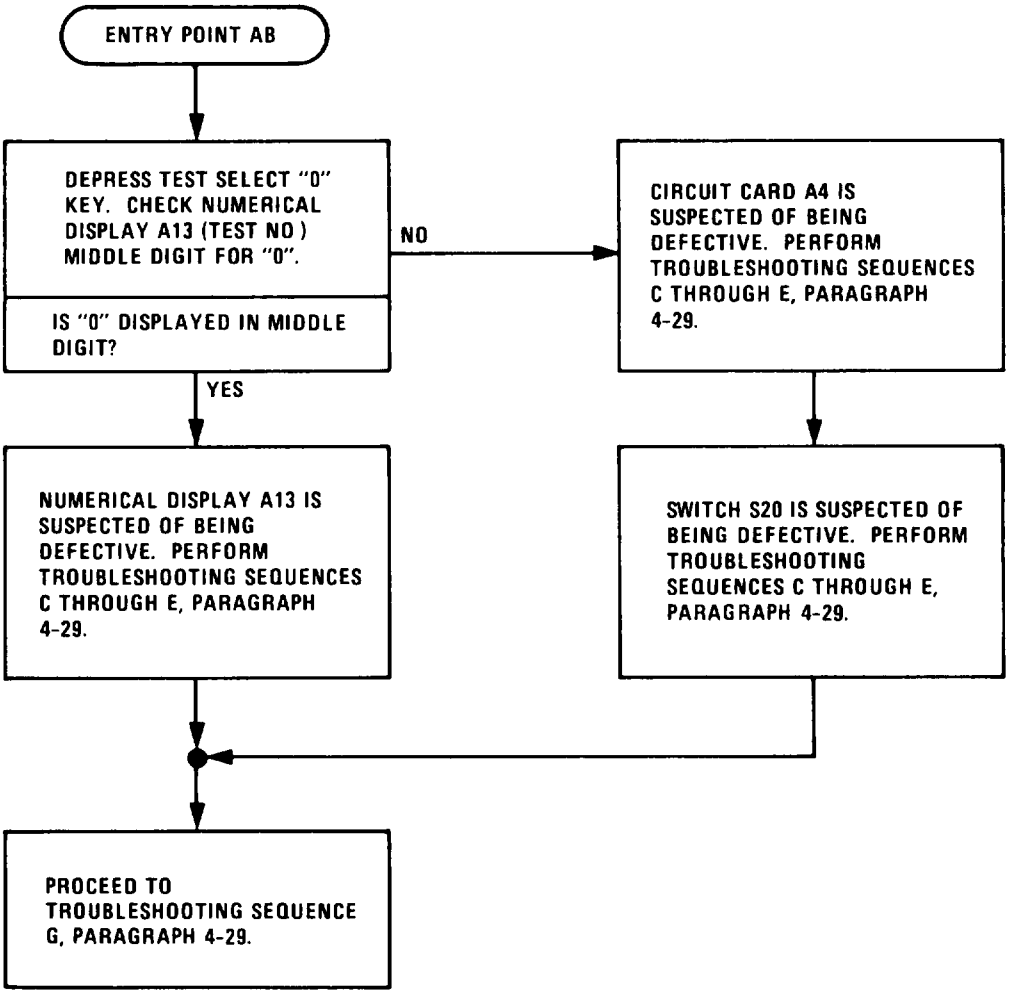
Troubleshooting Flow Chart - Entry Point Y



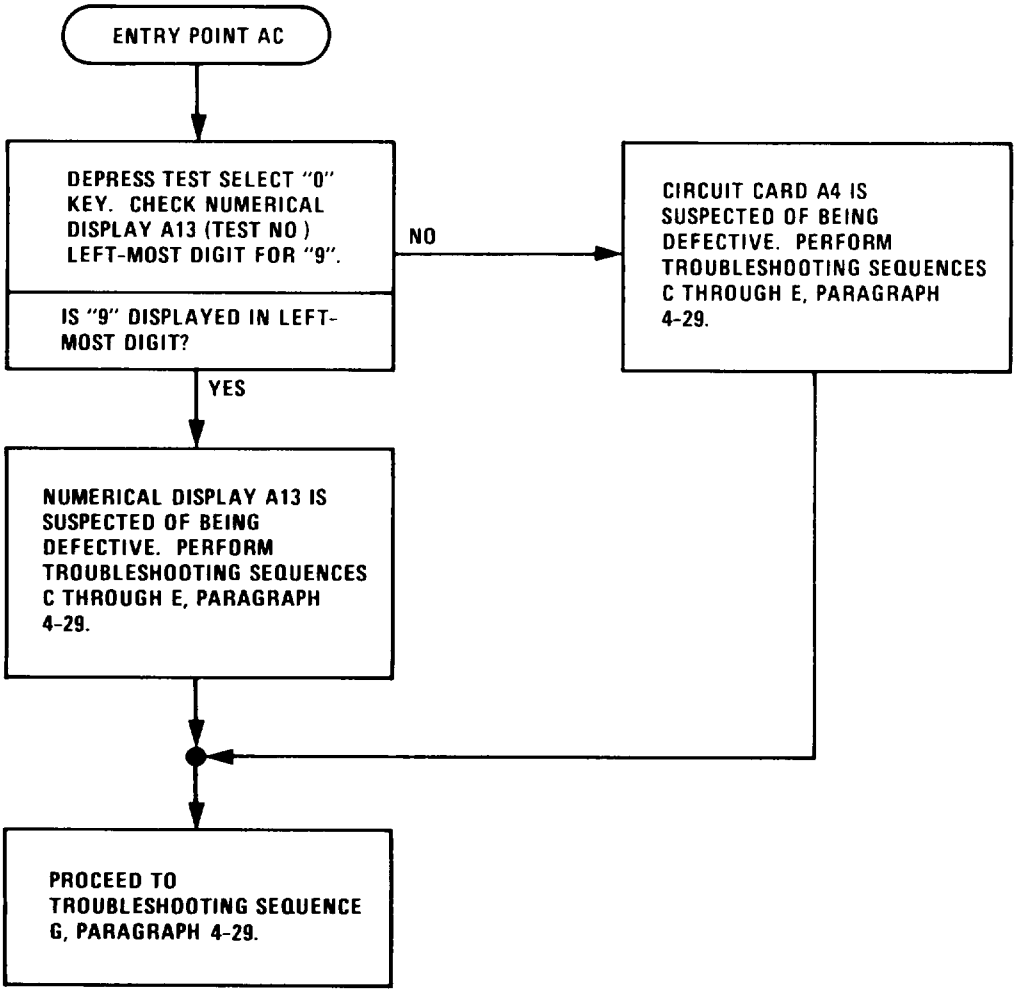
Troubleshooting Flow Chart - Entry Point Z



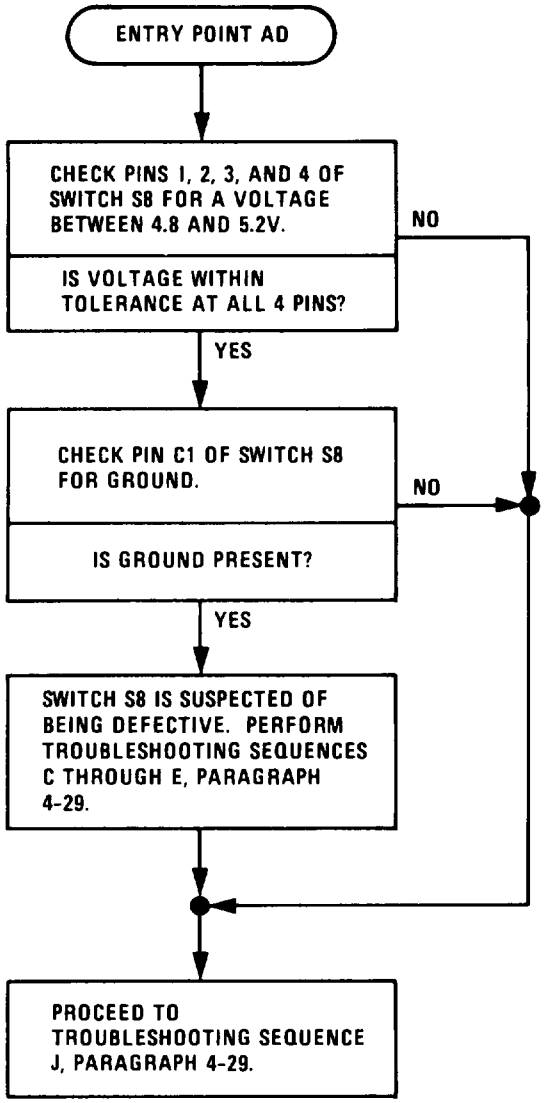
Troubleshooting Flow Chart - Entry Point AA



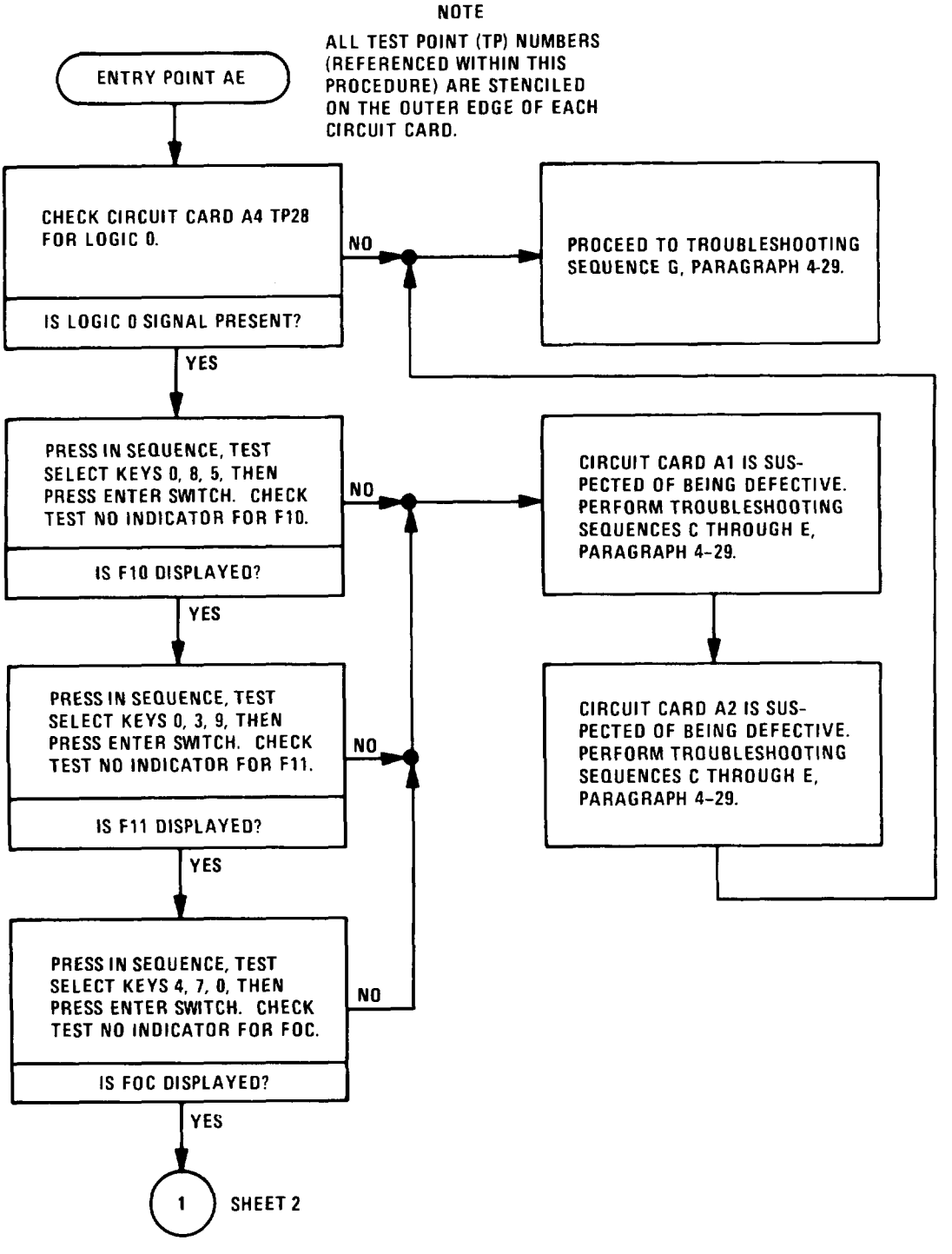
Troubleshooting Flow Chart - Entry Point AB



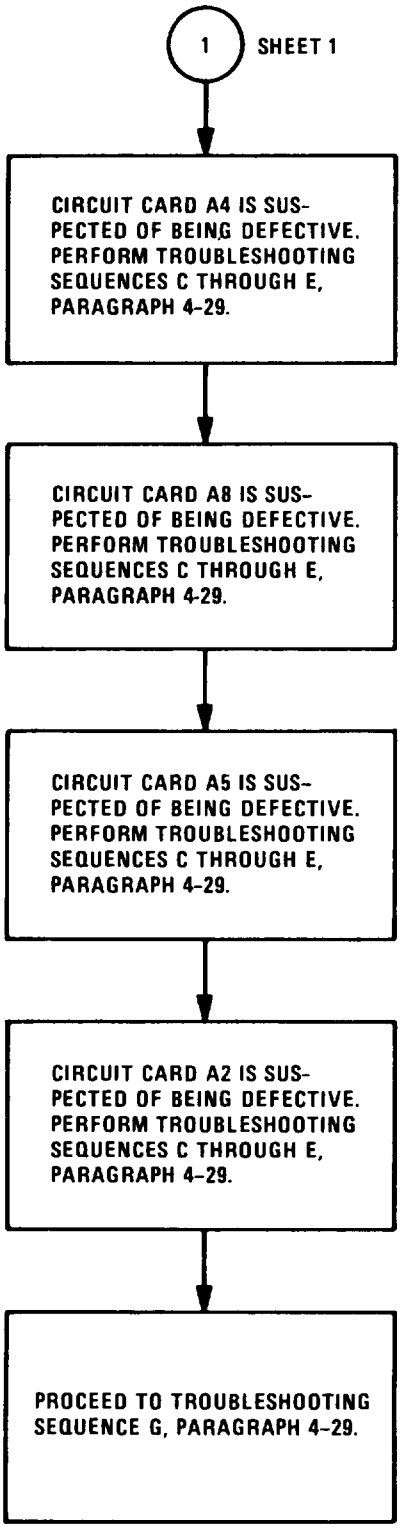
Troubleshooting Flow Chart - Entry Point AC



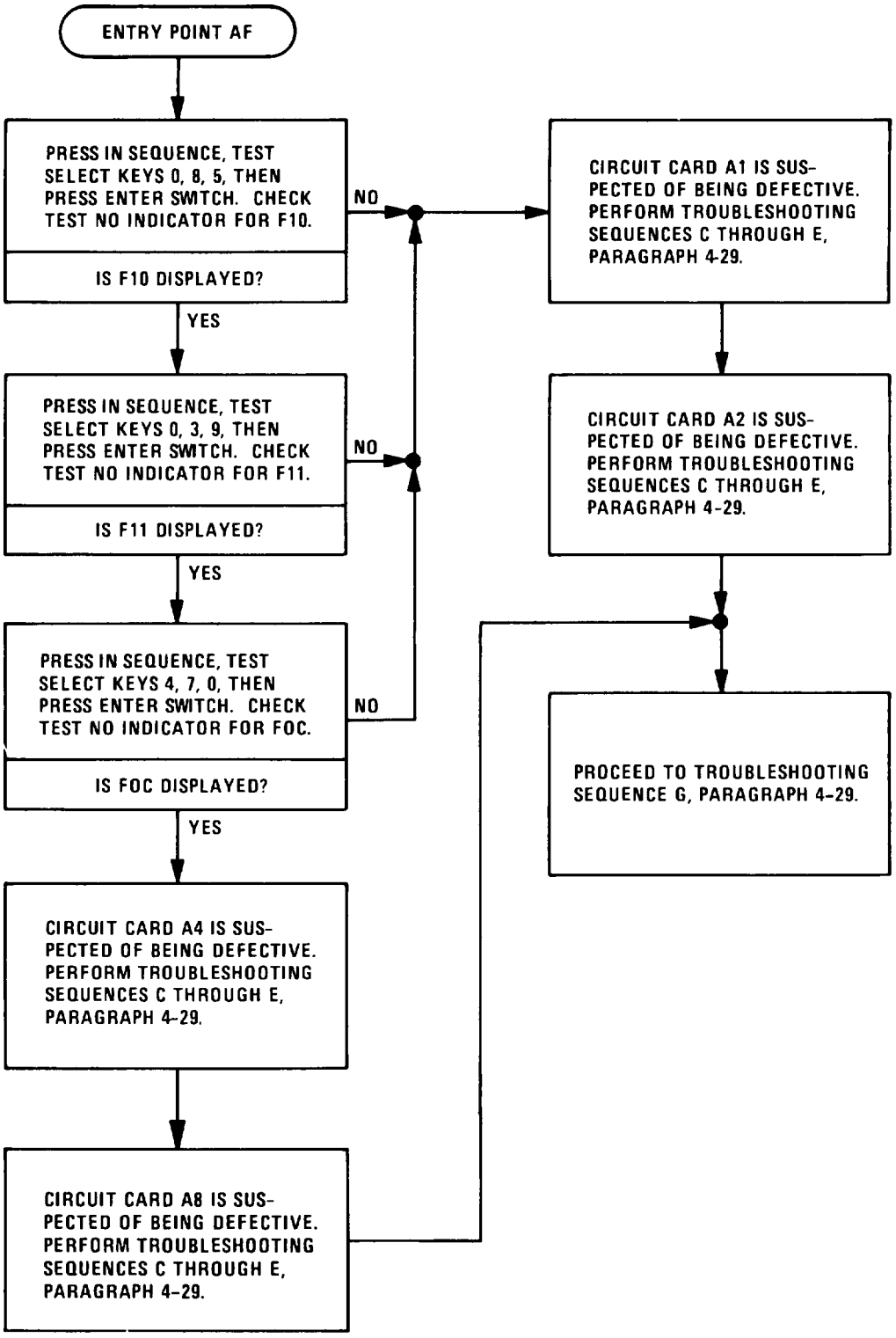
Troubleshooting Flow Chart - Entry Point AD



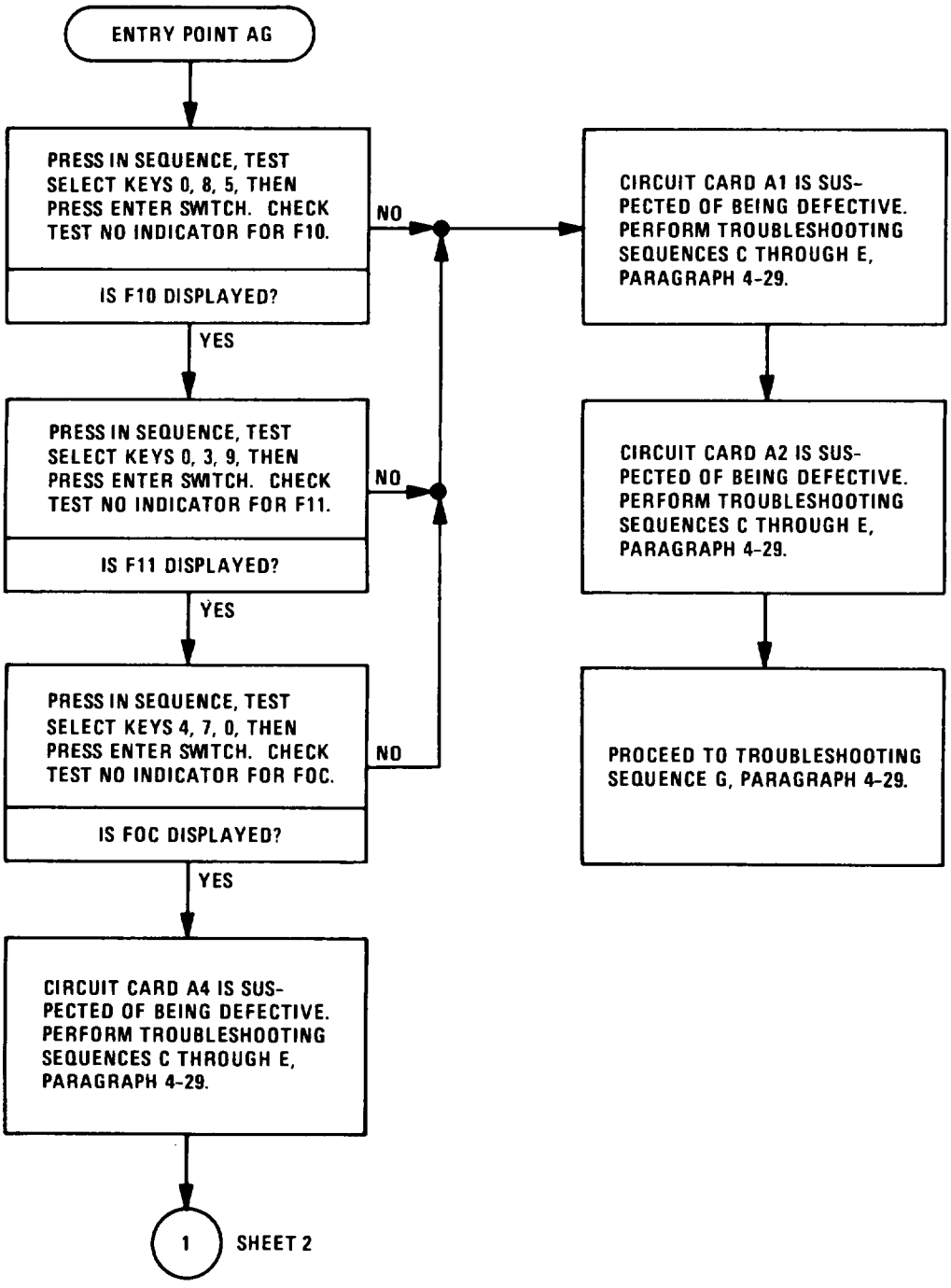
Troubleshooting Flow Chart - Entry Point AE (Sheet 1 of 2)



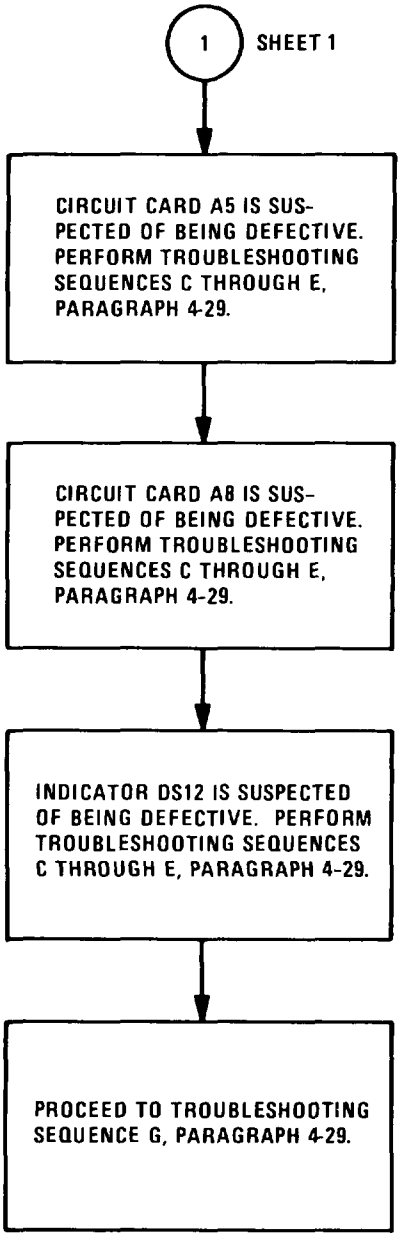
Troubleshooting Flow Chart - Entry Point AE (Sheet 2 of 2)



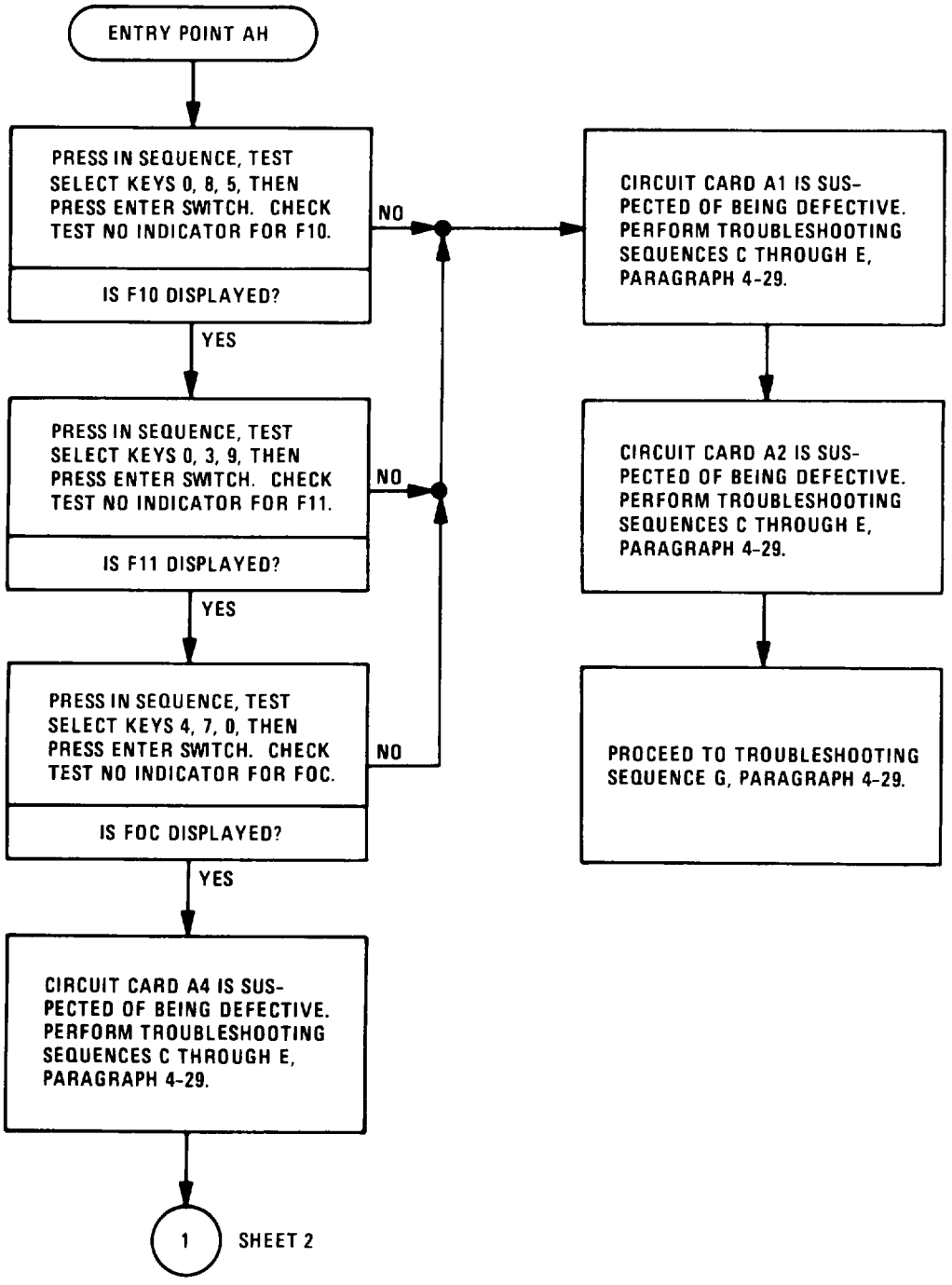
Troubleshooting Flow Chart - Entry Point AF



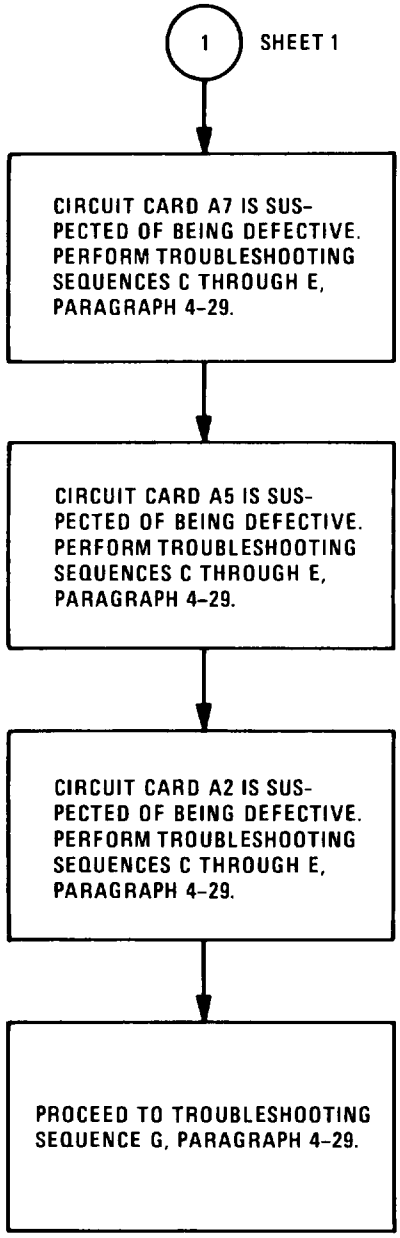
Troubleshooting Flow Chart - Entry Point AG (Sheet 1 of 2)



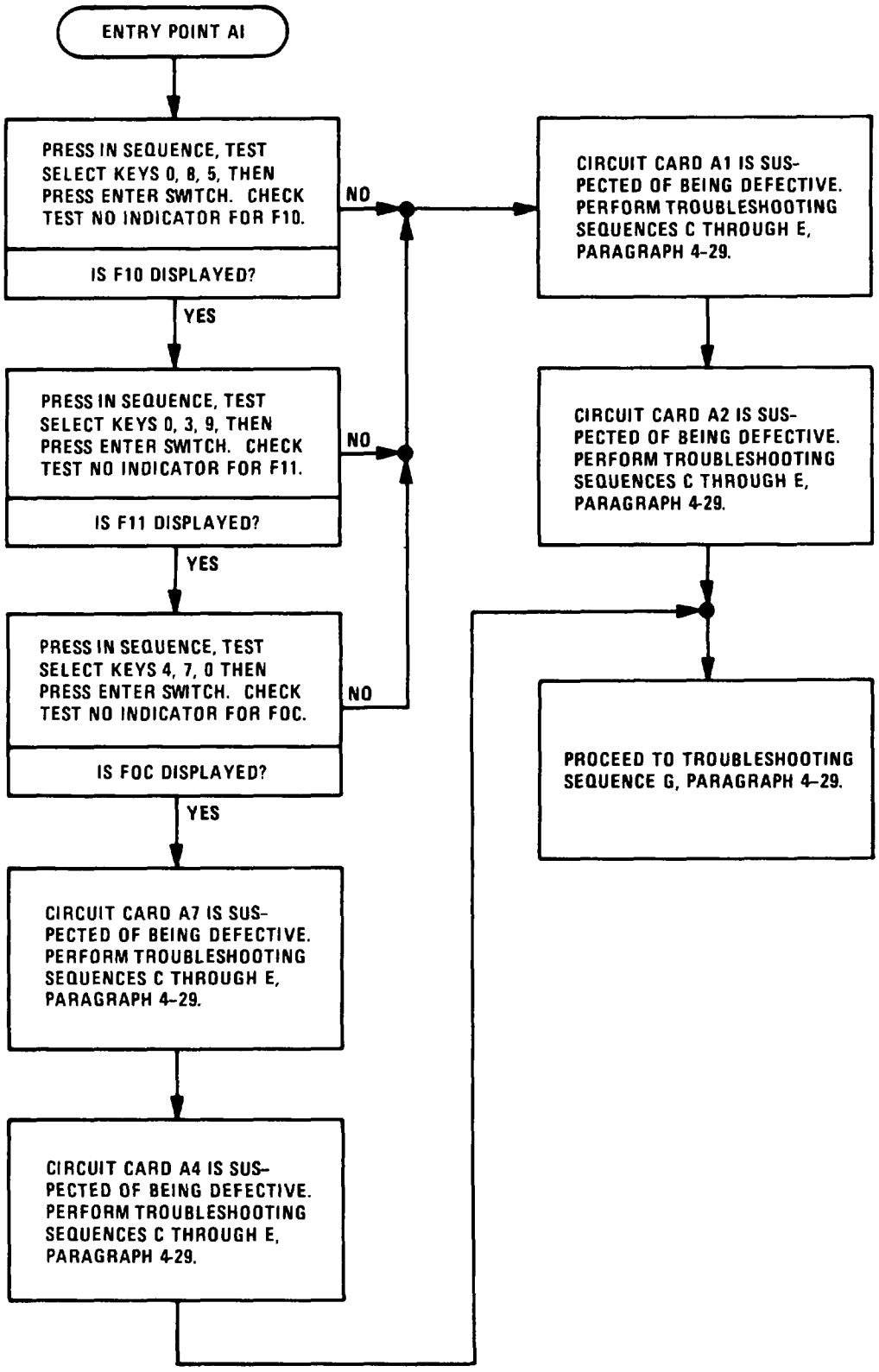
Troubleshooting Flow Chart - Entry Point AG (Sheet 2 of 2)



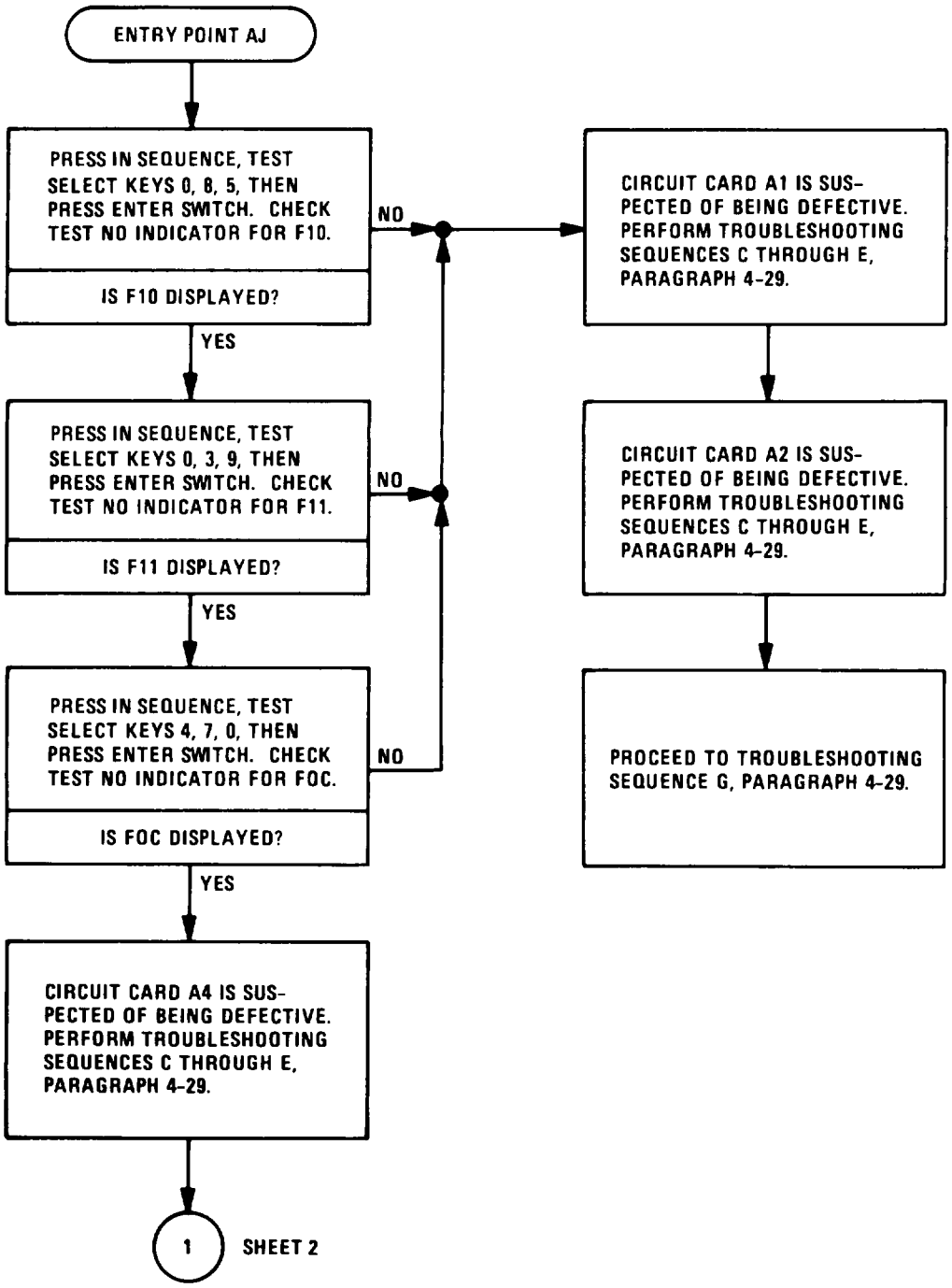
Troubleshooting Flow Chart - Entry Point AH (Sheet 1 of 2)



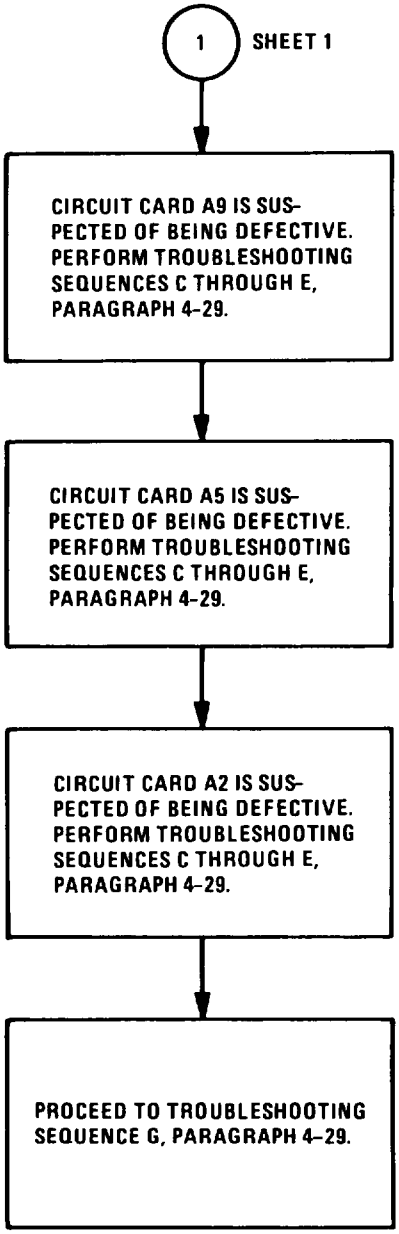
Troubleshooting Flow Chart - Entry Point AH (Sheet 2 of 2)



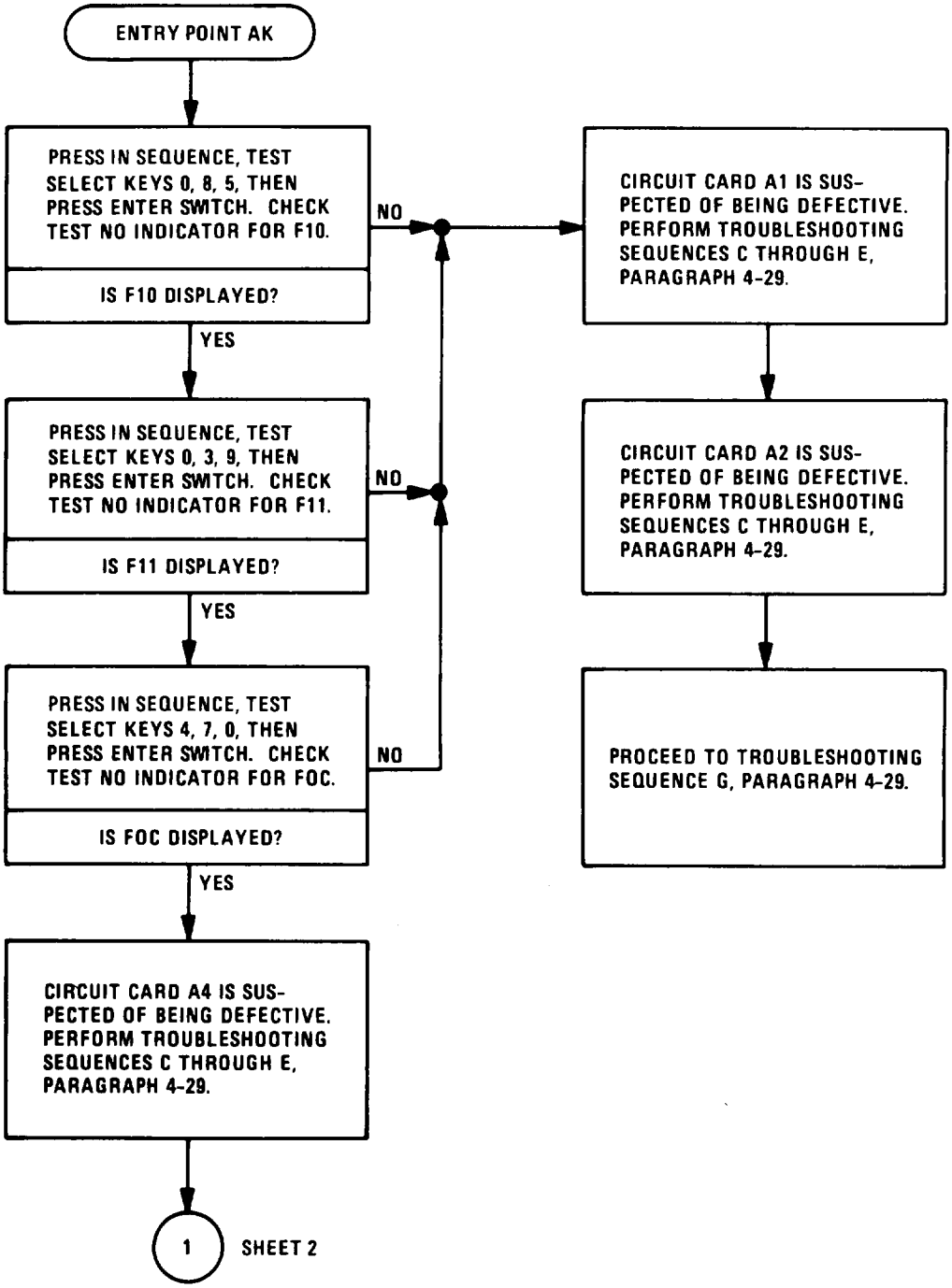
Troubleshooting Flow Chart - Entry Point AI



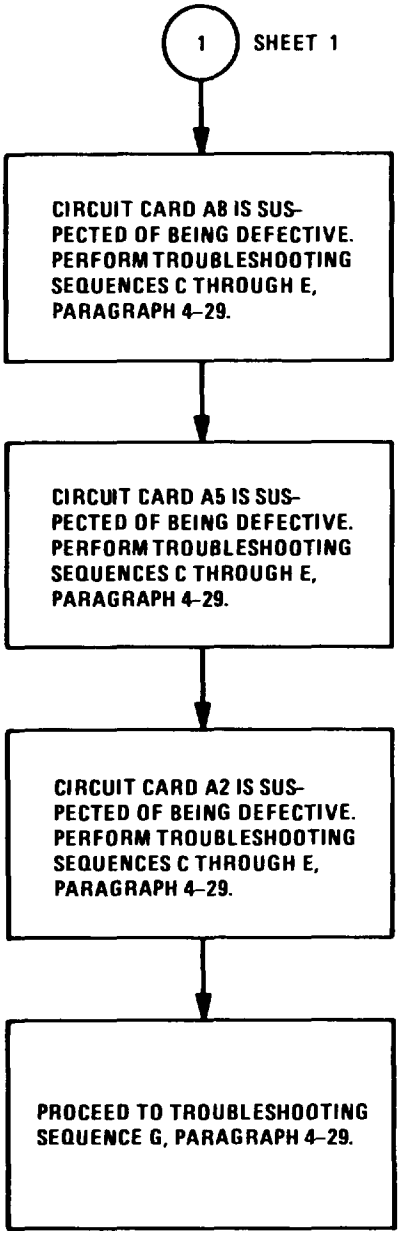
Troubleshooting Flow Chart - Entry Point AJ (Sheet 1 of 2)



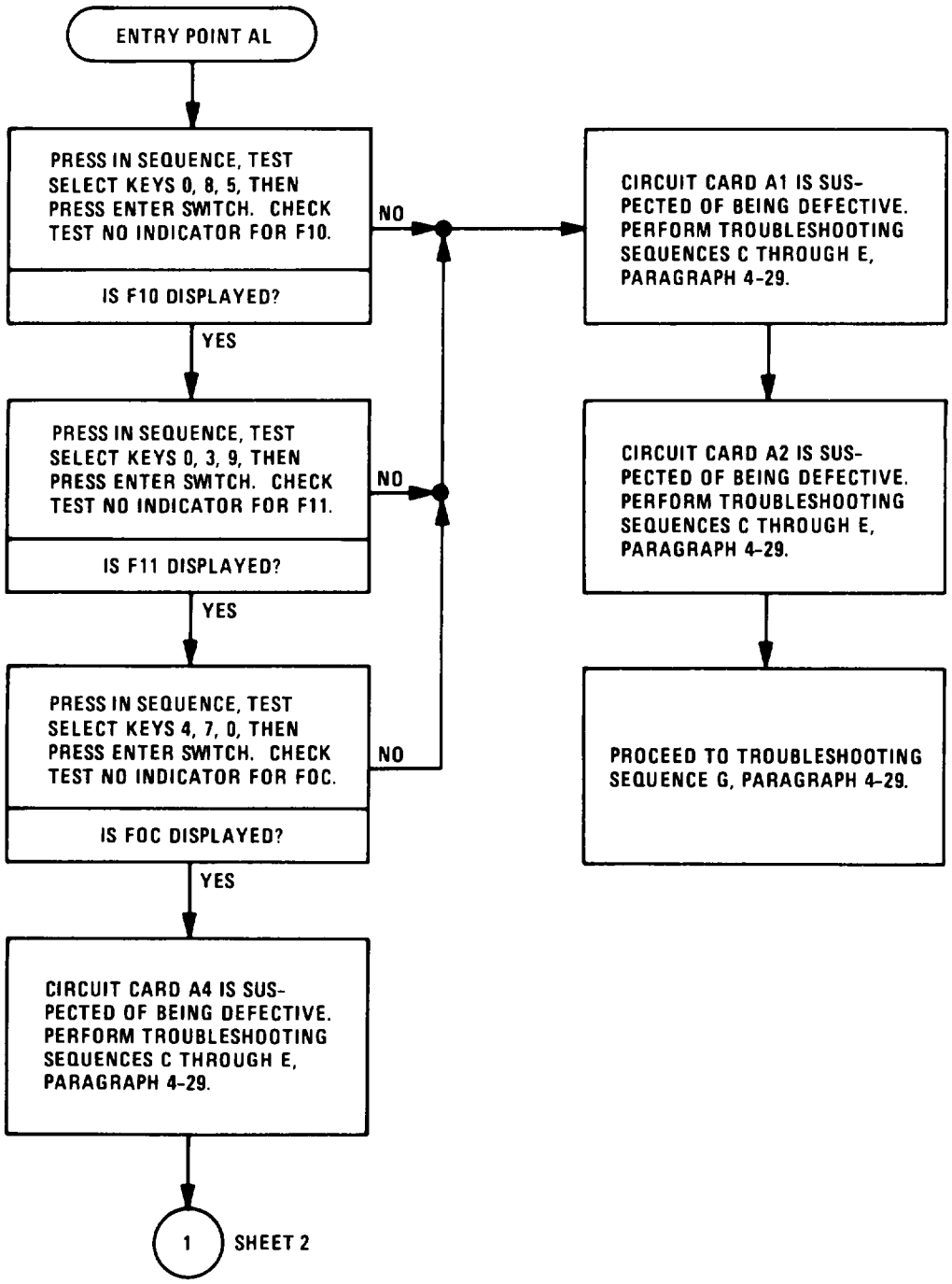
Troubleshooting Flow Chart - Entry Point AJ (Sheet 2 of 2)



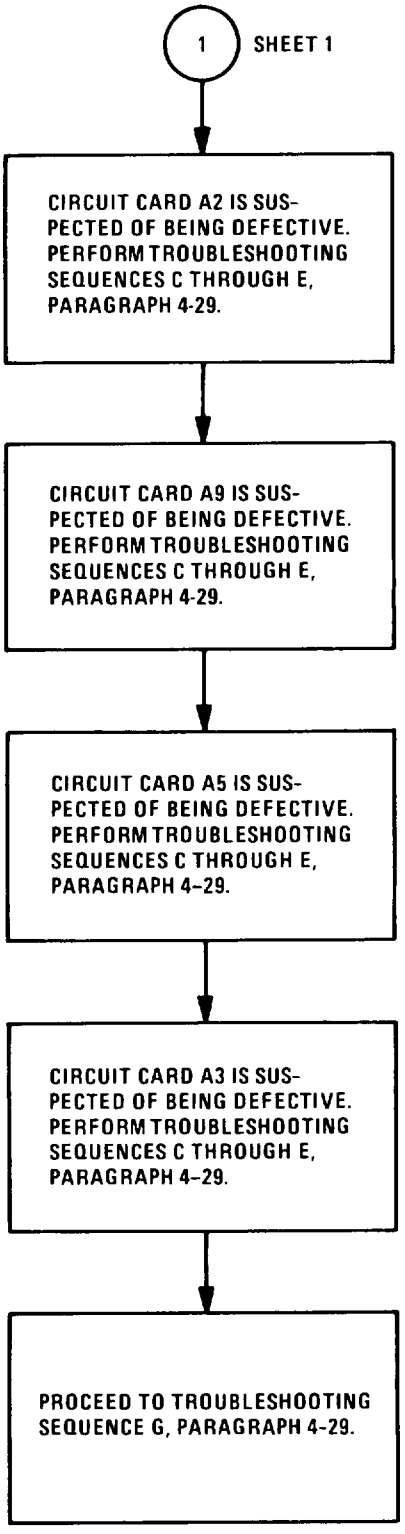
Troubleshooting Flow Chart - Entry Point AK (Sheet 1 of 2)



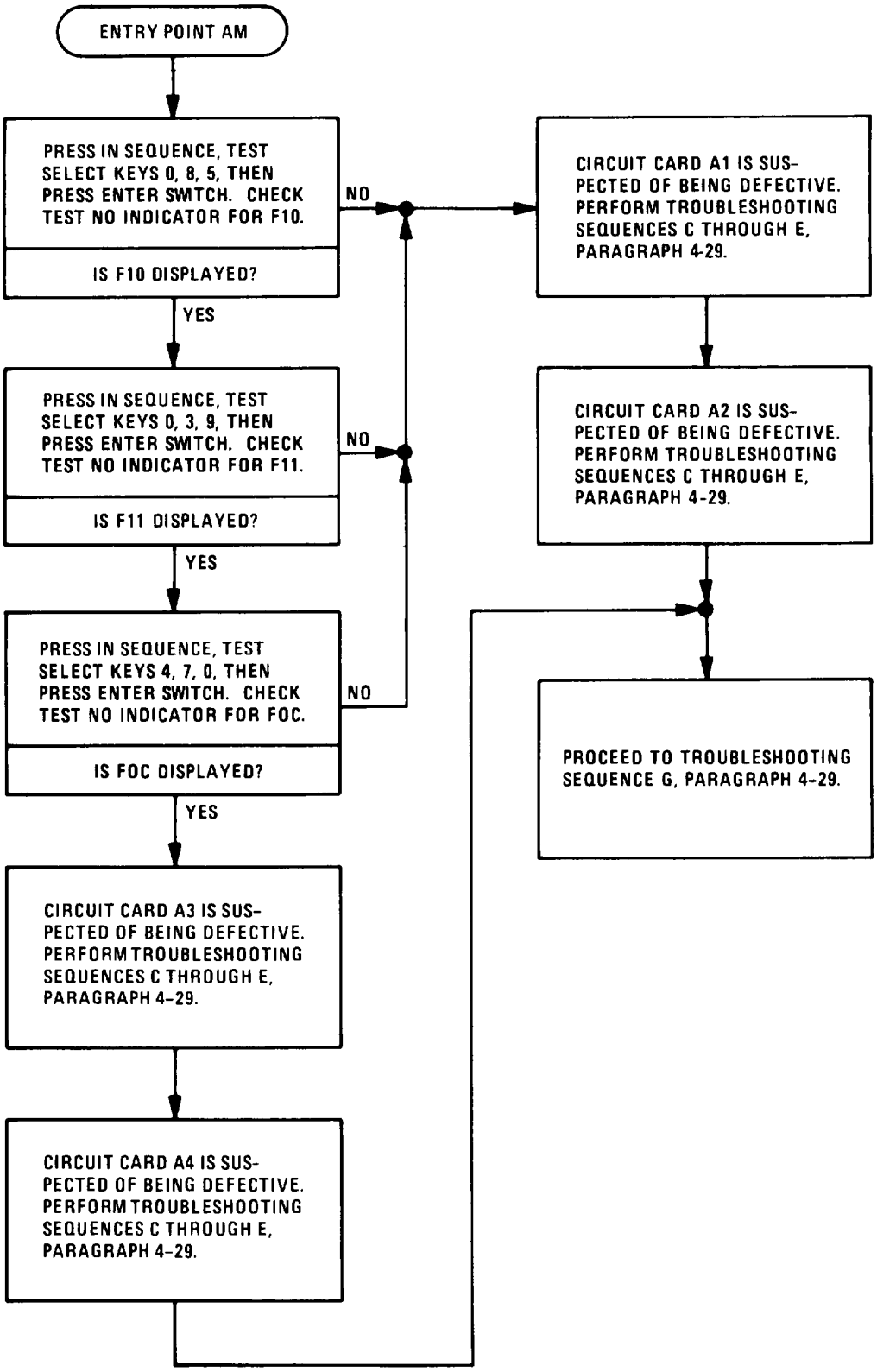
Troubleshooting Flow Chart - Entry Point AK (Sheet 2 of 2)



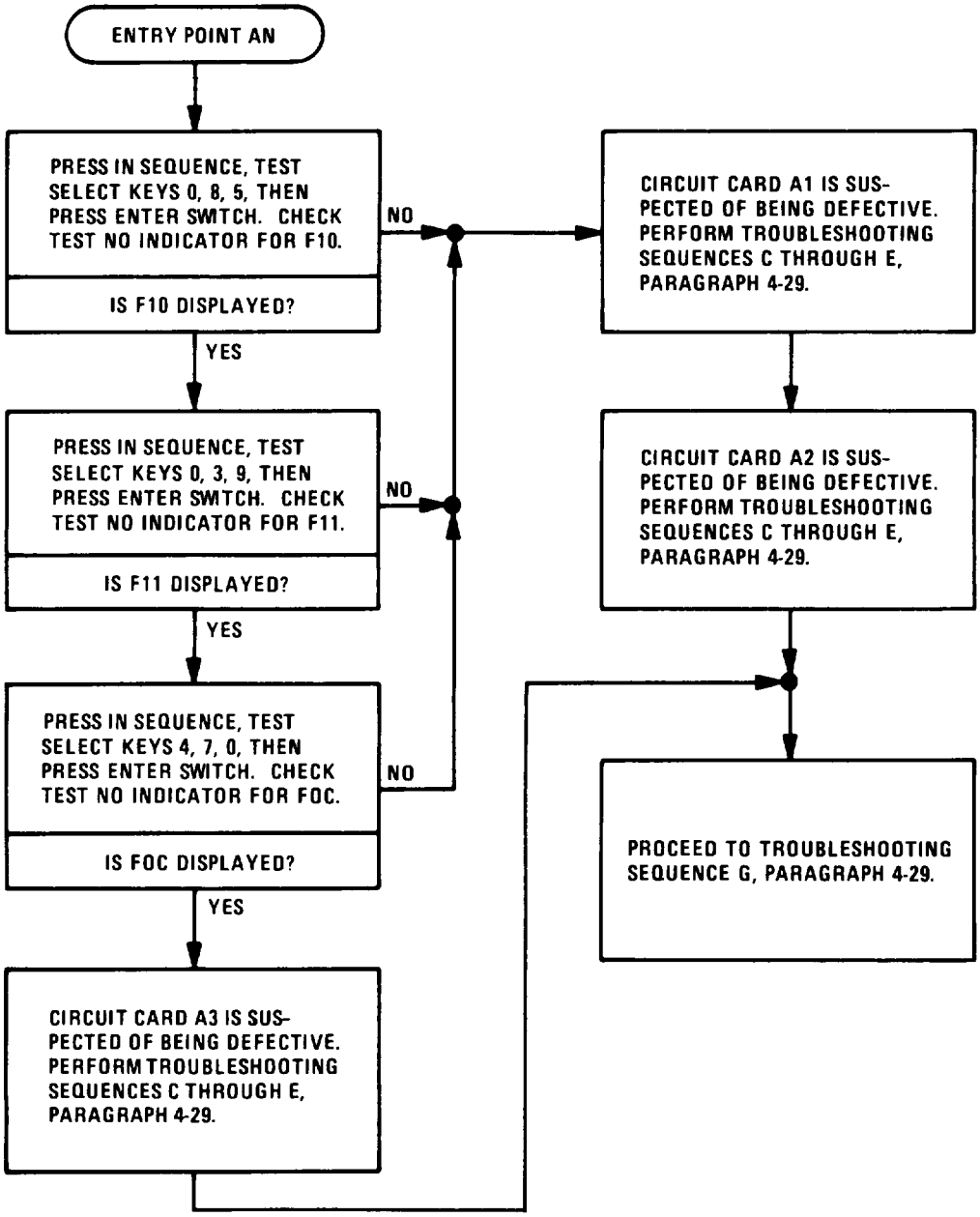
Troubleshooting Flow Chart - Entry Point AL (Sheet 1 of 2)



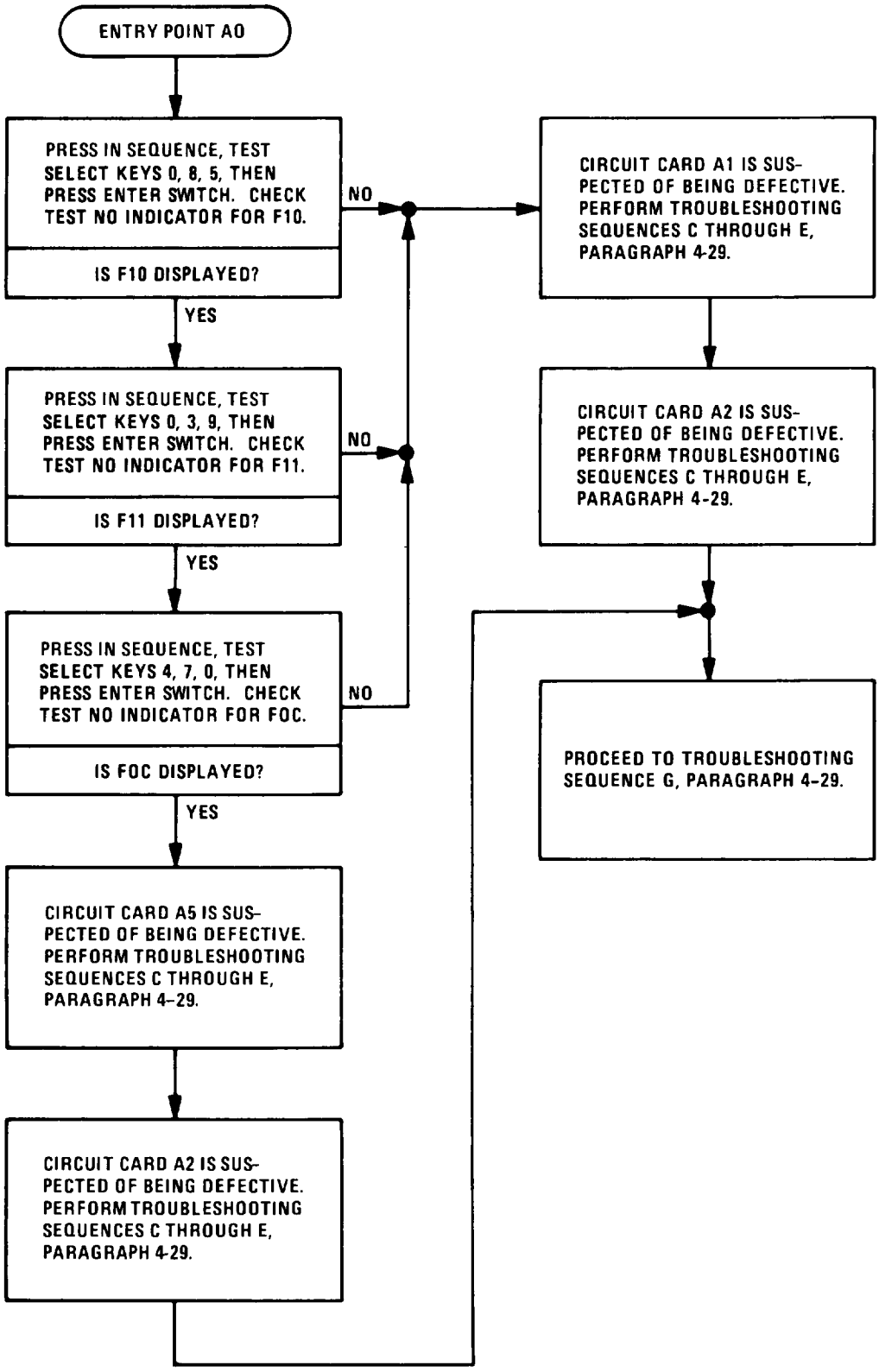
Troubleshooting Flow Chart - Entry Point AL (Sheet 2 of 2)



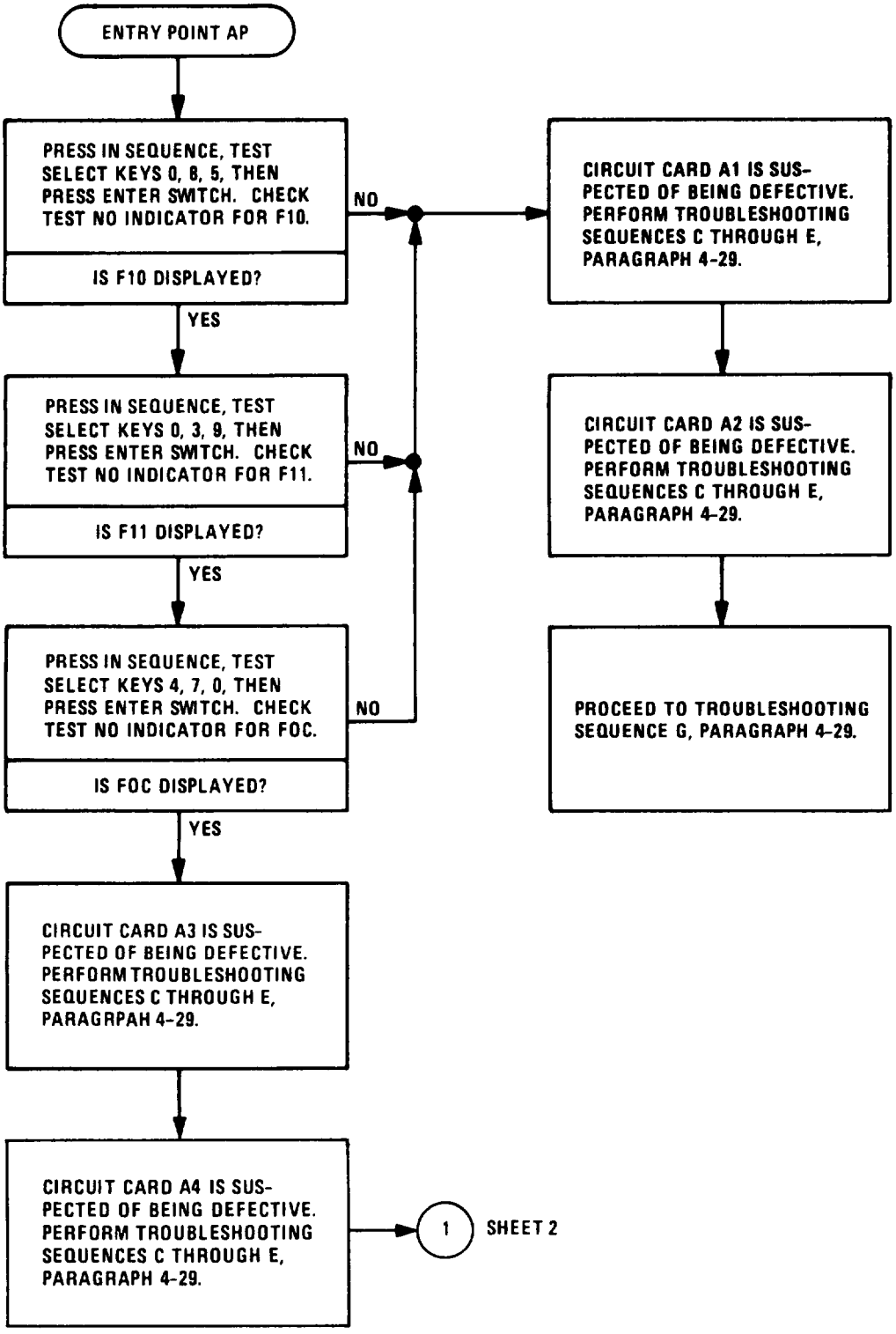
Troubleshooting Flow Chart - Entry Point AM



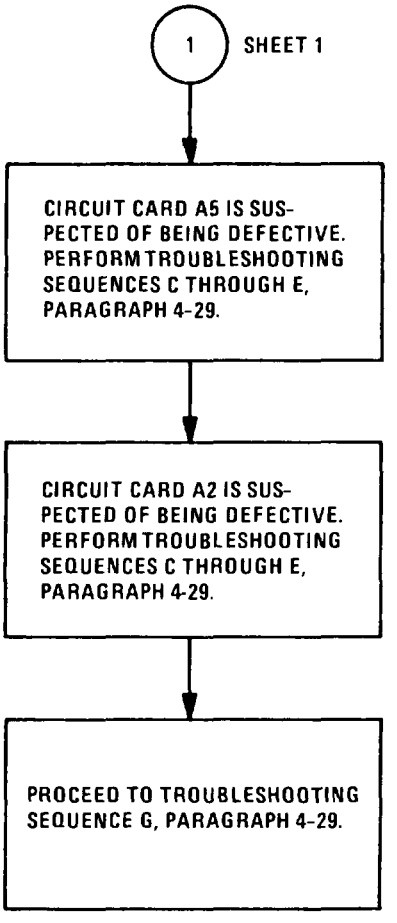
Troubleshooting Flow Chart - Entry Point AN



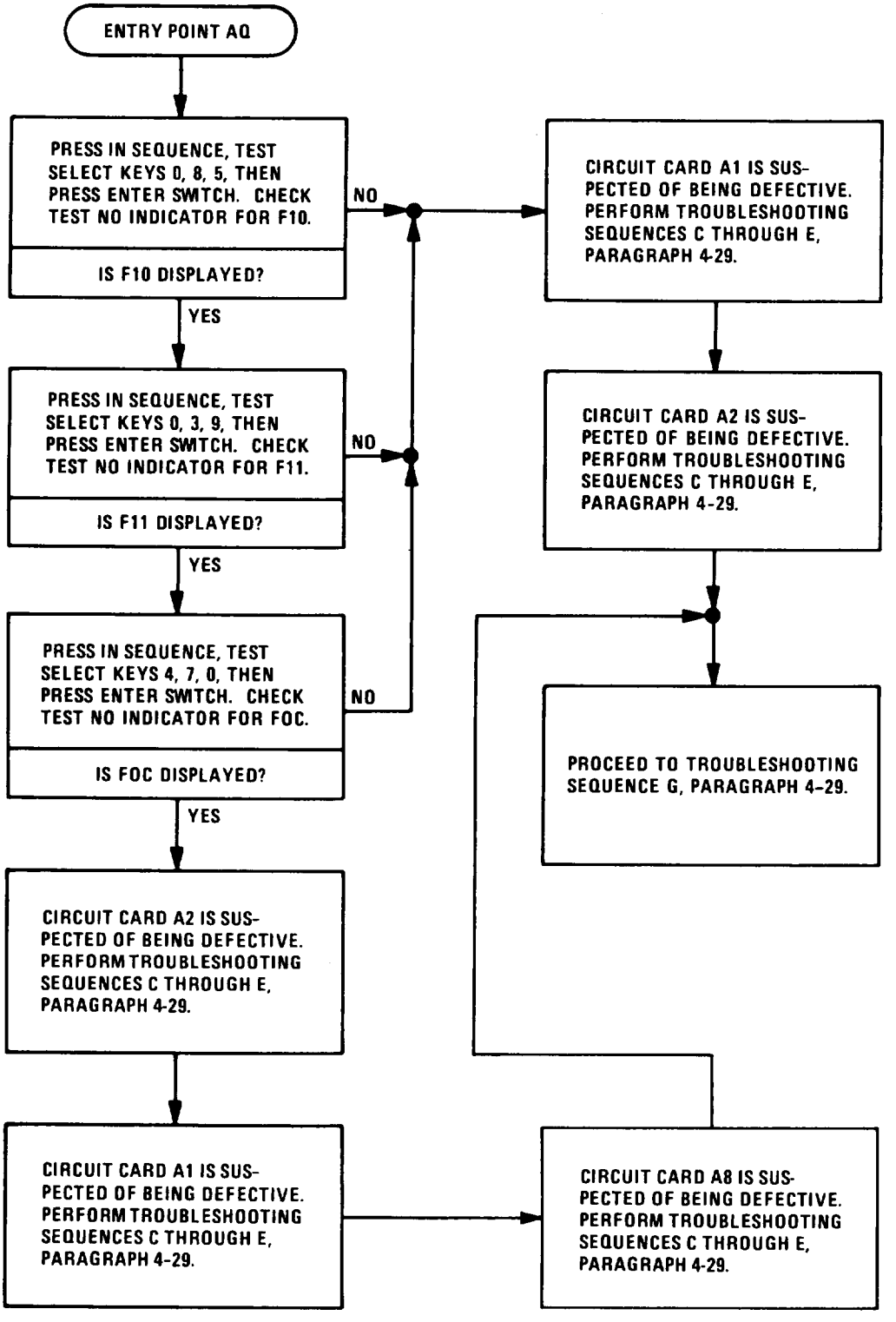
Troubleshooting Flow Chart - Entry Point AO



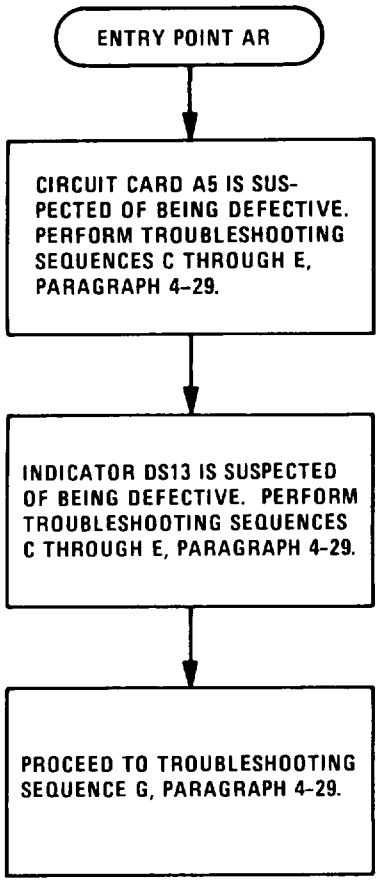
Troubleshooting Flow Chart - Entry Point AP (Sheet 1 of 2)



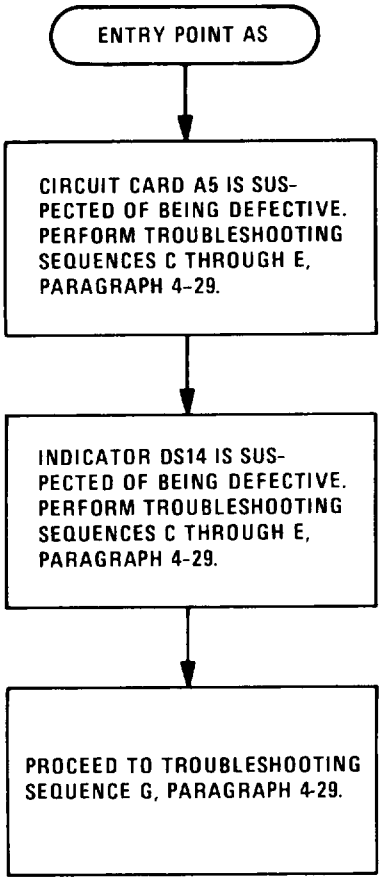
Troubleshooting Flow Chart - Entry Point AP (Sheet 2 of 2)



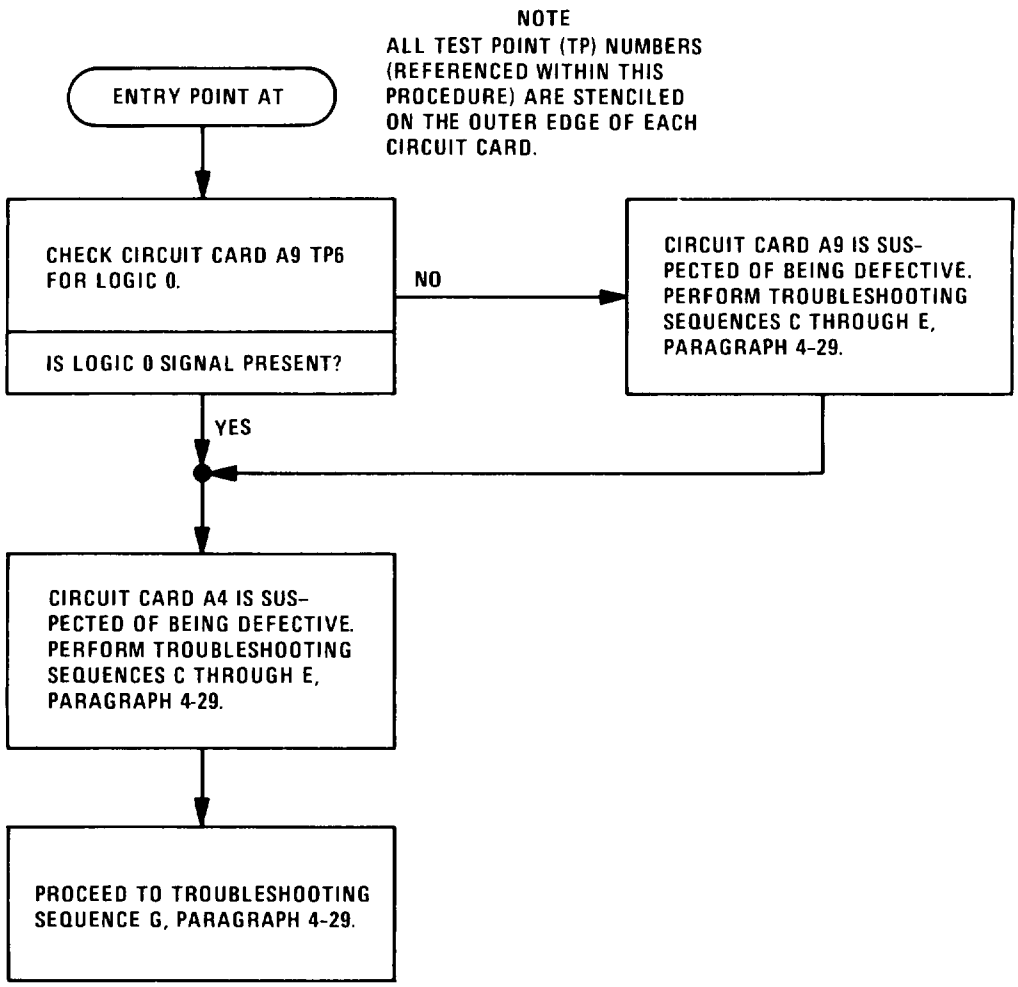
Troubleshooting Flow Chart - Entry Point AQ



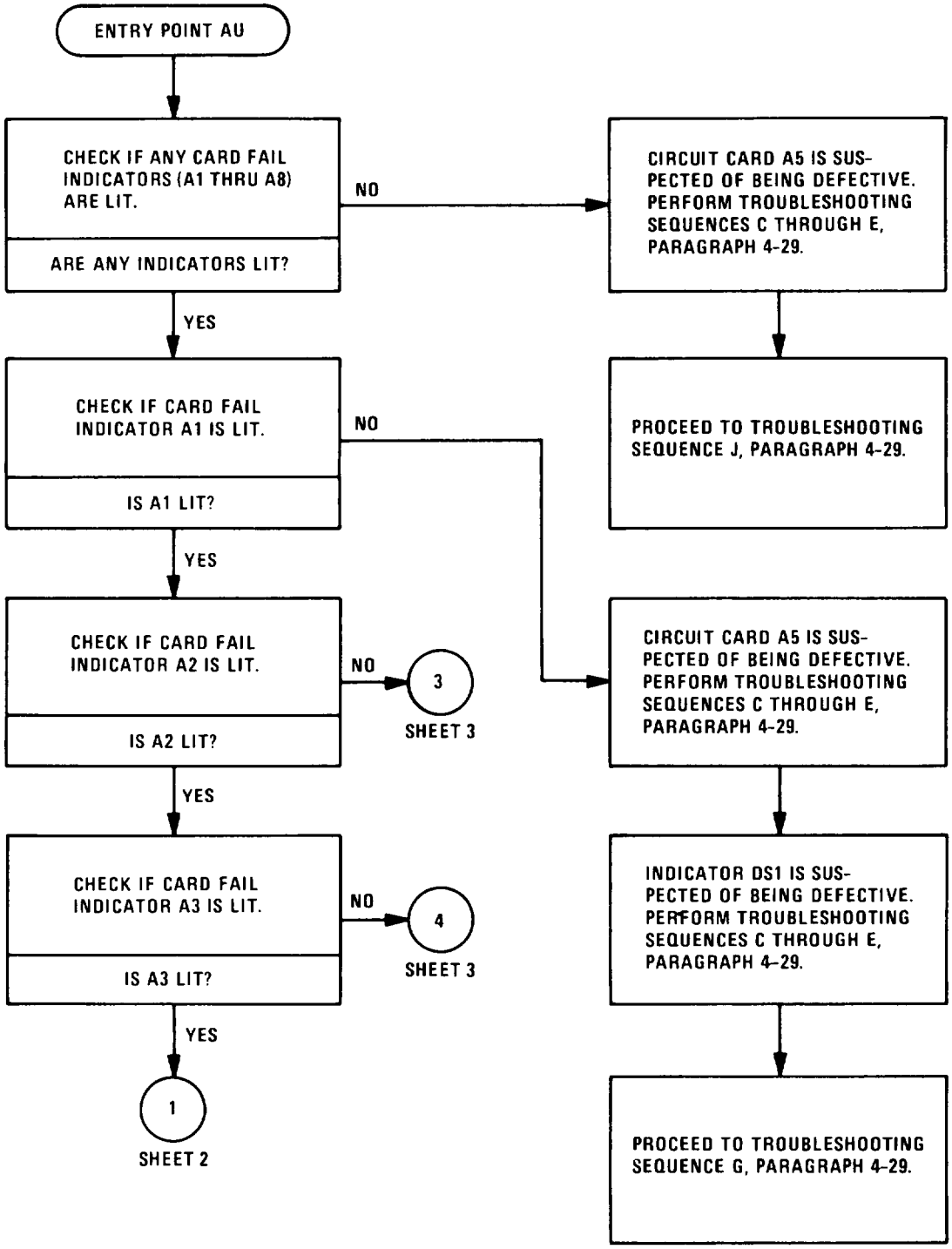
Troubleshooting Flow Chart - Entry Point AR



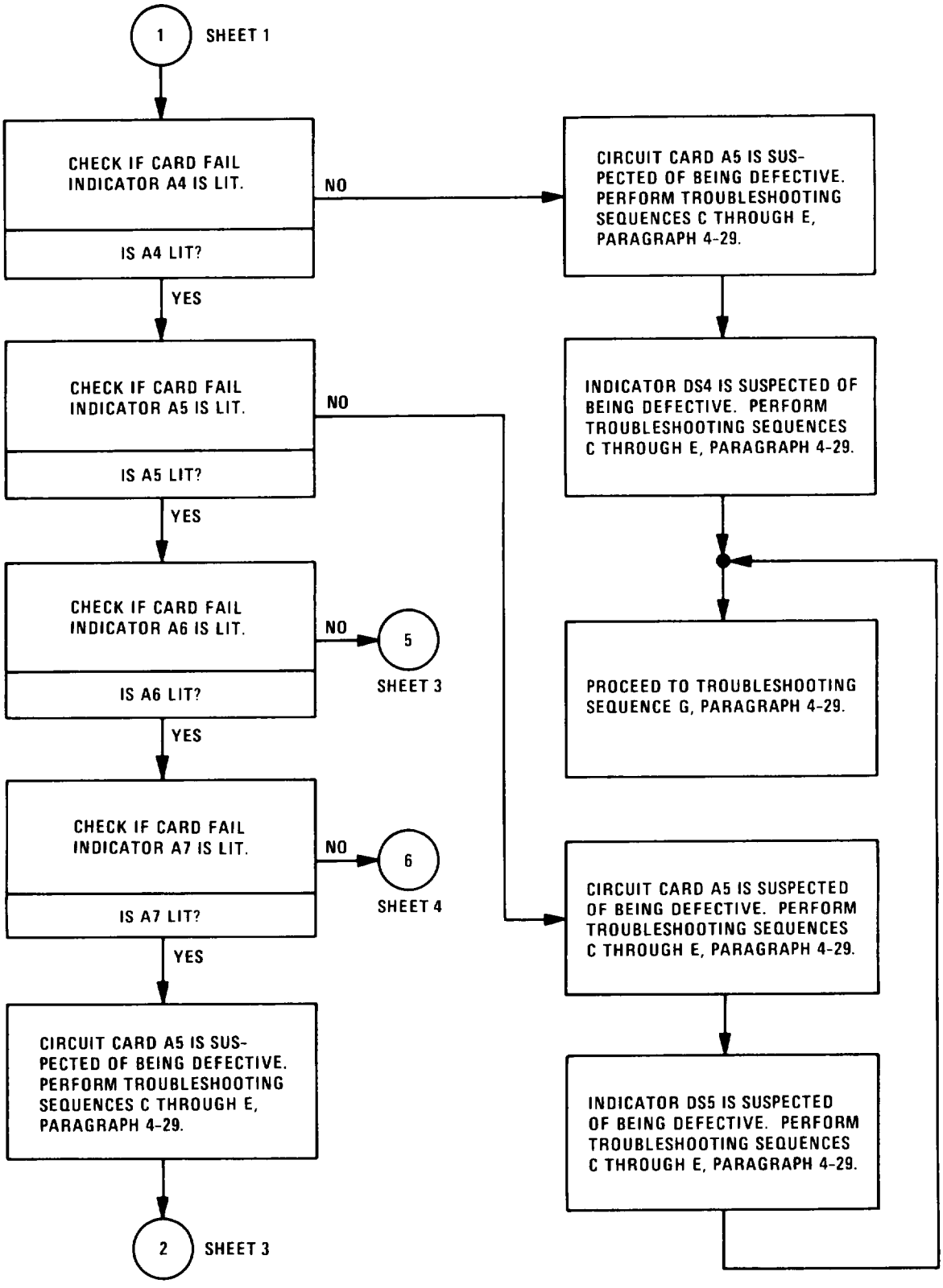
Troubleshooting Flow Chart - Entry Point AS



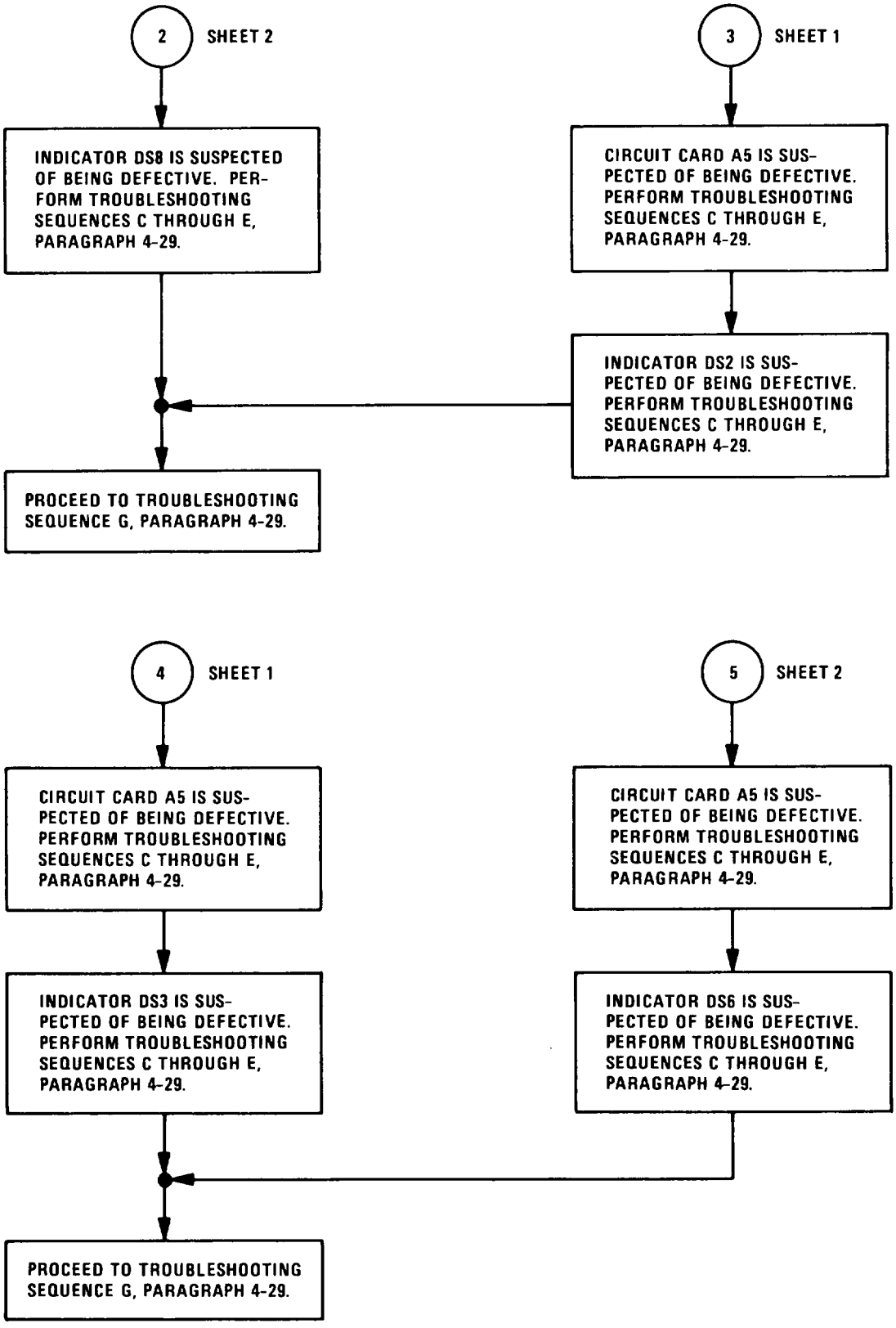
Troubleshooting Flow Chart - Entry Point AT



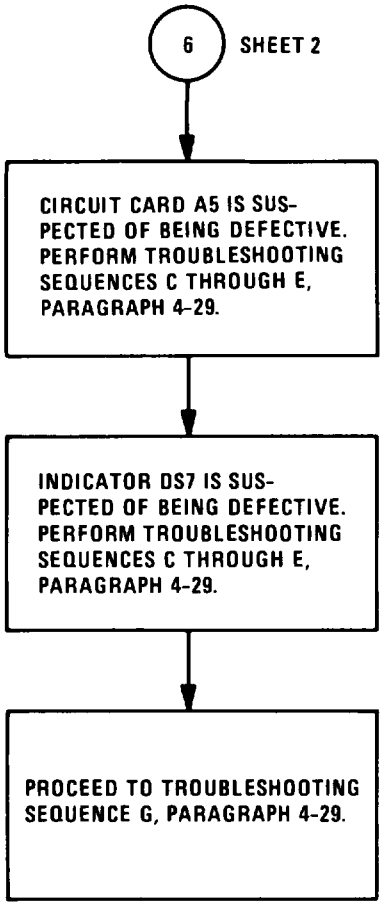
Troubleshooting Flow Chart - Entry Point AU (Sheet 1 of 4)



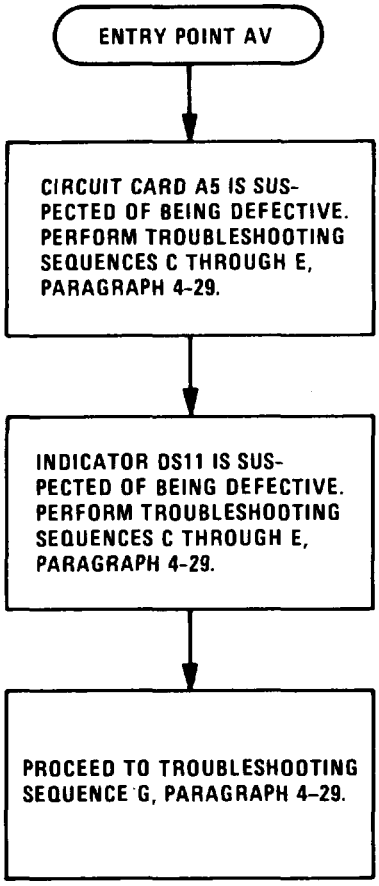
Troubleshooting Flow Chart - Entry Point AU (Sheet 2 of 4)



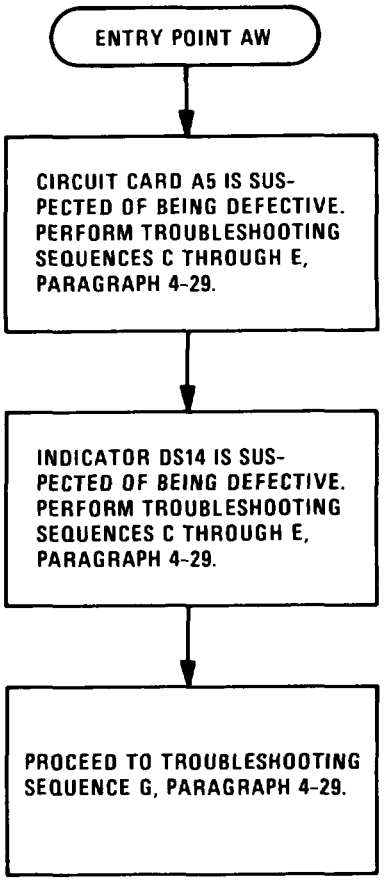
Troubleshooting Flow Chart - Entry Point AU (Sheet 3 of 4)



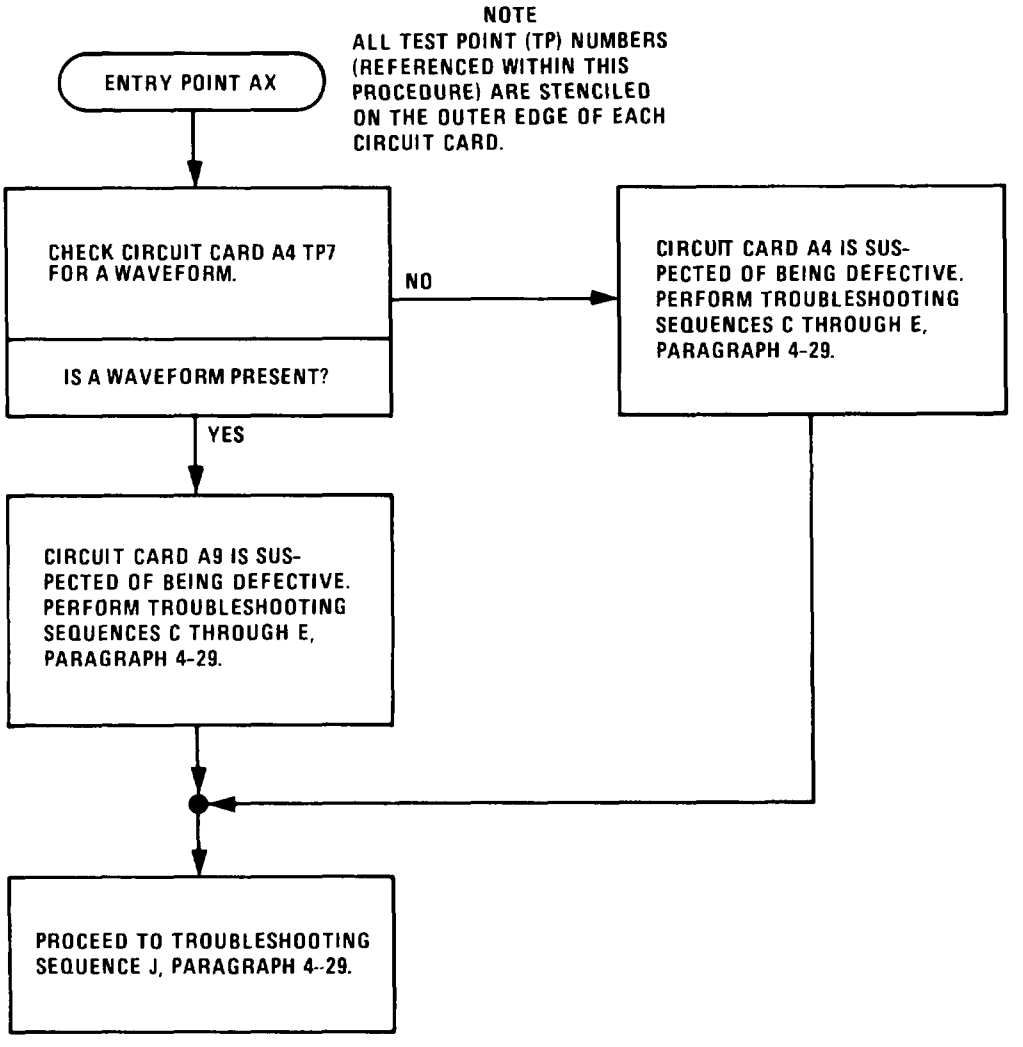
Troubleshooting Flow Chart - Entry Point AU (Sheet 4 of 4)



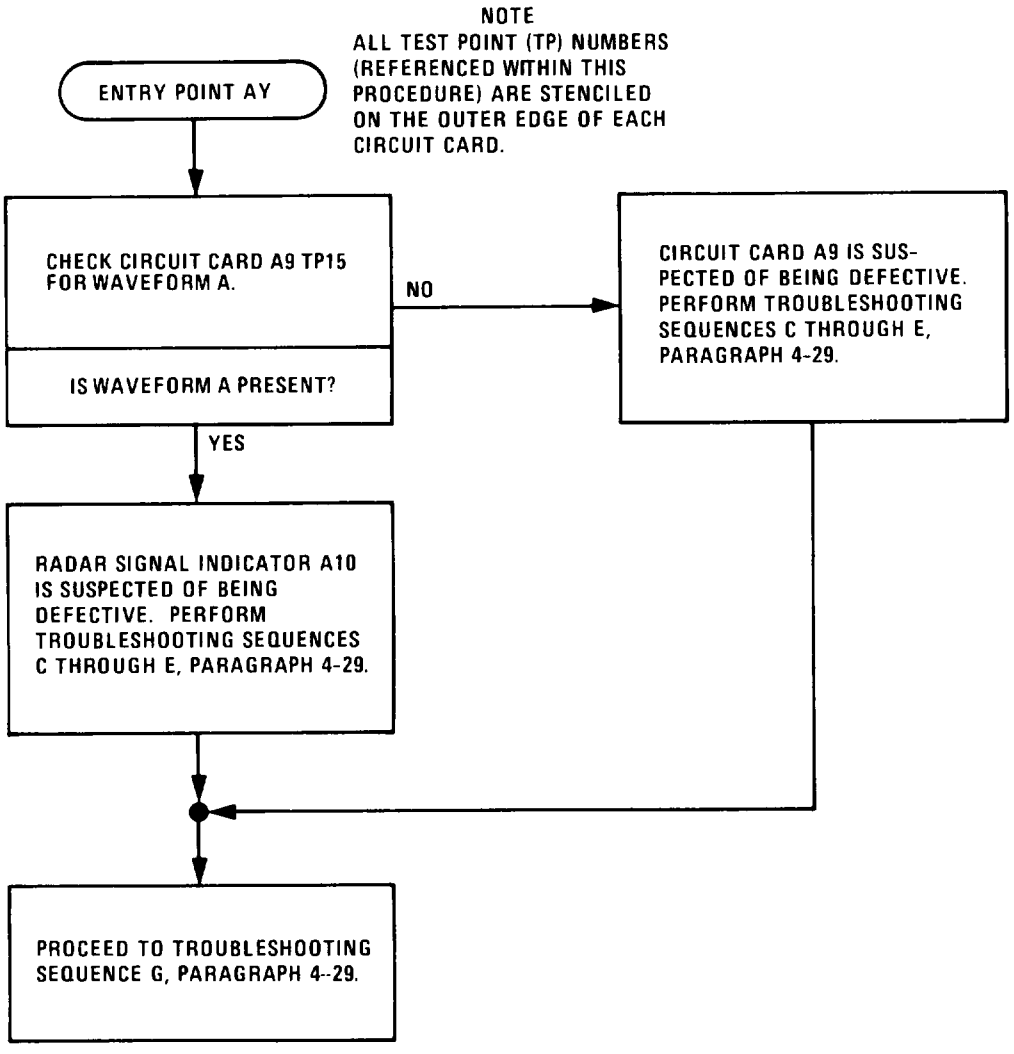
Troubleshooting Flow Chart - Entry Point AV



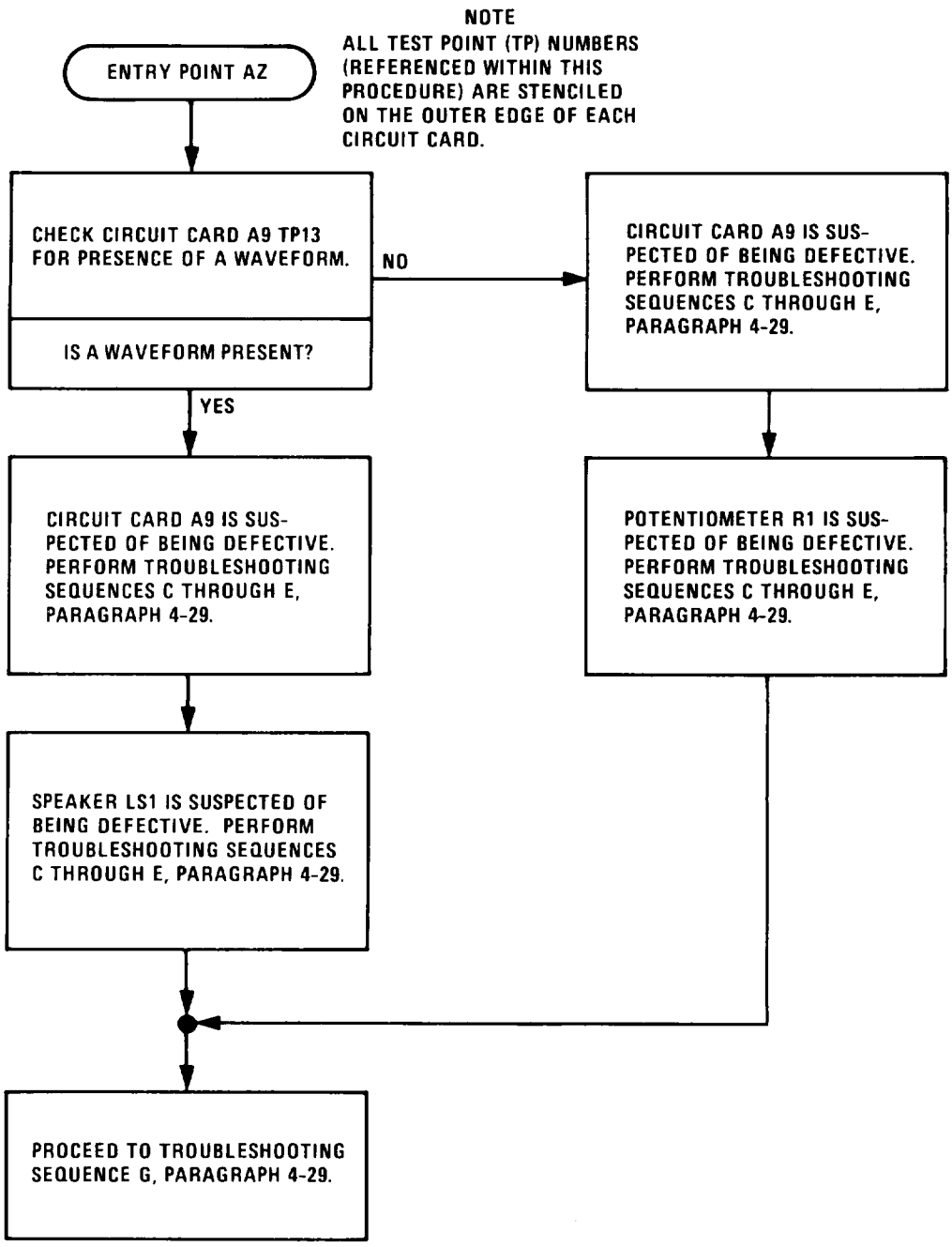
Troubleshooting Flow Chart - Entry Point AW



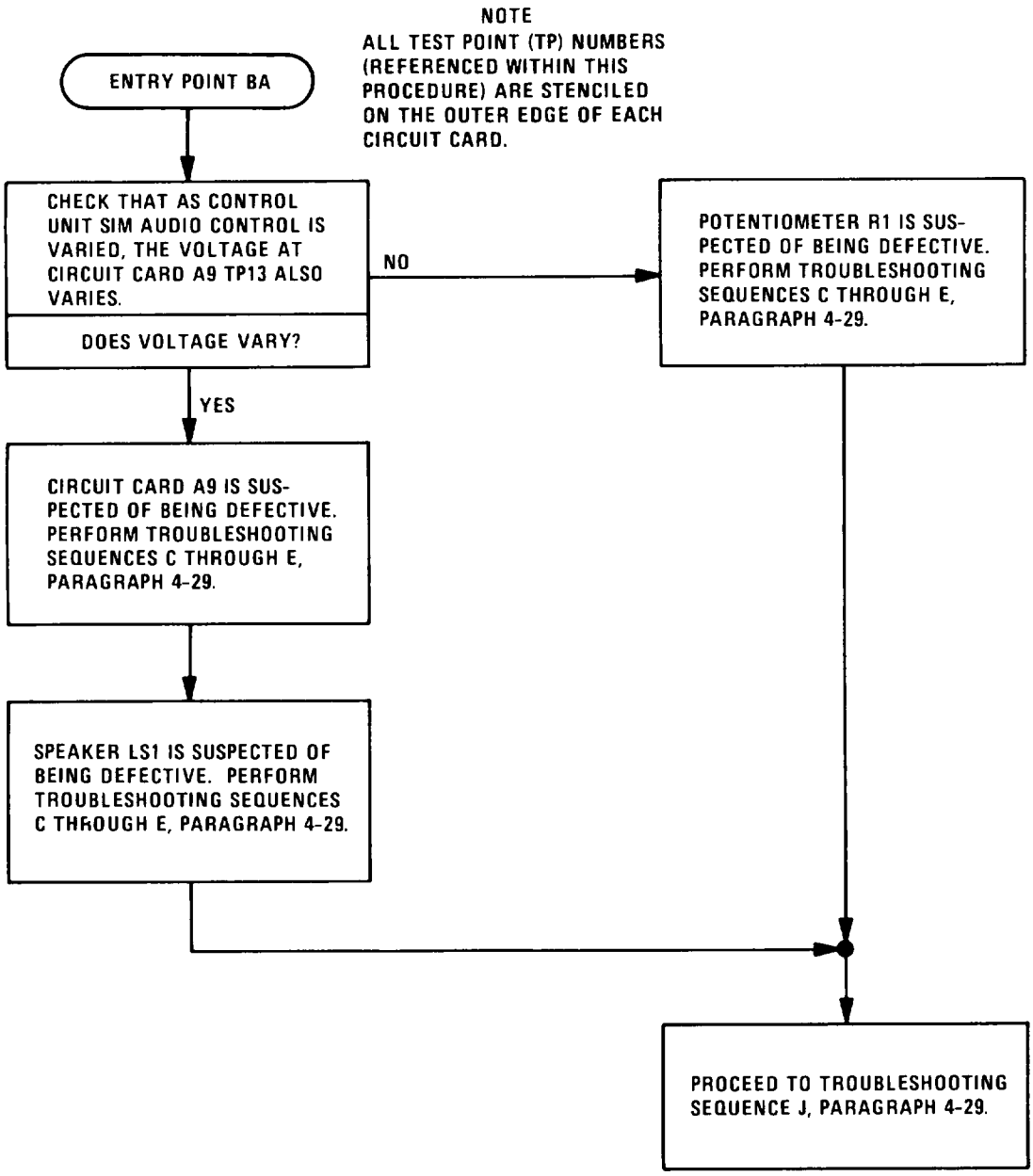
Troubleshooting Flow Chart - Entry Point AX



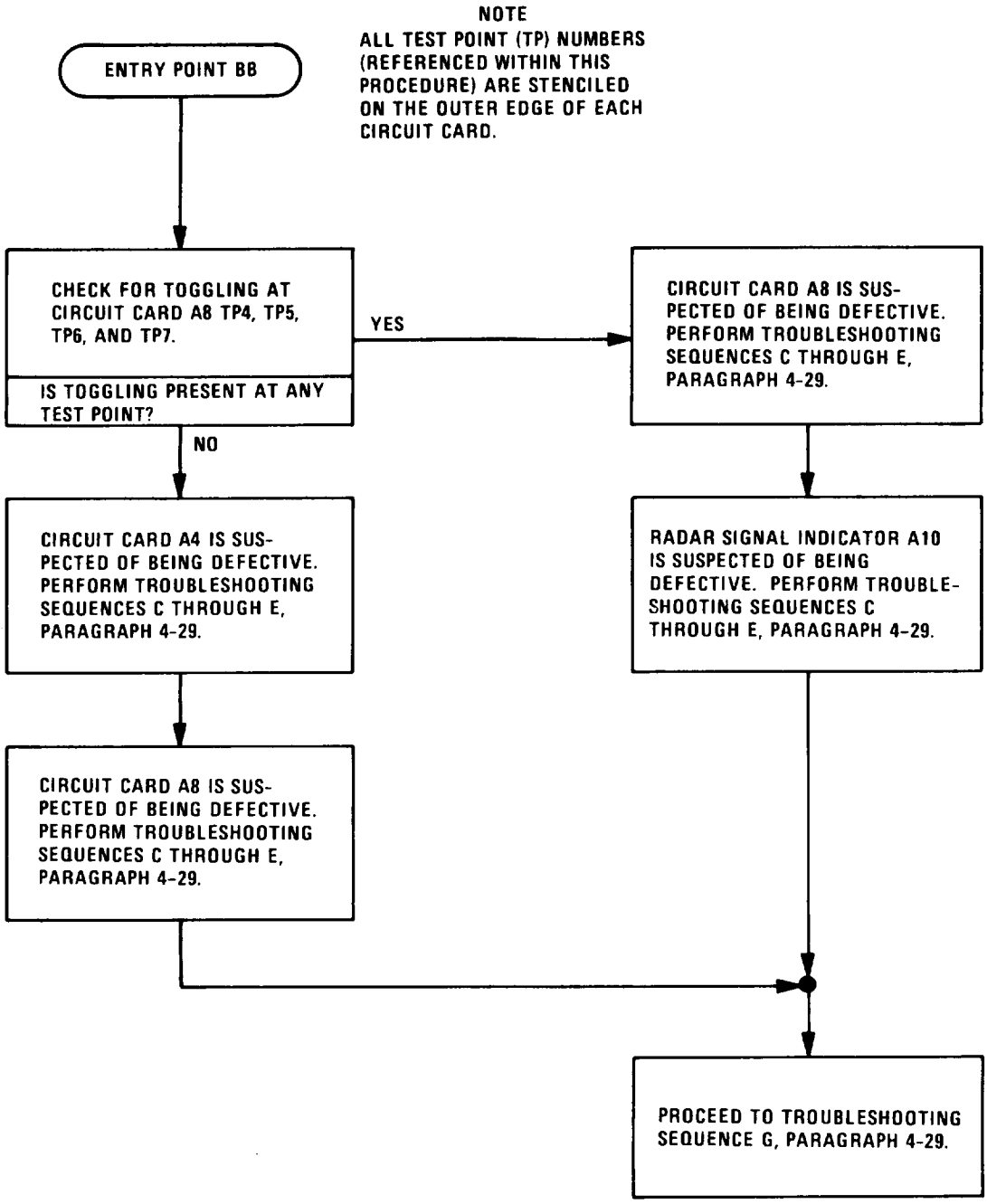
Troubleshooting Flow Chart - Entry Point AY



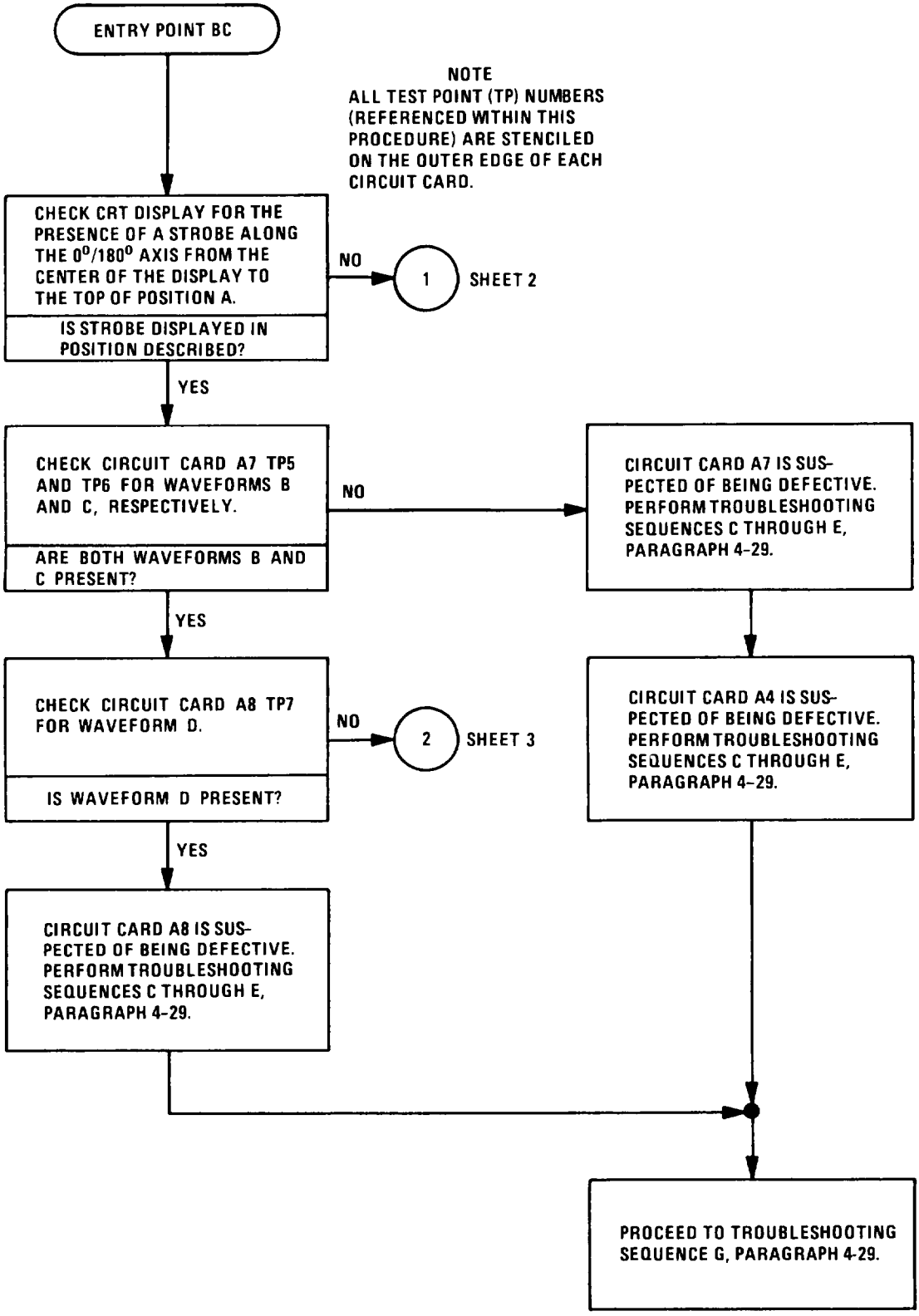
Troubleshooting Flow Chart - Entry Point AZ



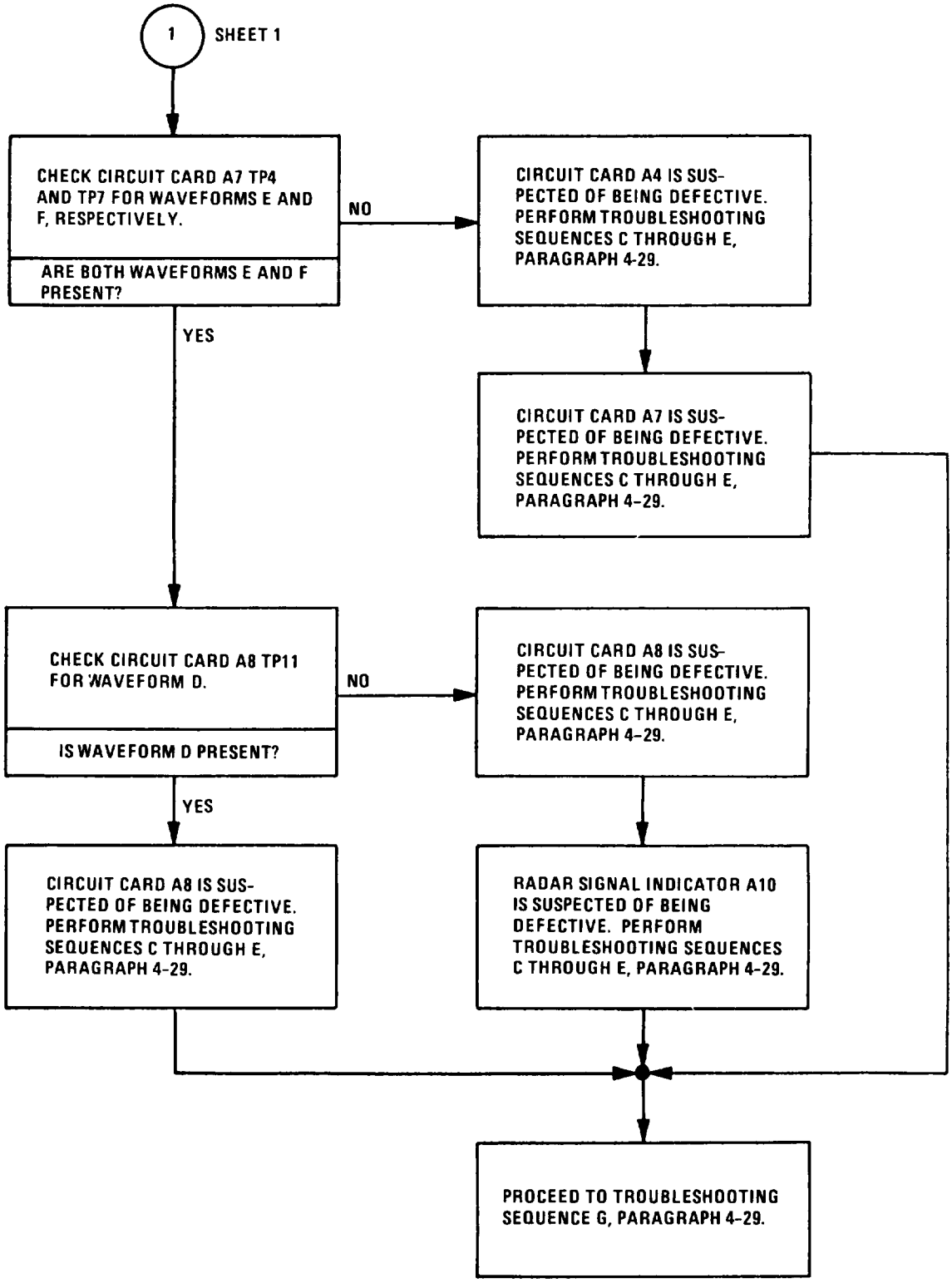
Troubleshooting Flow Chart - Entry Point BA



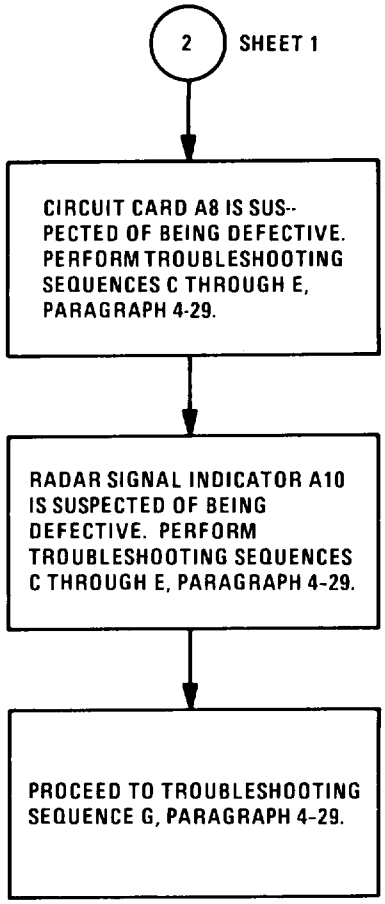
Troubleshooting Flow Chart - Entry Point BB



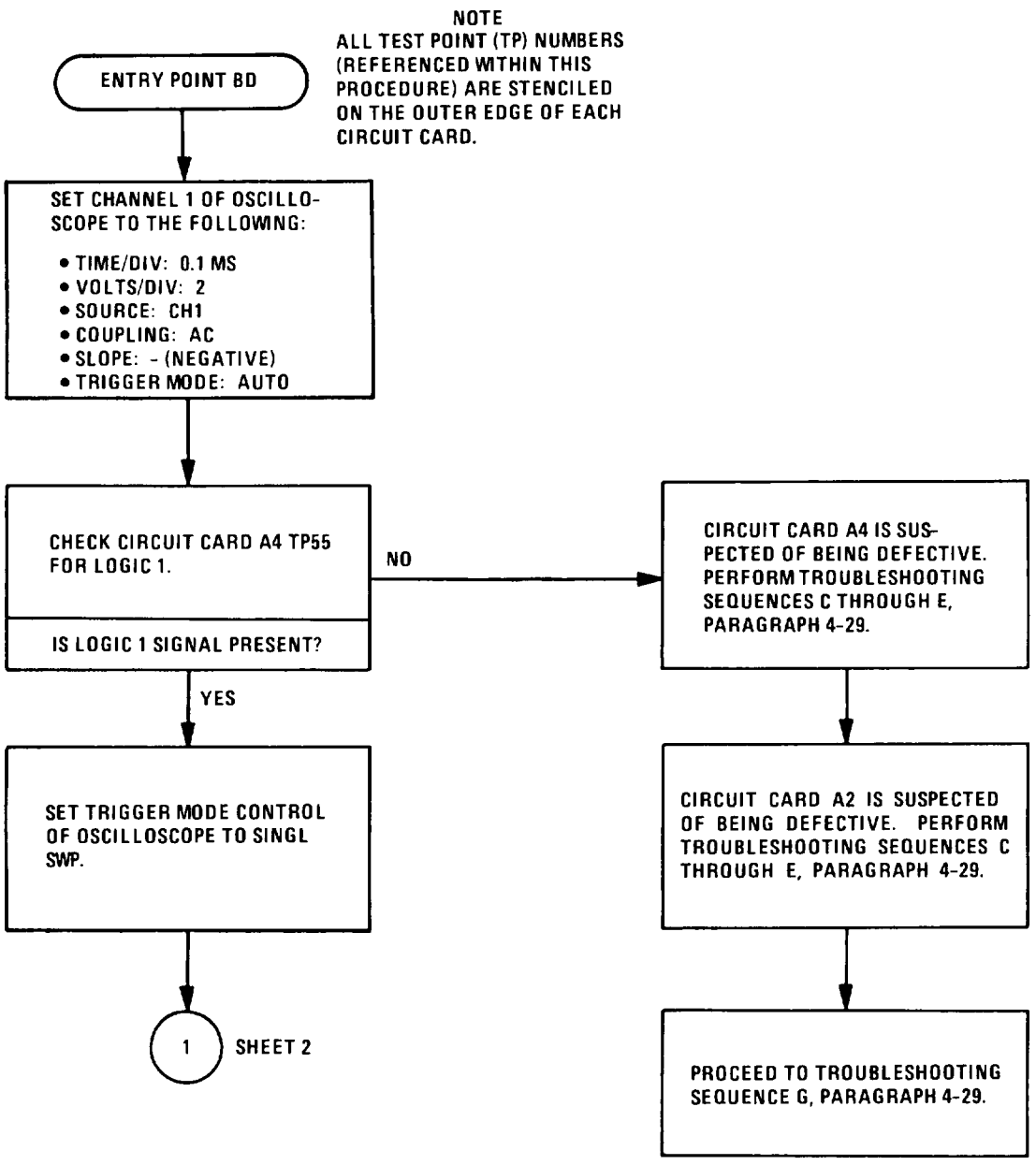
Troubleshooting Flow Chart - Entry Point BC (Sheet 1 of 3)



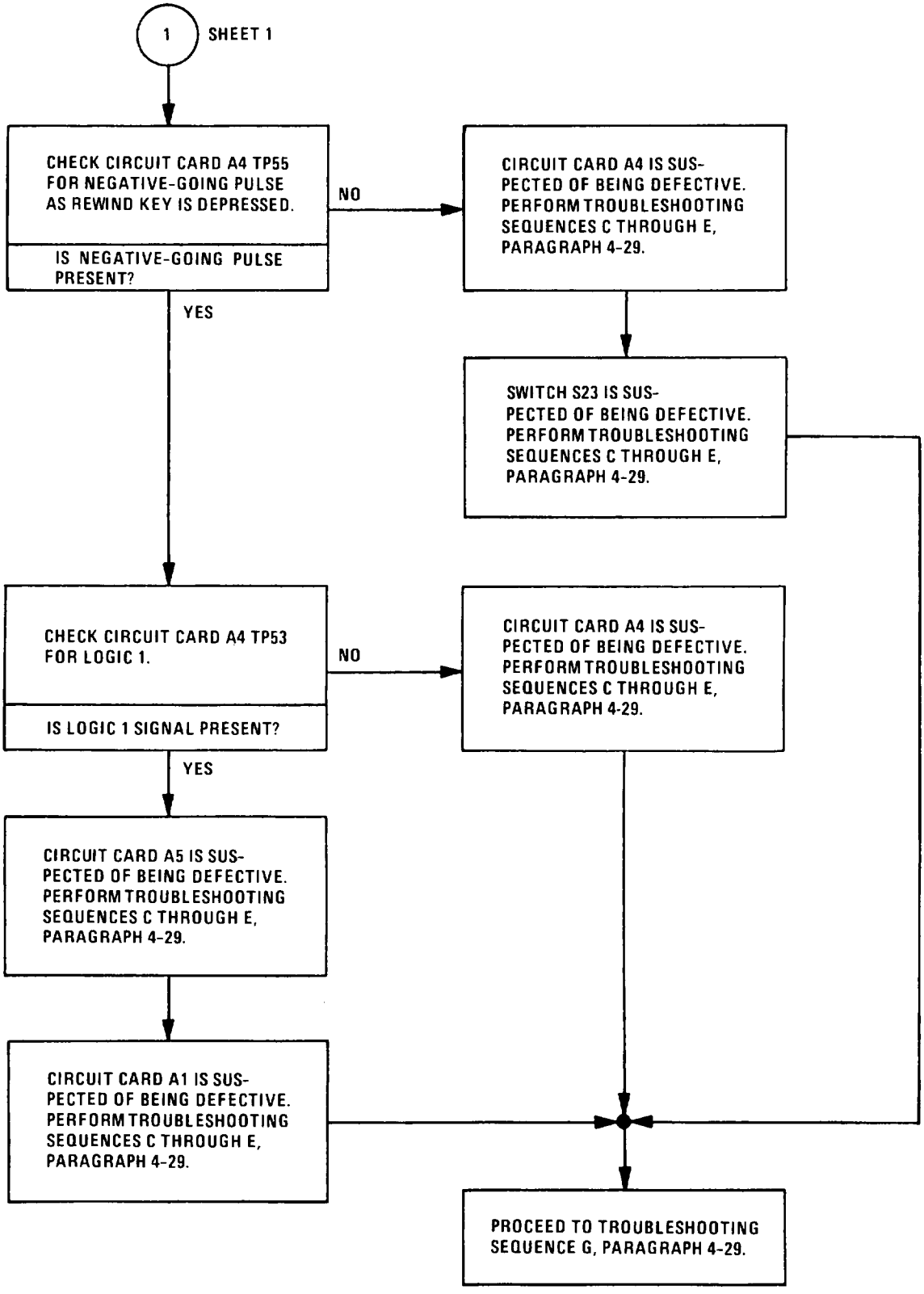
Troubleshooting Flow Chart - Entry Point BC (Sheet 2 of 3)



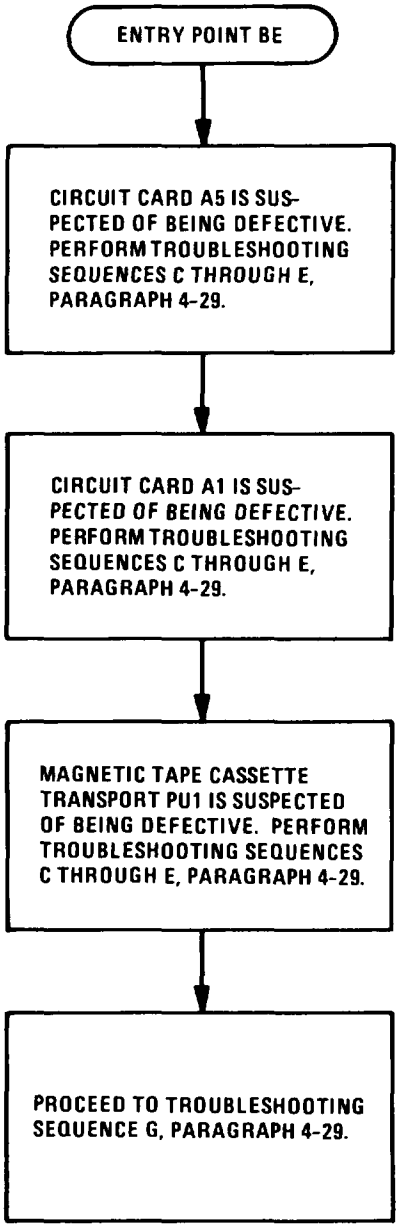
Troubleshooting Flow Chart - Entry Point BC (Sheet 3 of 3)



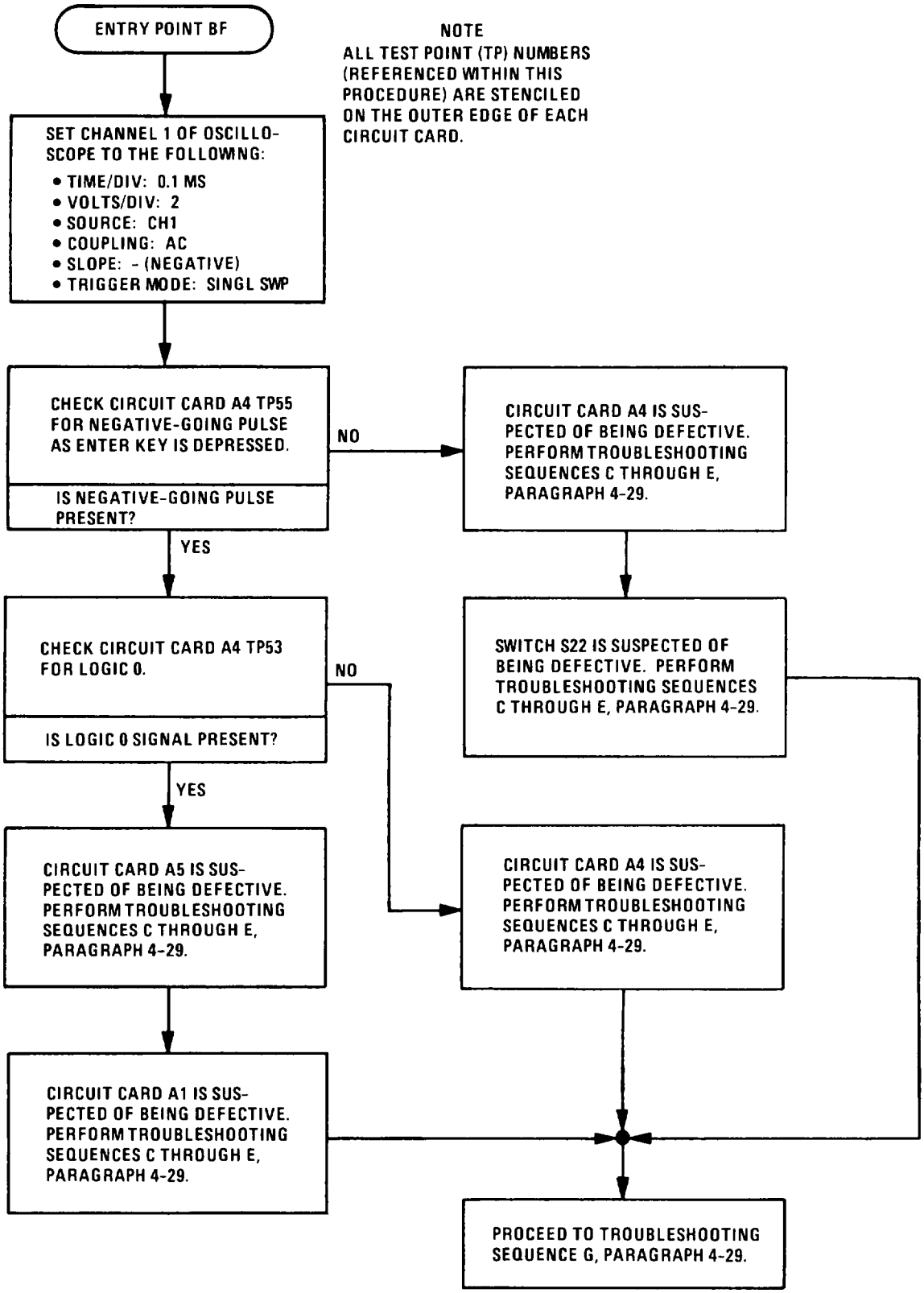
Troubleshooting Flow Chart - Entry Point BD (Sheet 1 of 2)



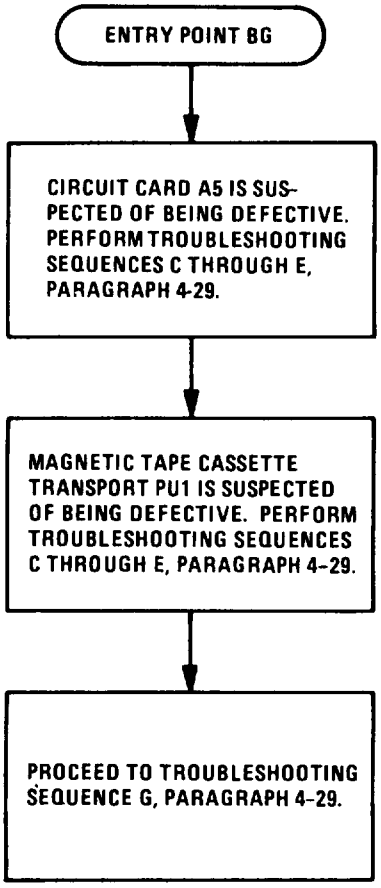
Troubleshooting Flow Chart - Entry Point BD (Sheet 2 of 2)



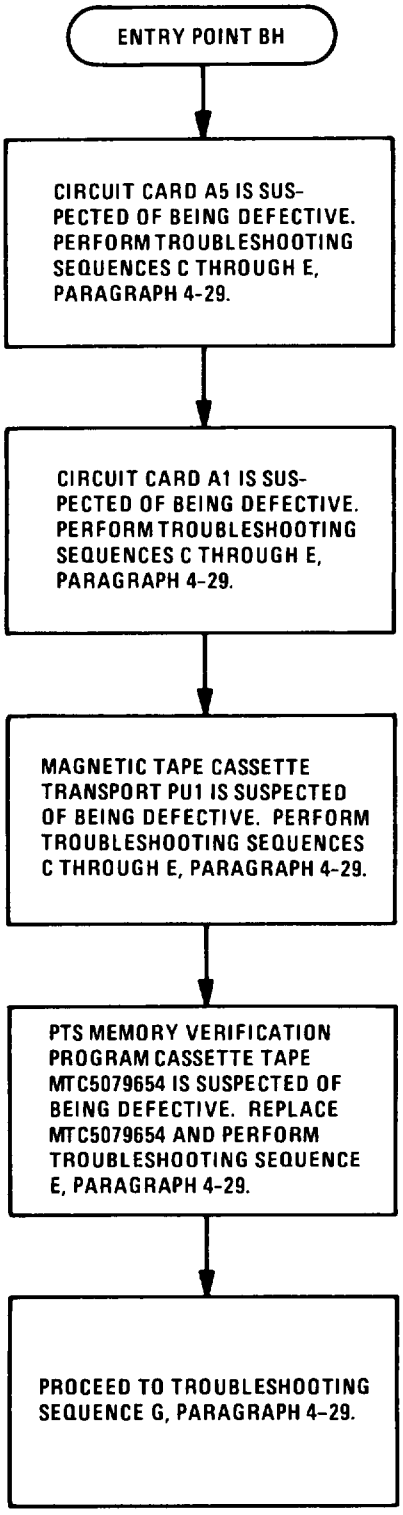
Troubleshooting Flow Chart - Entry Point BE



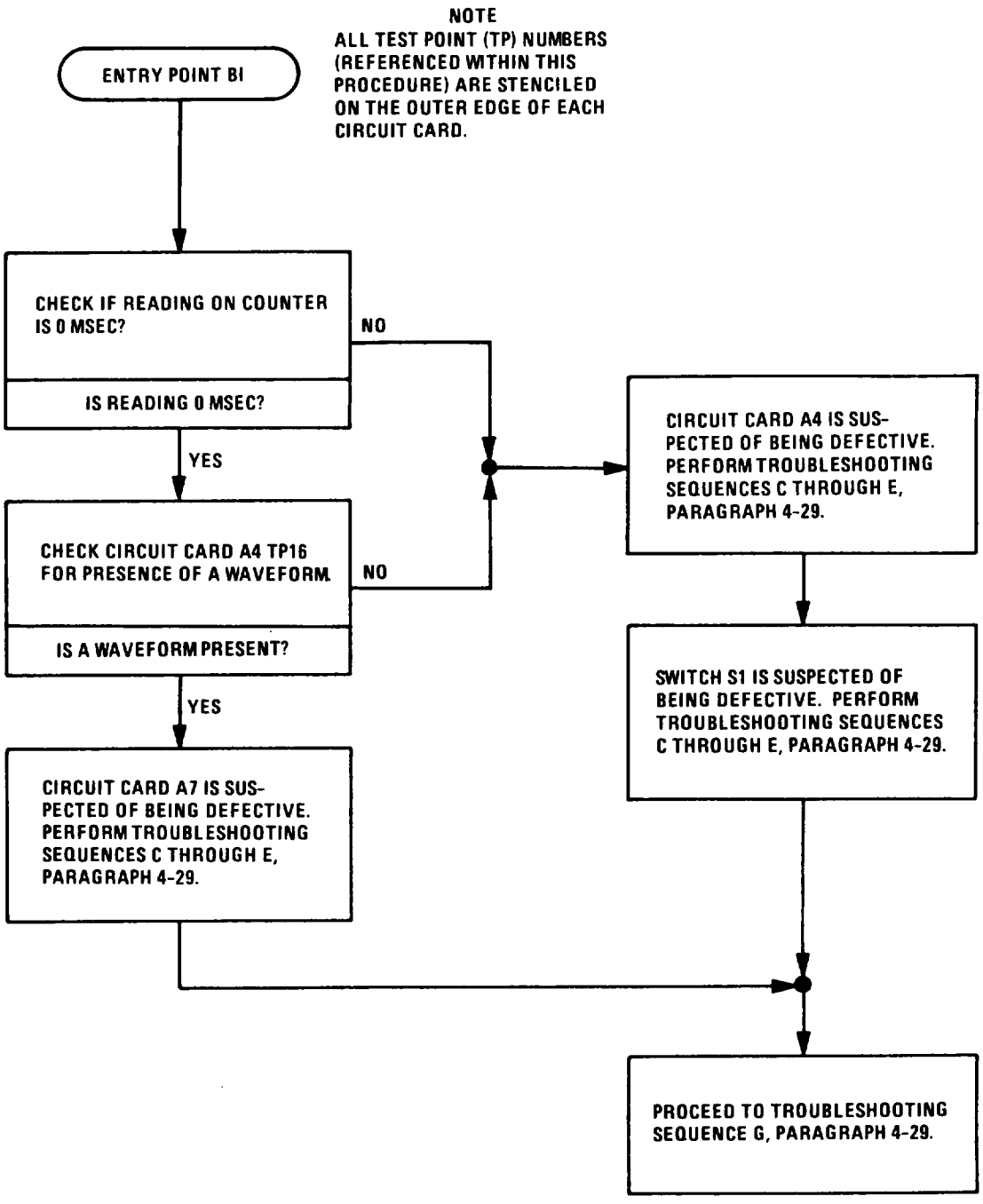
Troubleshooting Flow Chart - Entry Point BF



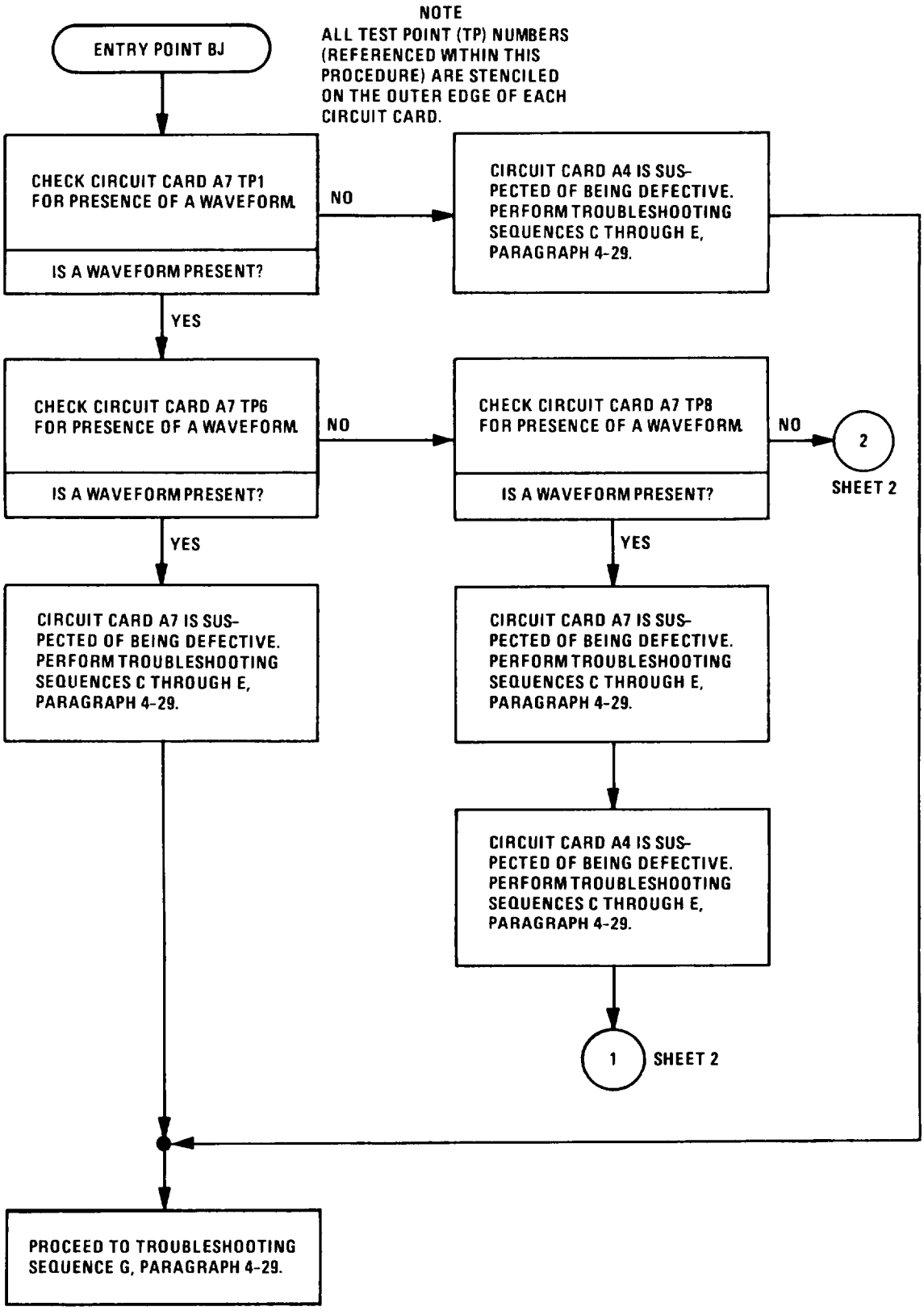
Troubleshooting Flow Chart - Entry Point BG



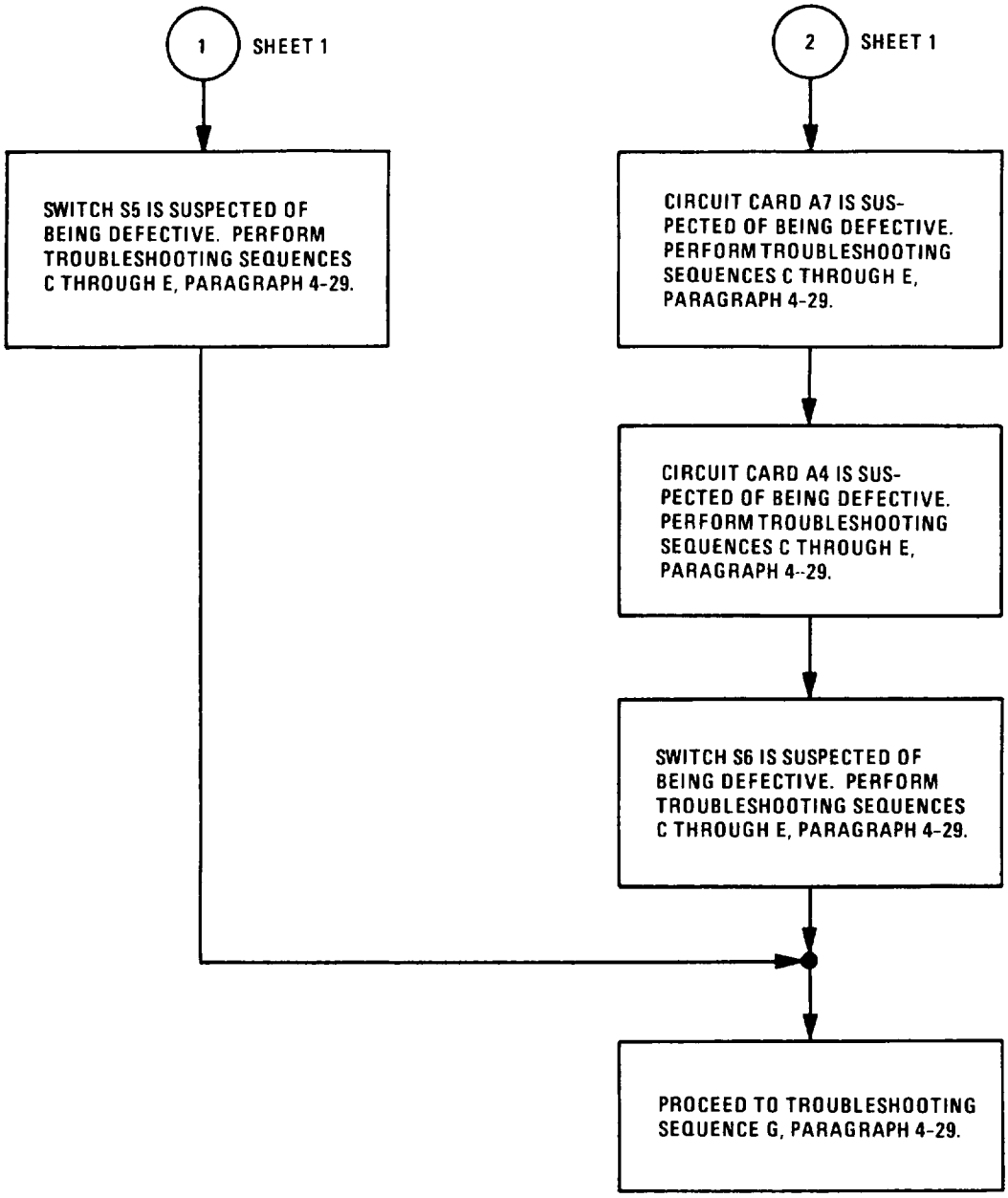
Troubleshooting Flow Chart - Entry Point BH



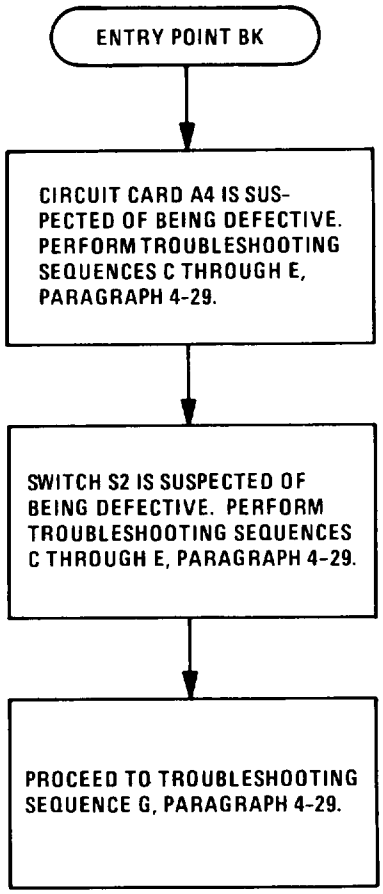
Troubleshooting Flow Chart - Entry Point BI



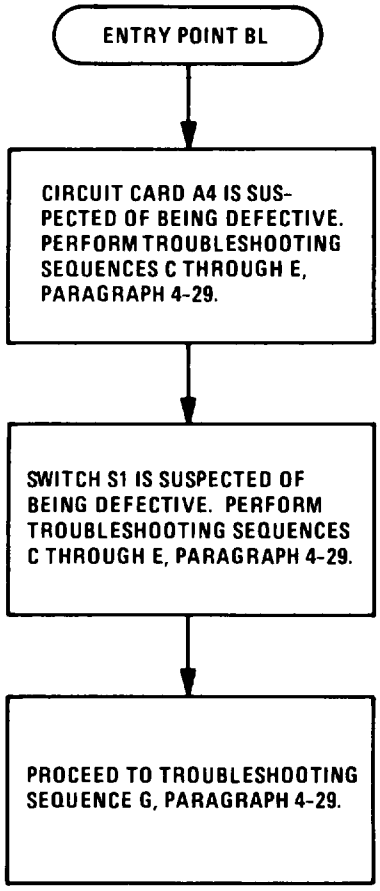
Troubleshooting Flow Chart - Entry Point BJ (Sheet 1 of 2)



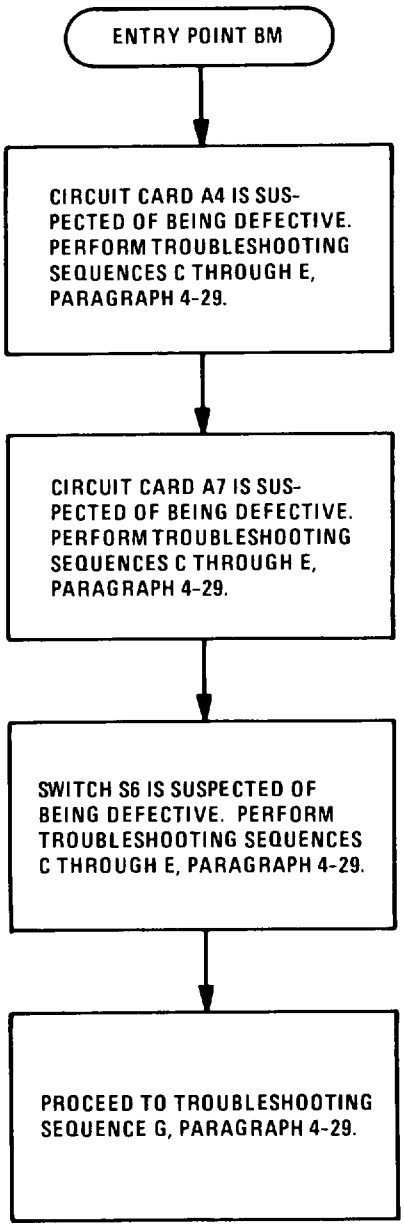
Troubleshooting Flow Chart - Entry Point BJ (Sheet 2 of 2)



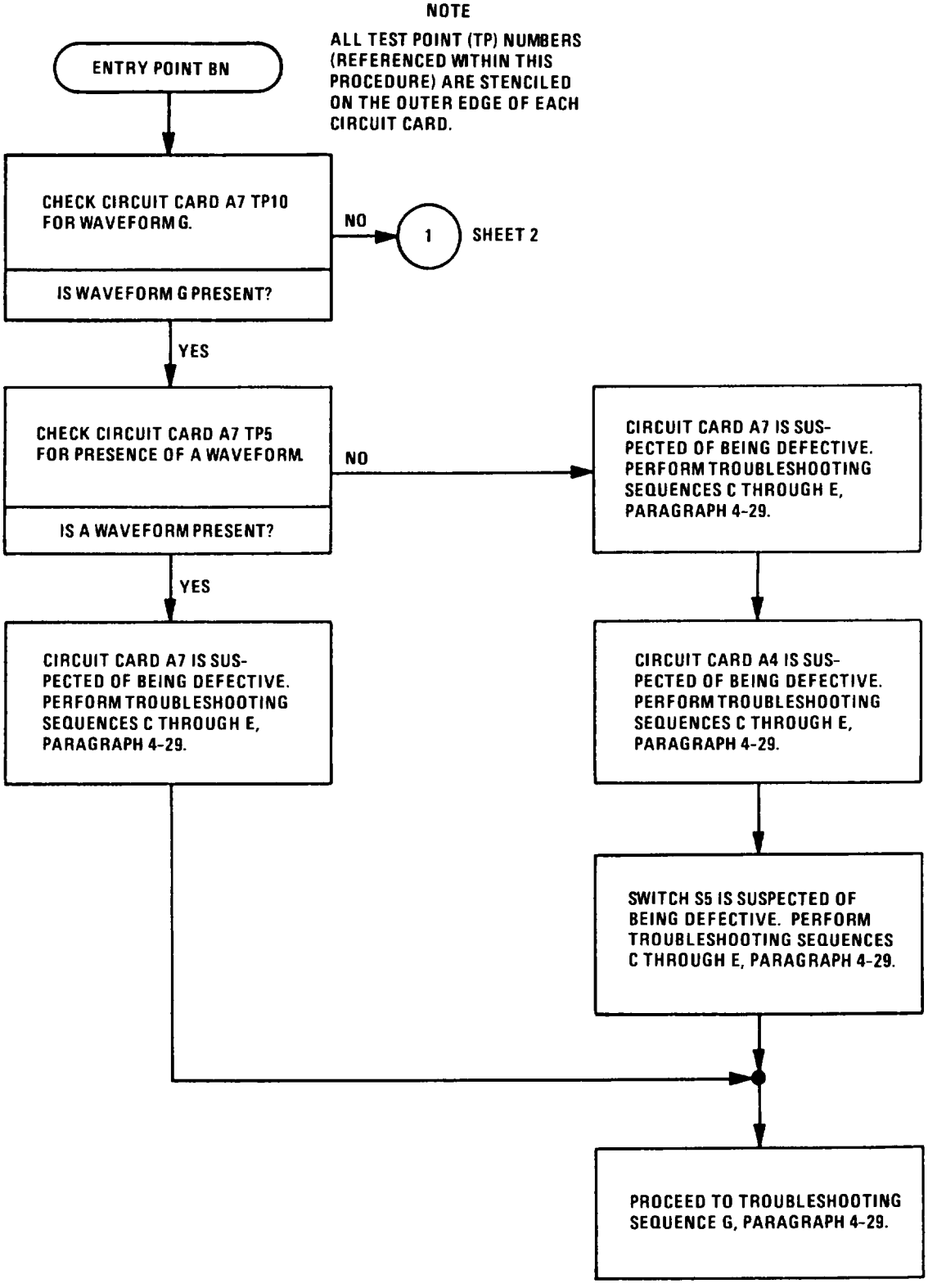
Troubleshooting Flow Chart - Entry Point BK



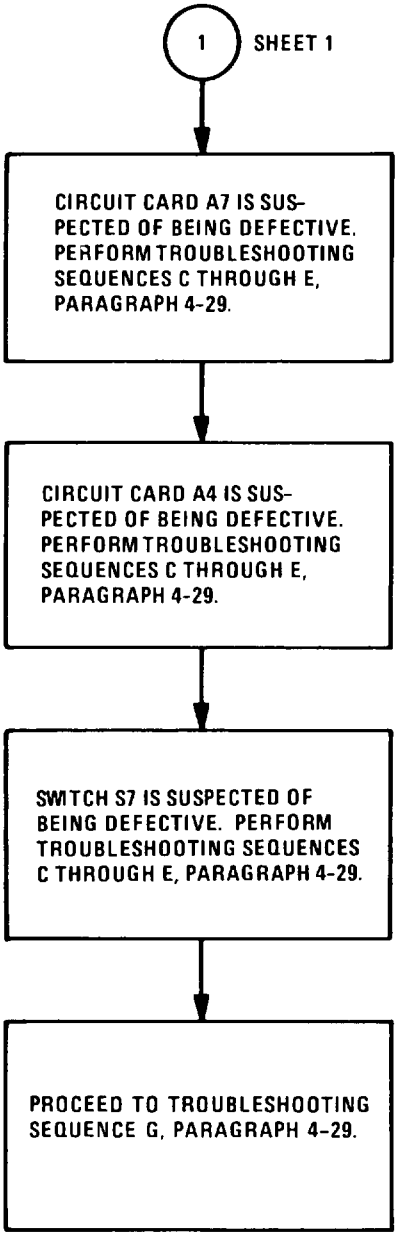
Troubleshooting Flow Chart - Entry Point BL



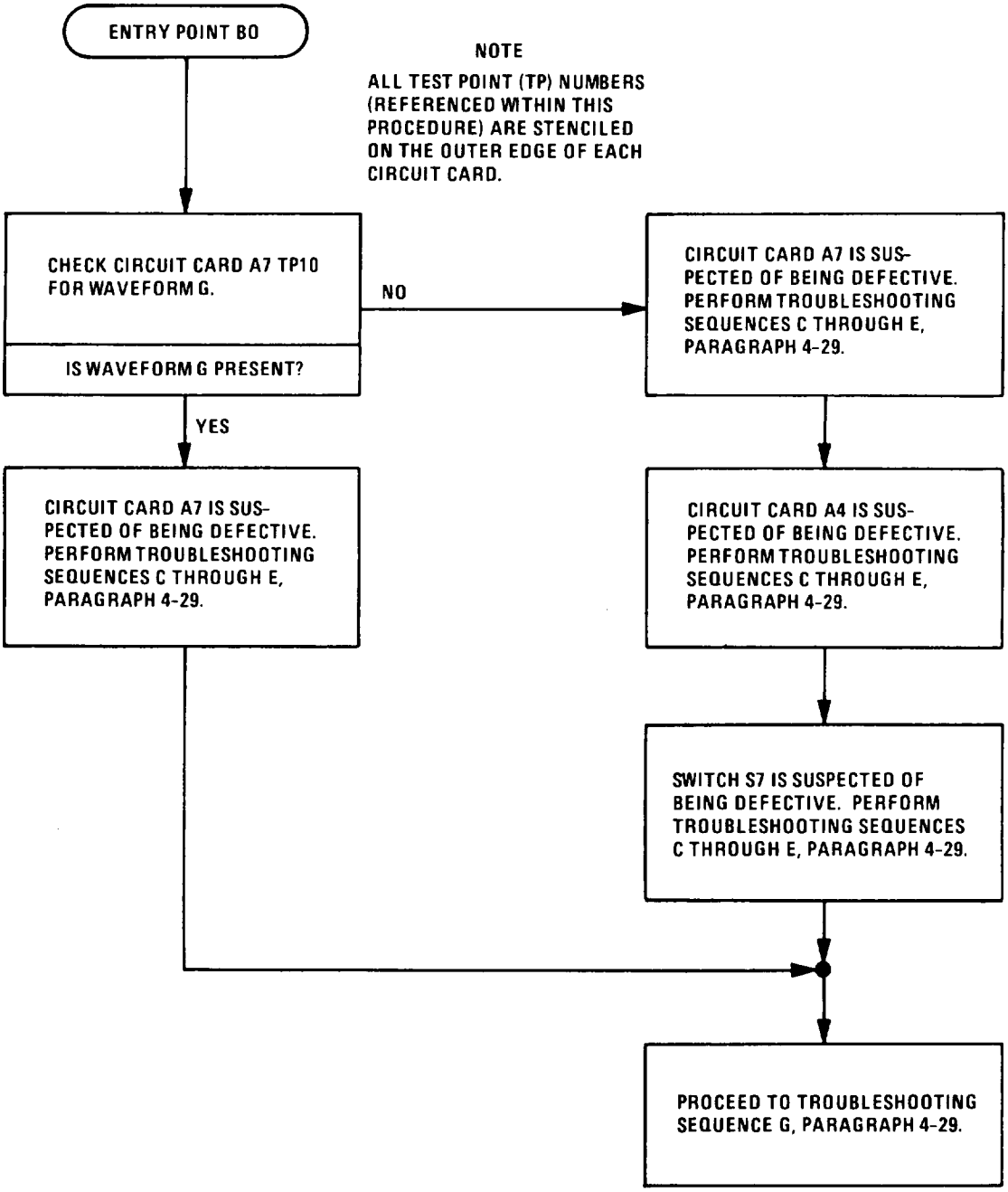
Troubleshooting Flow Chart - Entry Point BM



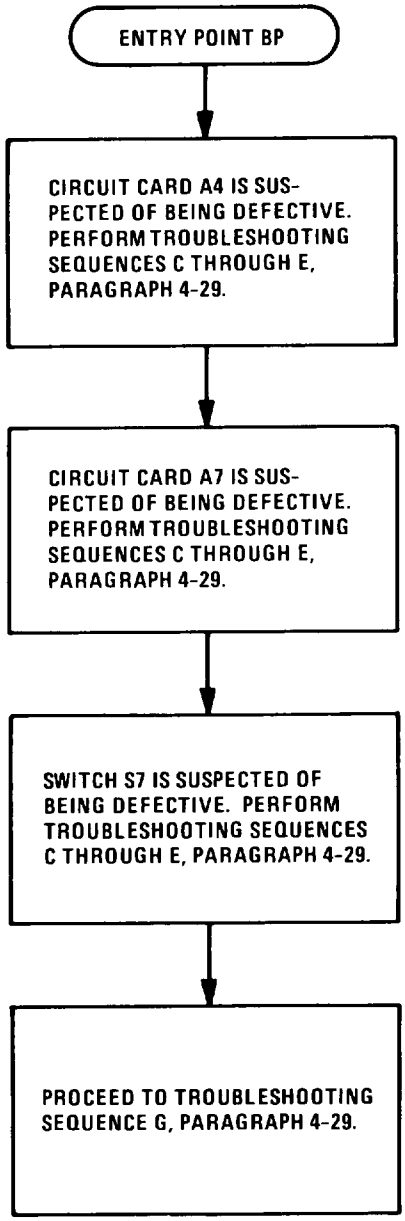
Troubleshooting Flow Chart - Entry Point BN (Sheet 1 of 2)



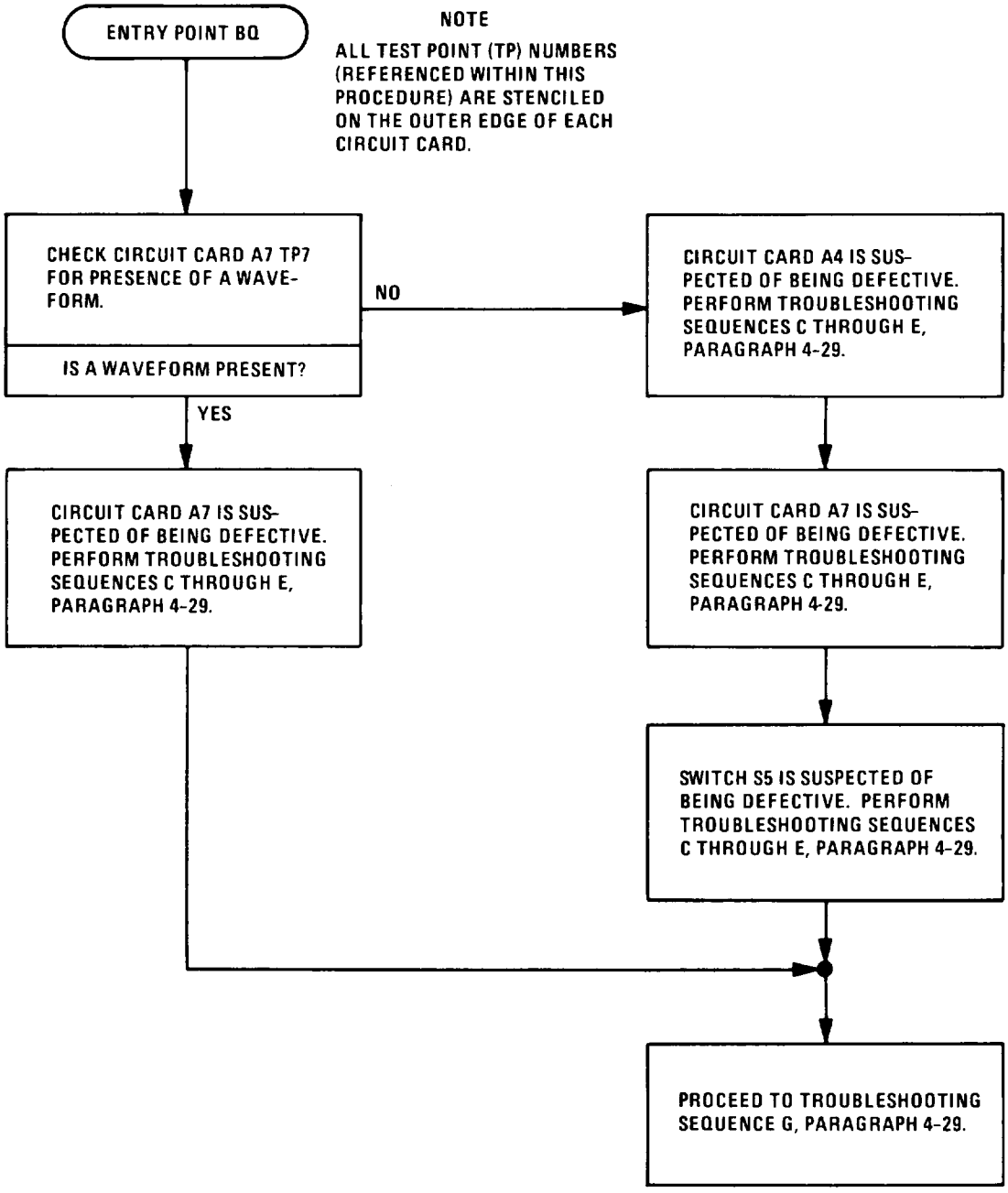
Troubleshooting Flow Chart - Entry Point BN (Sheet 2 of 2)



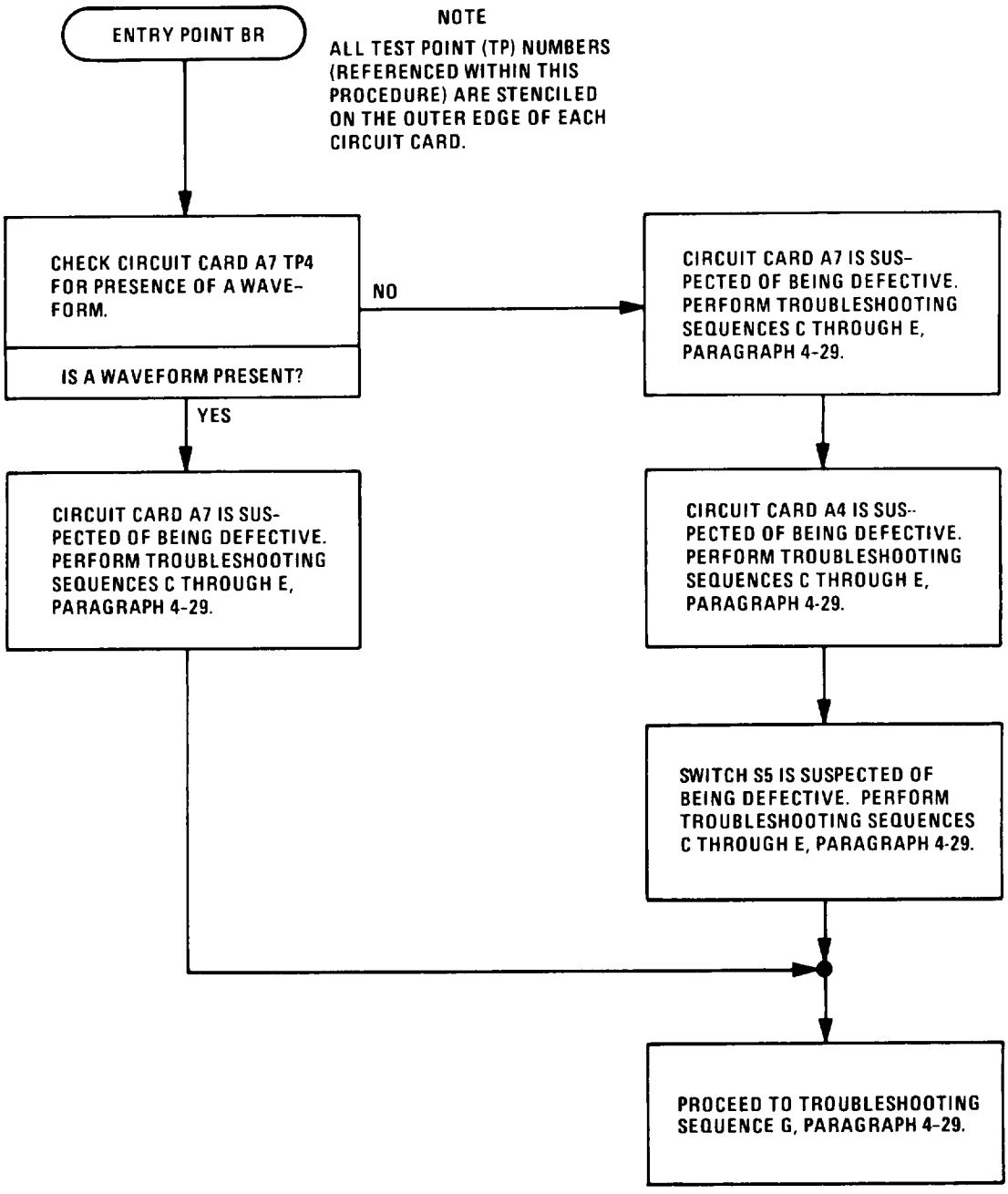
Troubleshooting Flow Chart - Entry Point BO



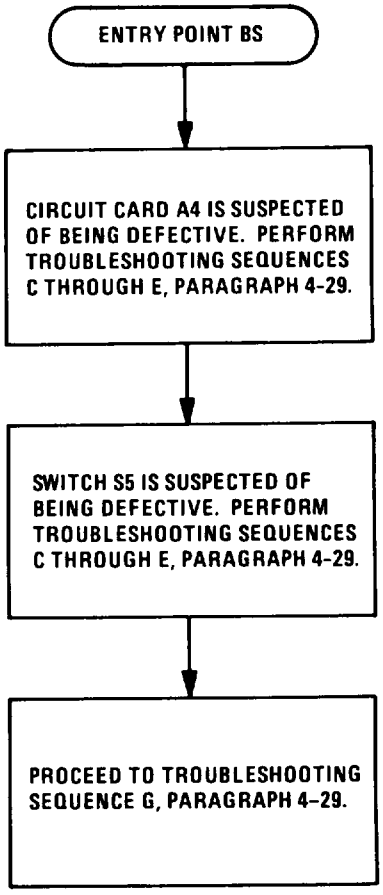
Troubleshooting Flow Chart - Entry Point BP



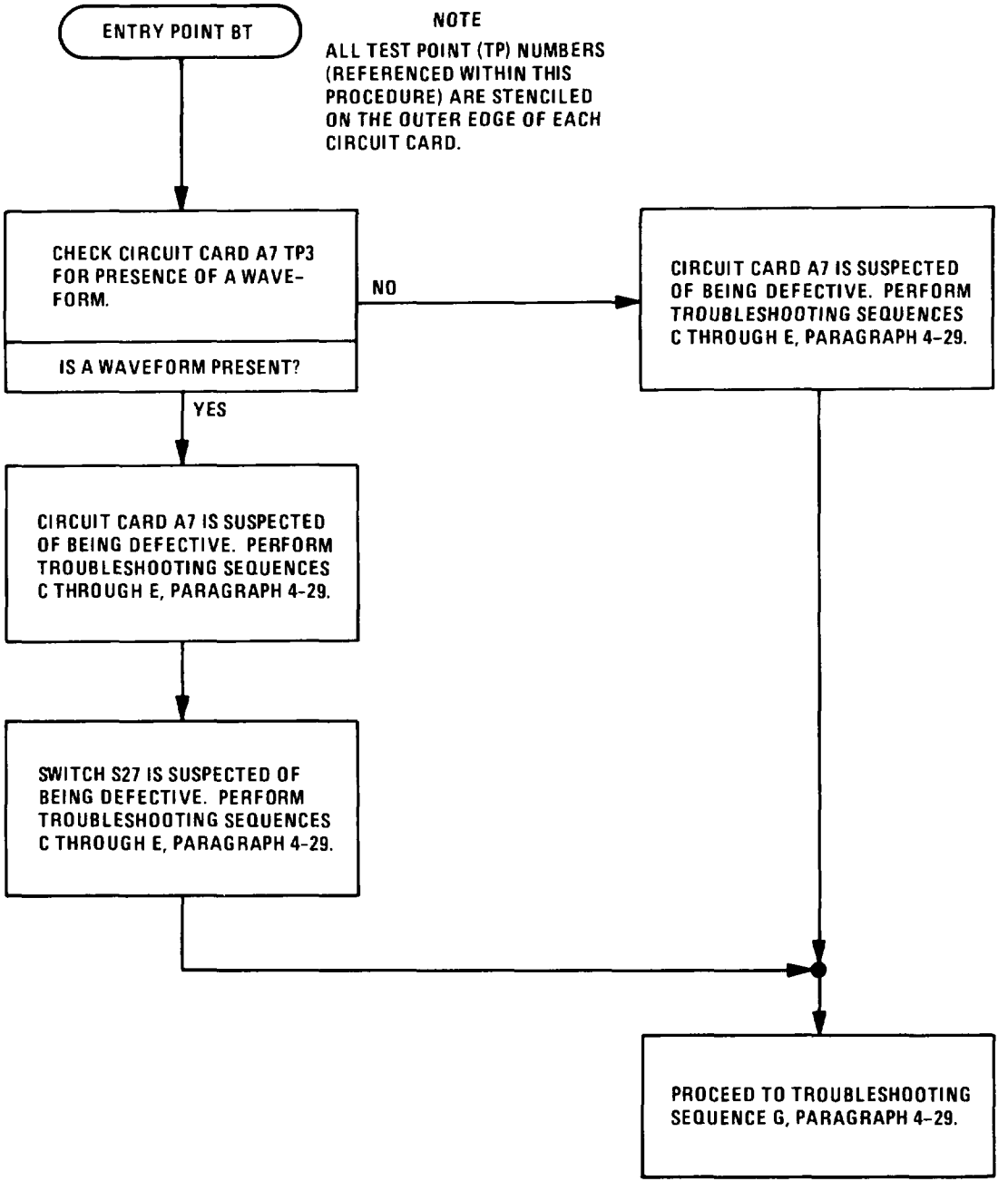
Troubleshooting Flow Chart - Entry Point BQ



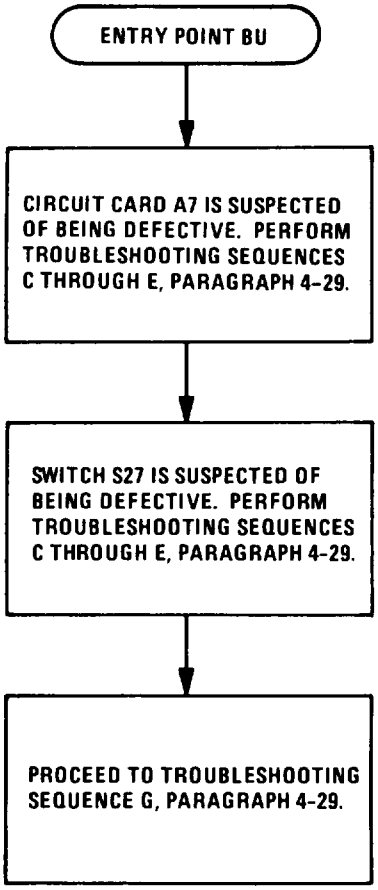
Troubleshooting Flow Chart - Entry Point BR



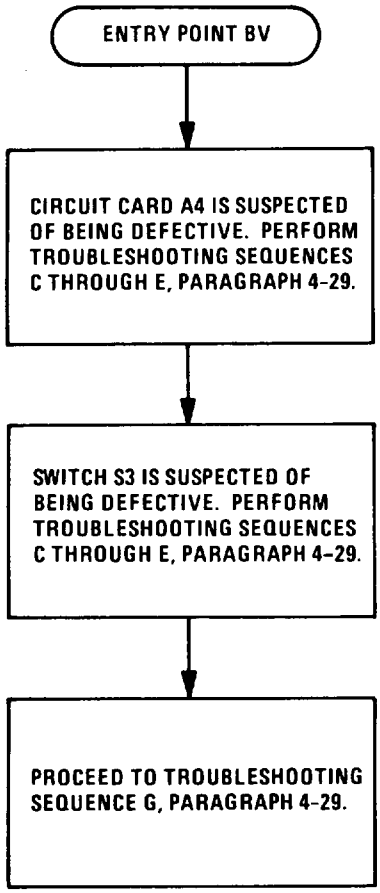
Troubleshooting Flow Chart - Entry Point BS



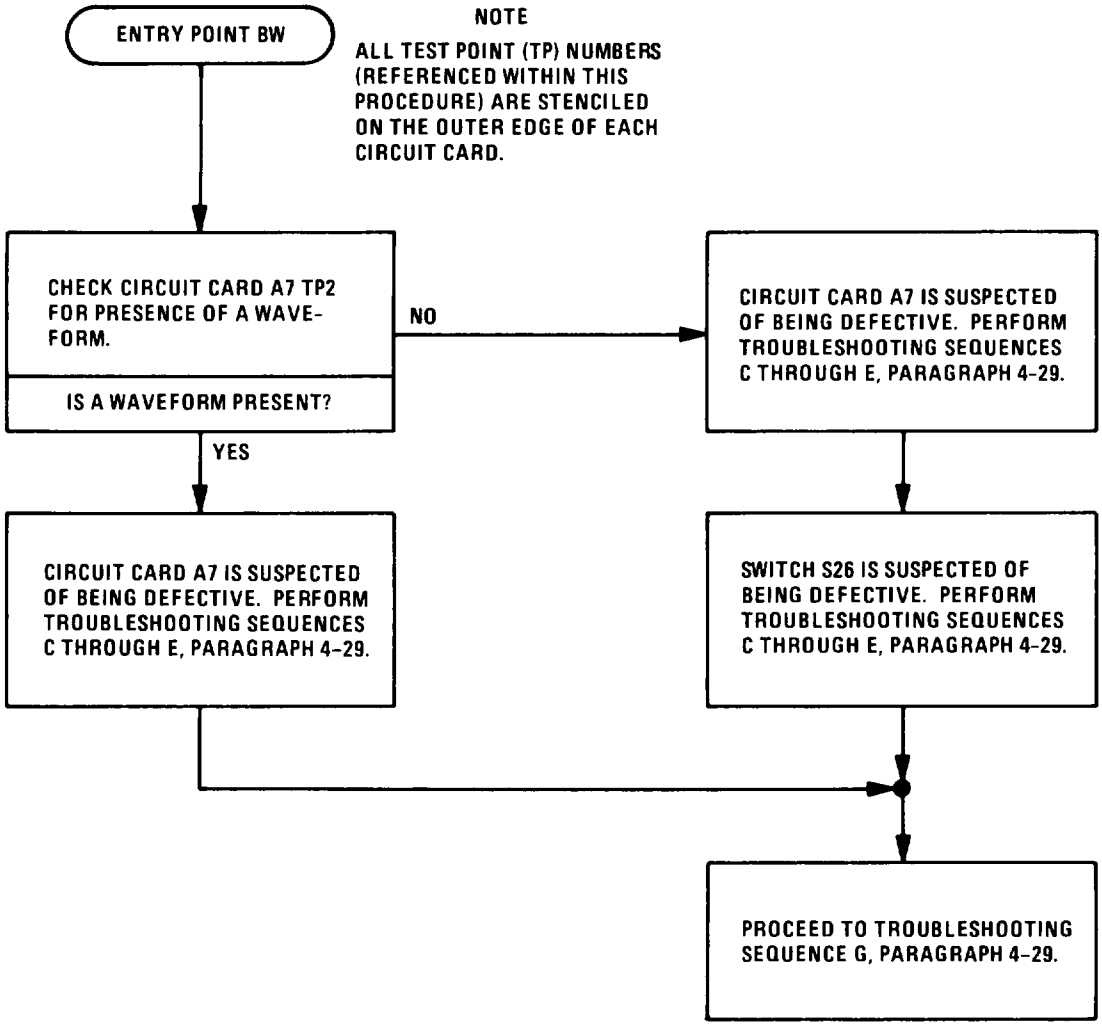
Troubleshooting Flow Chart - Entry Point BT



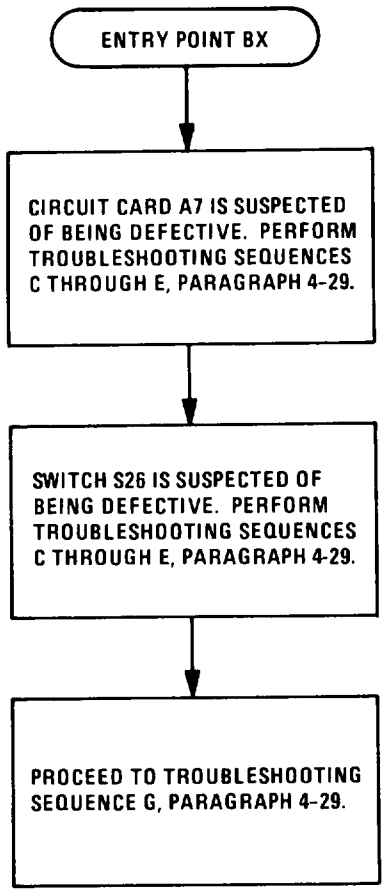
Troubleshooting Flow Chart - Entry Point BU



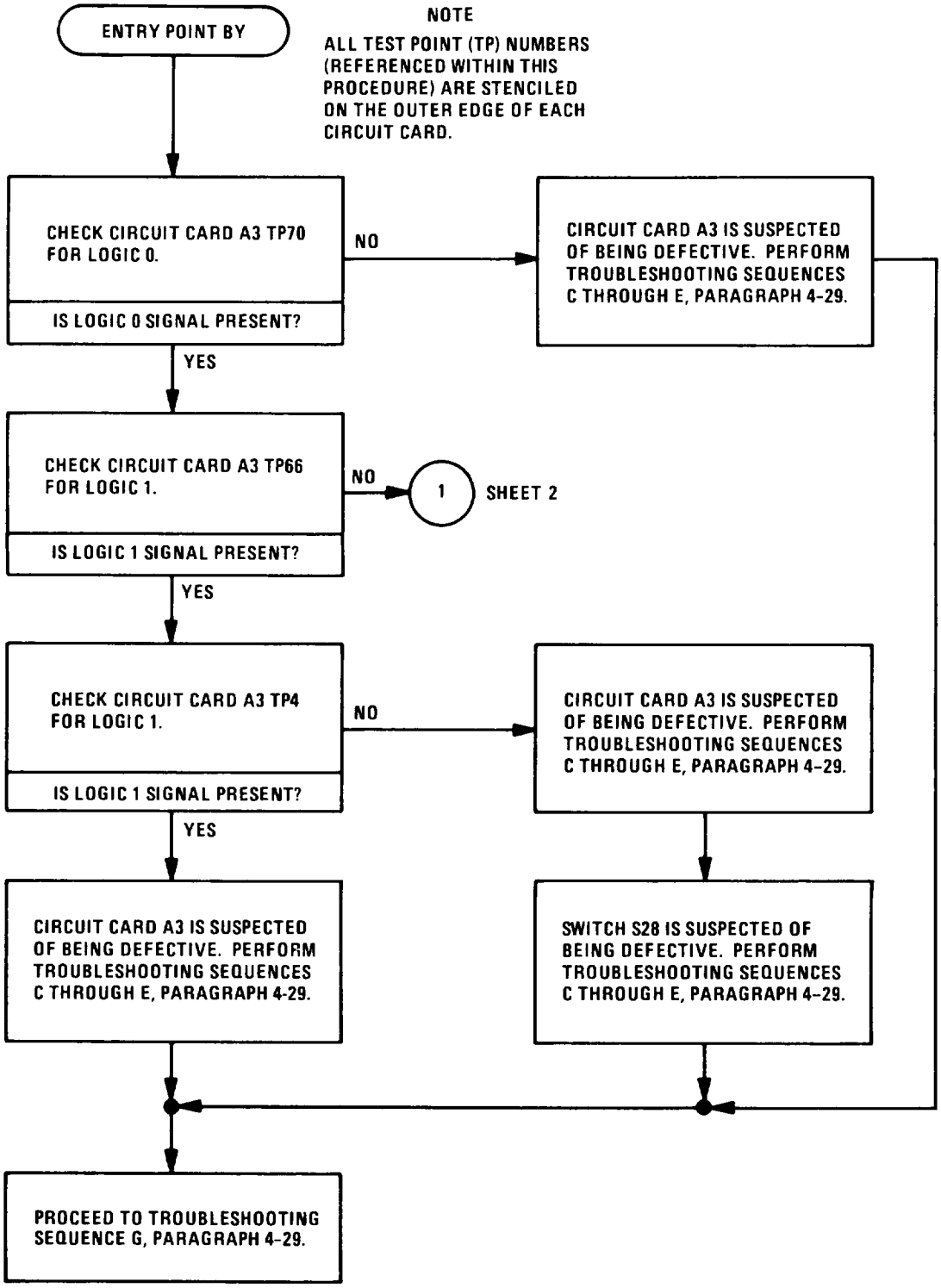
Troubleshooting Flow Chart - Entry Point BV



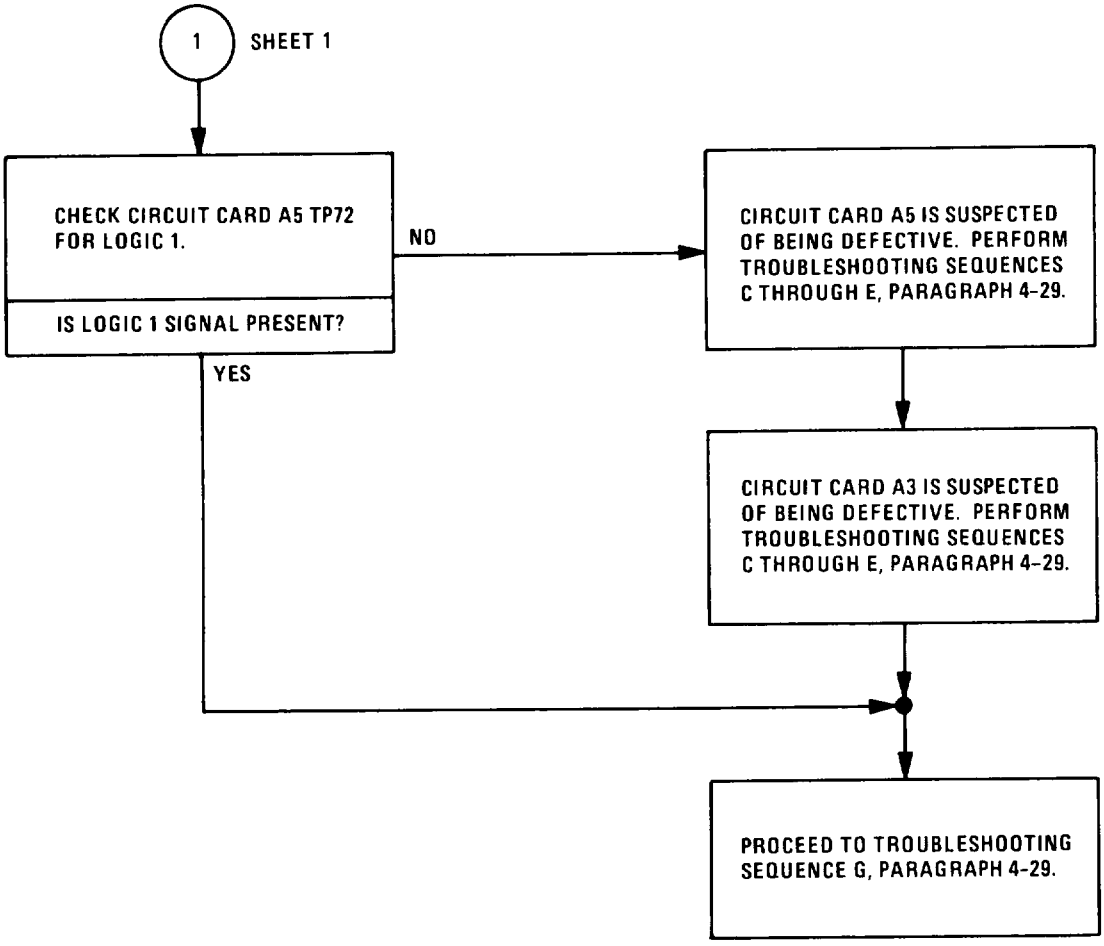
Troubleshooting Flow Chart - Entry Point BW



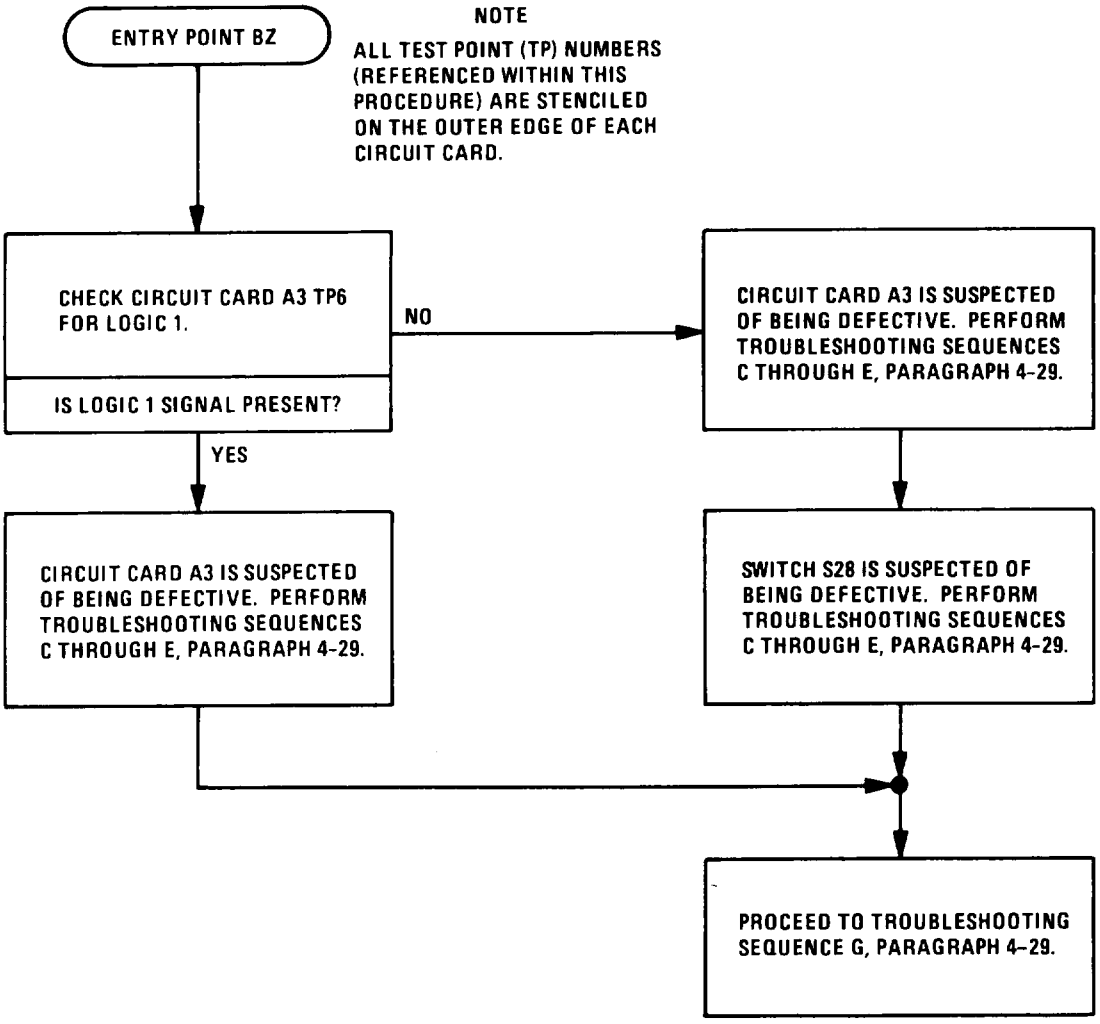
Troubleshooting Flow Chart - Entry Point BX



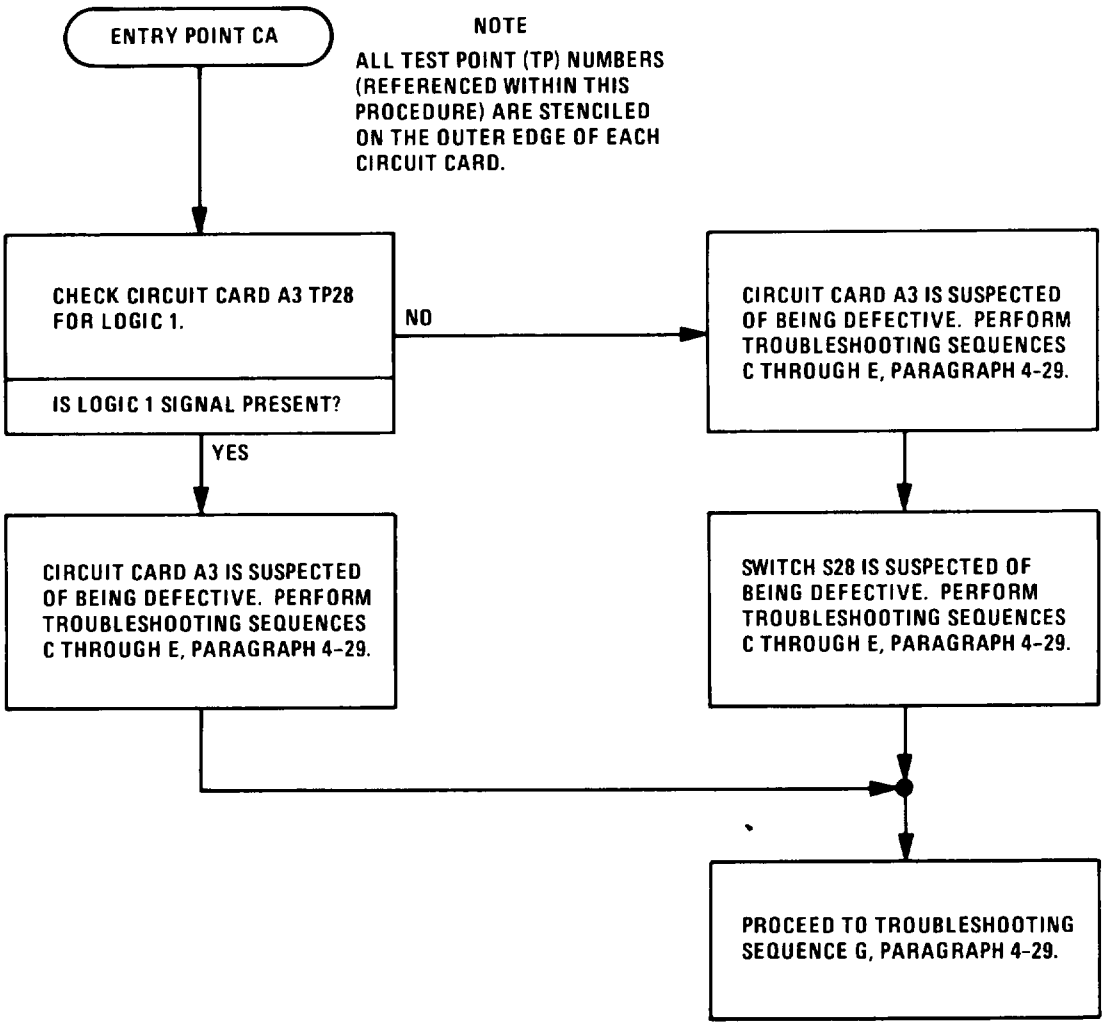
Troubleshooting Flow Chart - Entry Point BY (Sheet 1 of 2)



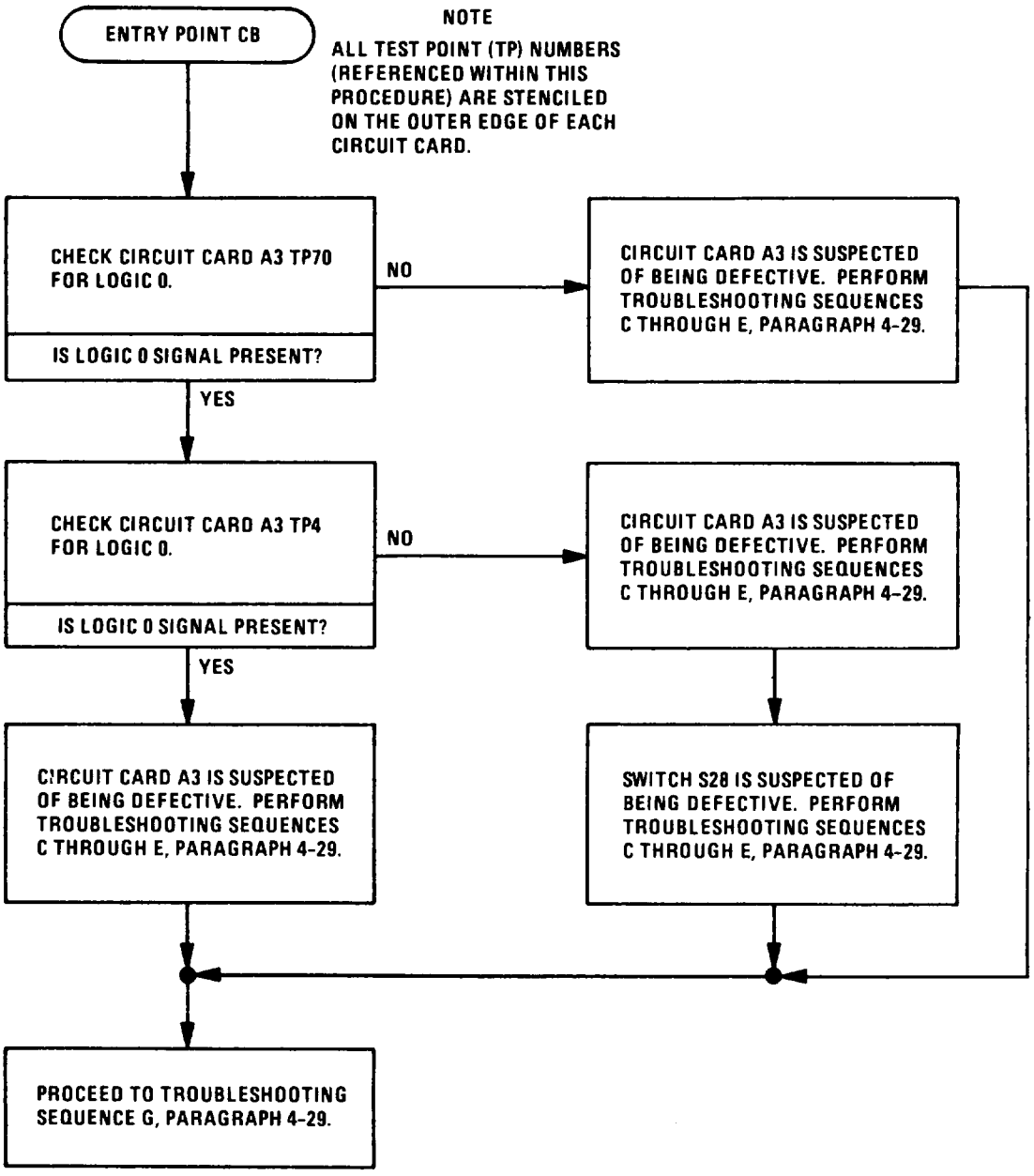
Troubleshooting Flow Chart - Entry Point BY (Sheet 2 of 2)



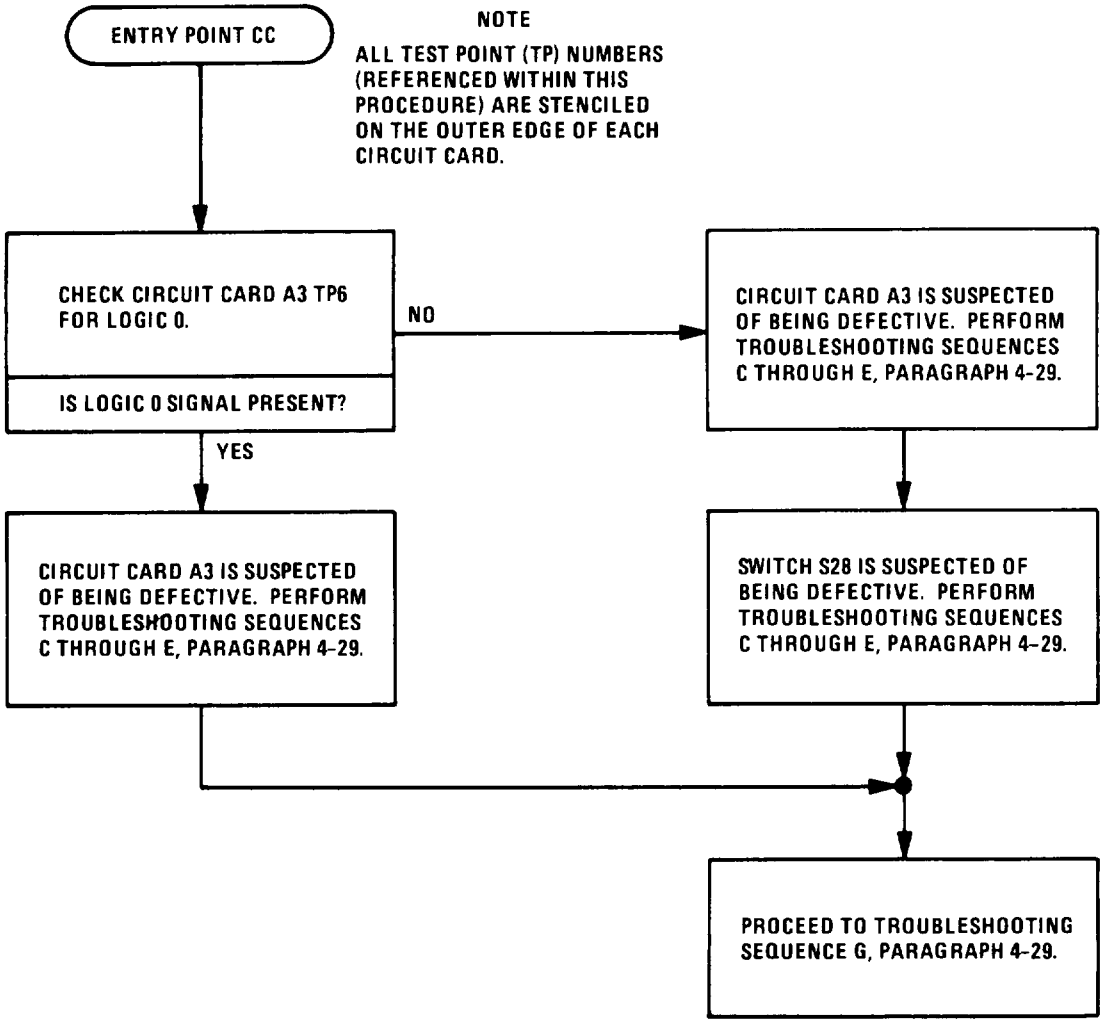
Troubleshooting Flow Chart - Entry Point BZ



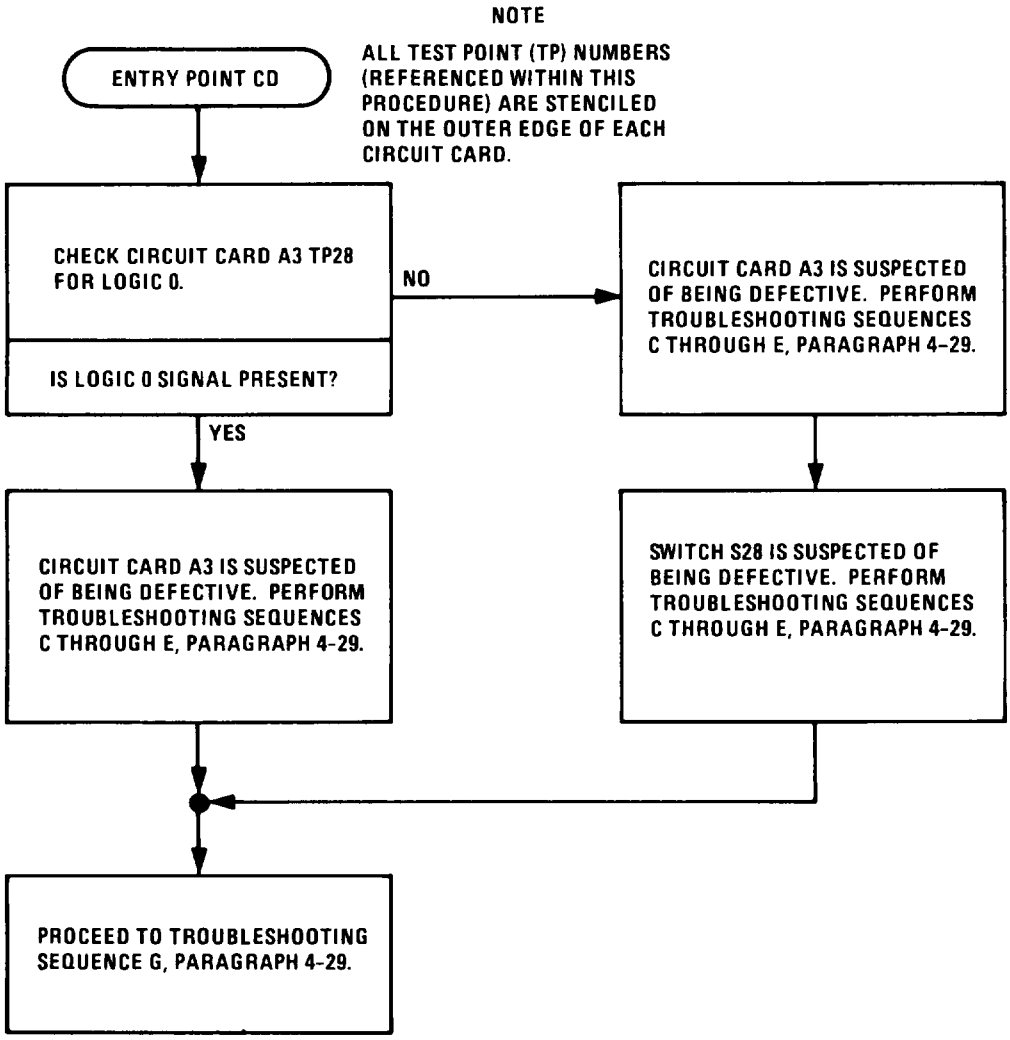
Troubleshooting Flow Chart - Entry Point CA



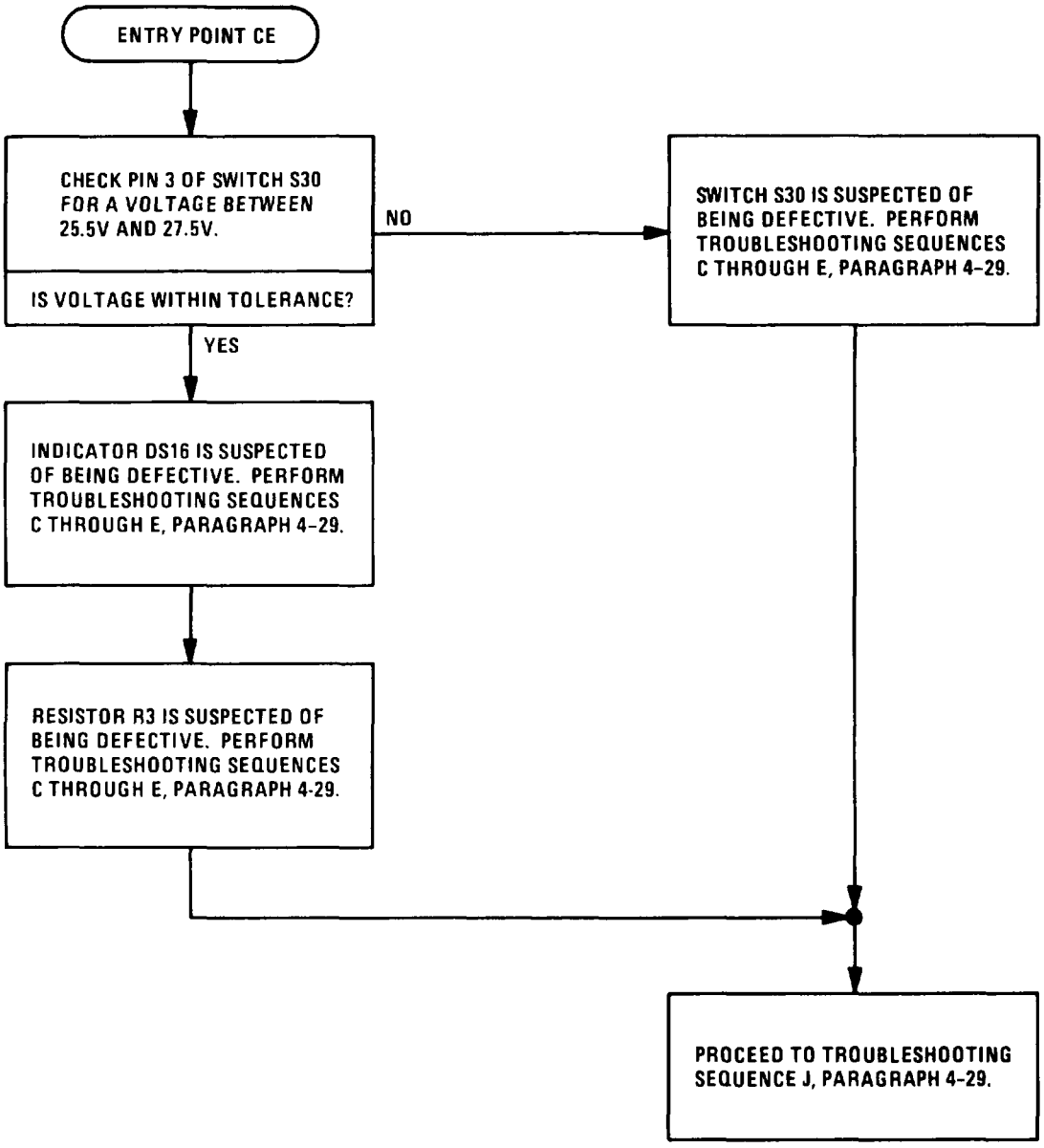
Troubleshooting Flow Chart - Entry Point CB



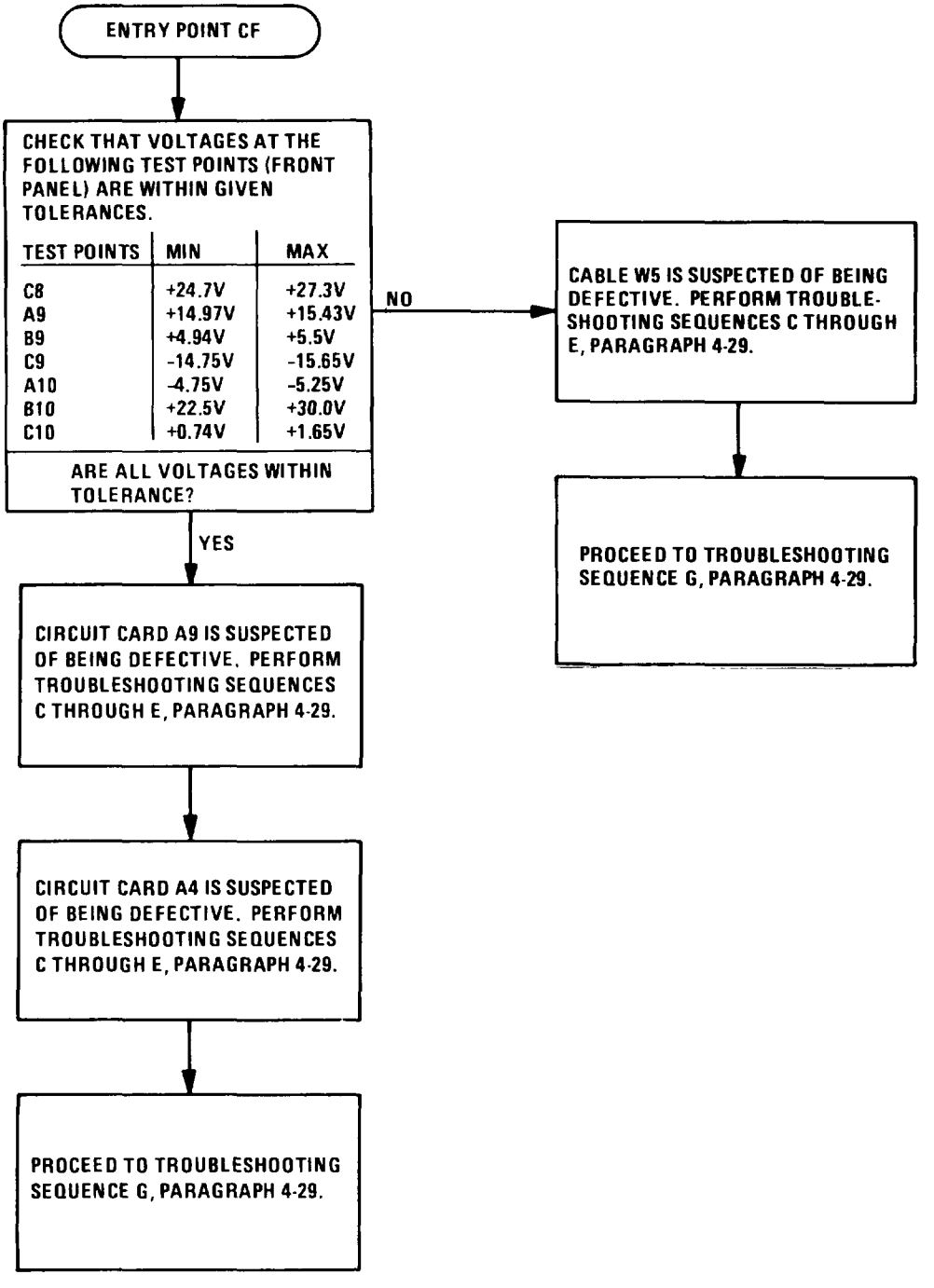
Troubleshooting Flow Chart - Entry Point CC



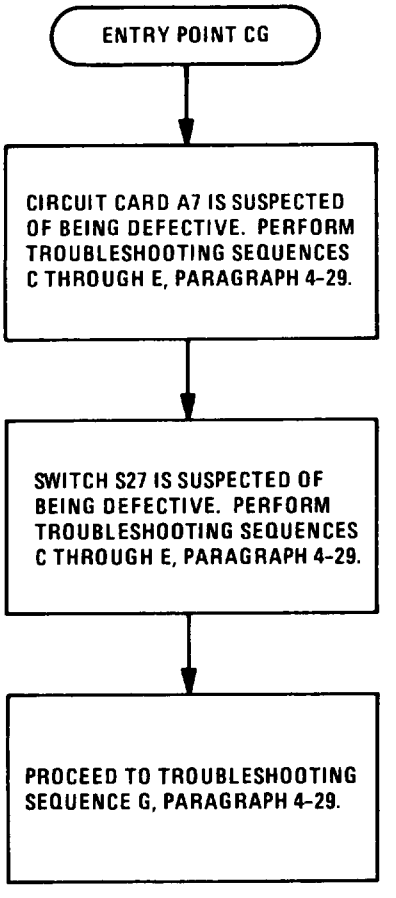
Troubleshooting Flow Chart - Entry Point CD



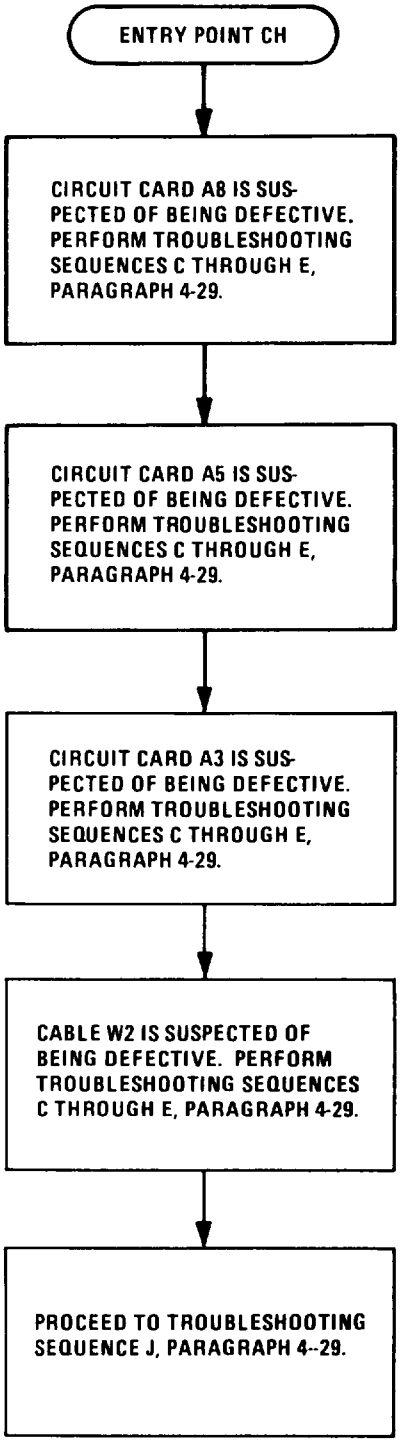
Troubleshooting Flow Chart - Entry Point CE



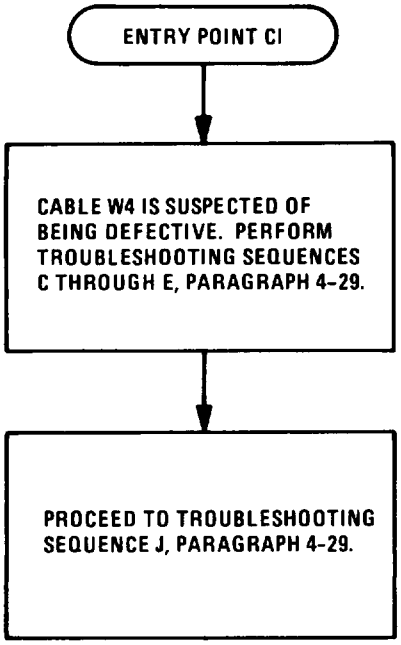
Troubleshooting Flow Chart - Entry Point CF



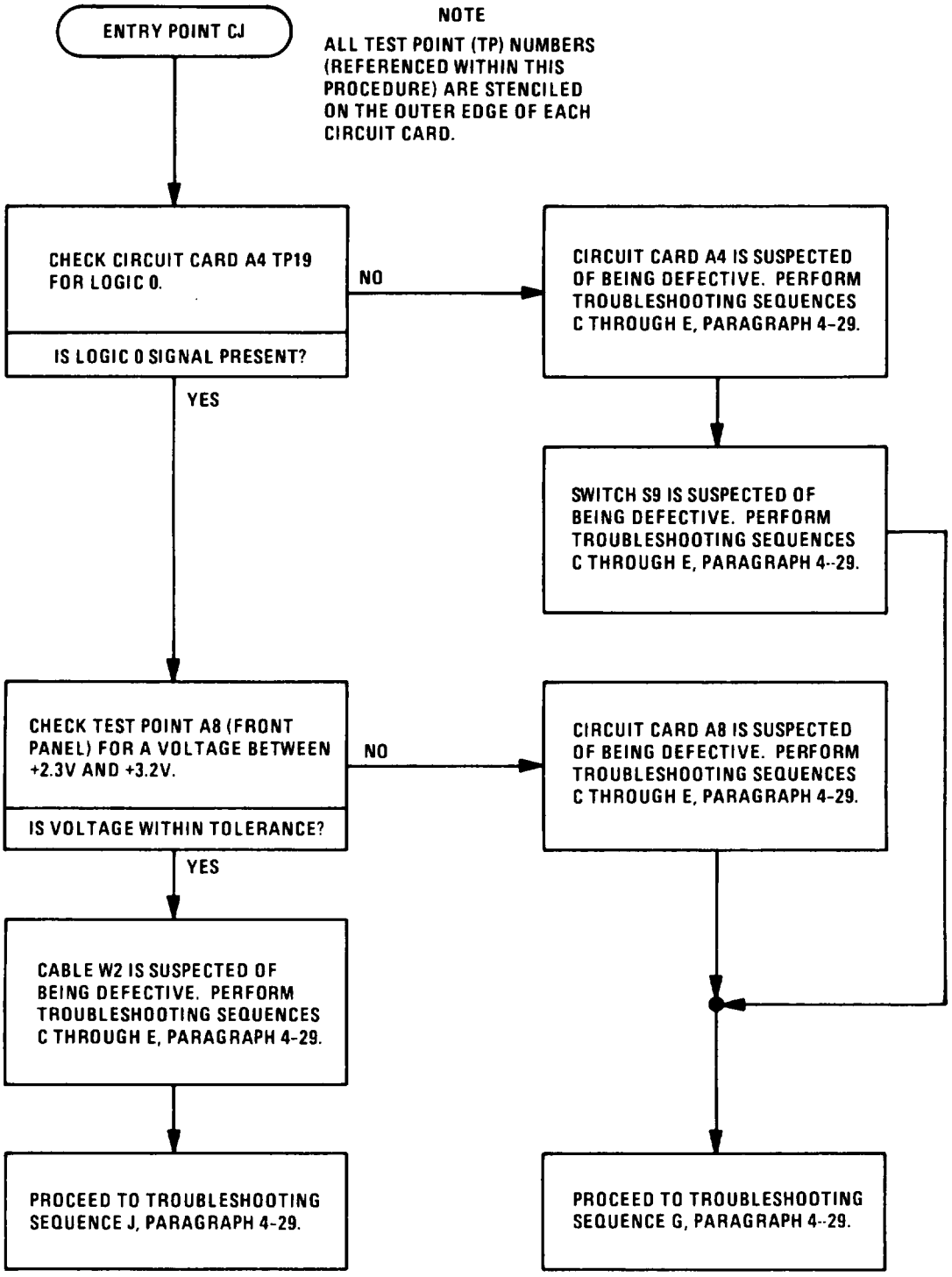
Troubleshooting Flow Chart - Entry Point CG



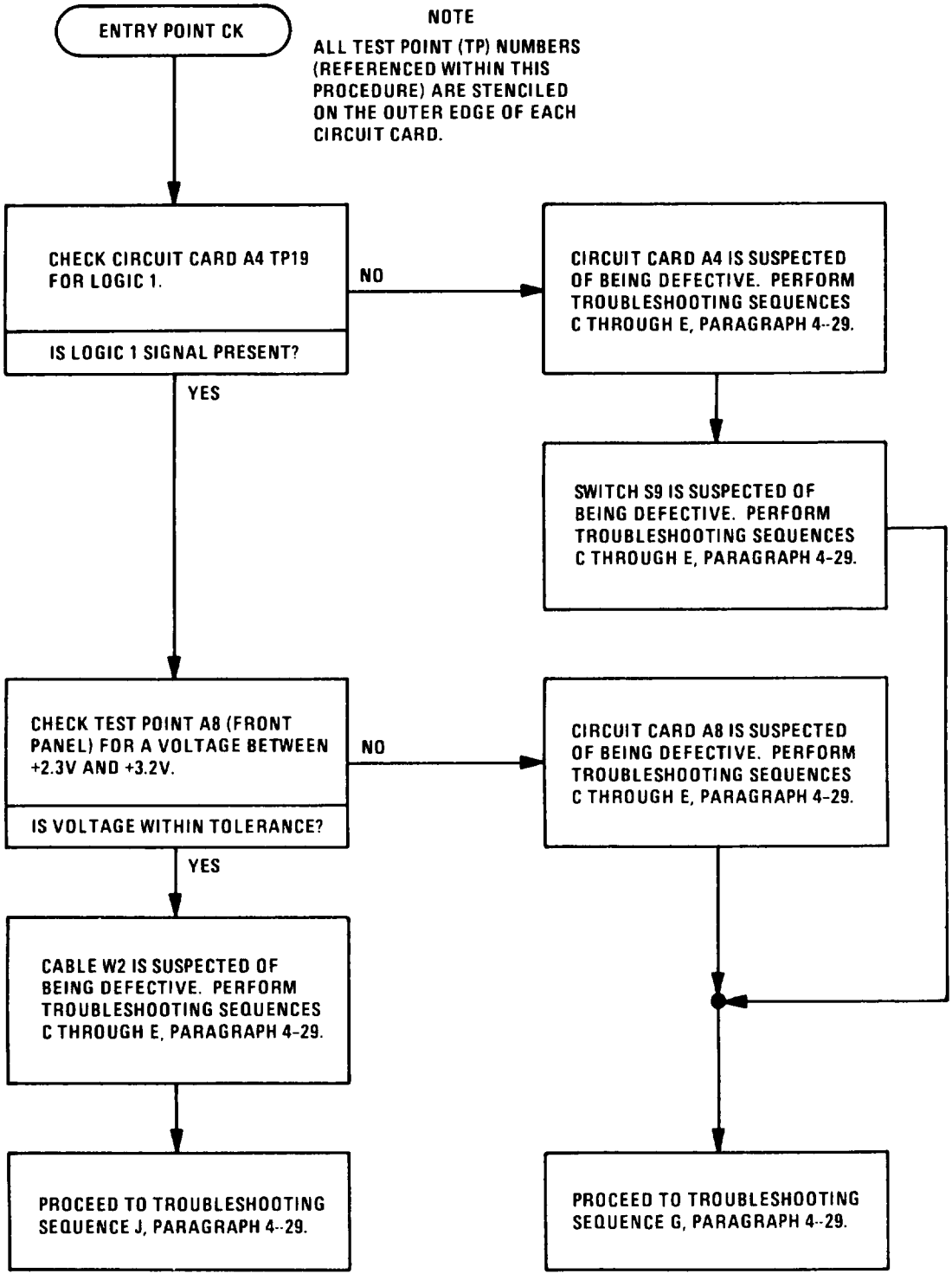
Troubleshooting Flow Chart - Entry Point CH



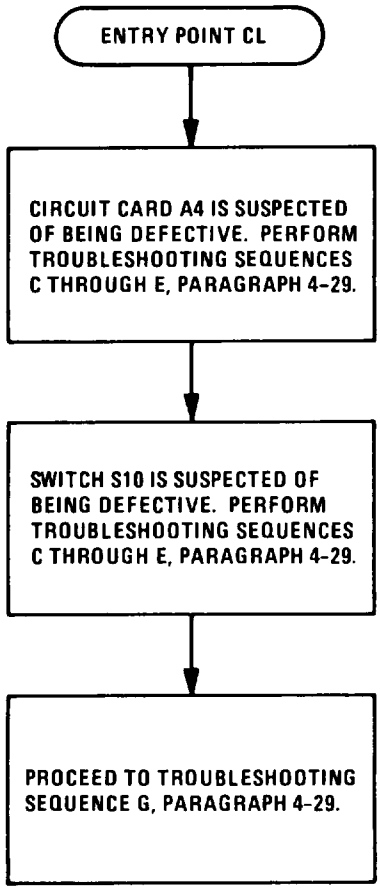
Troubleshooting Flow Chart - Entry Point CI



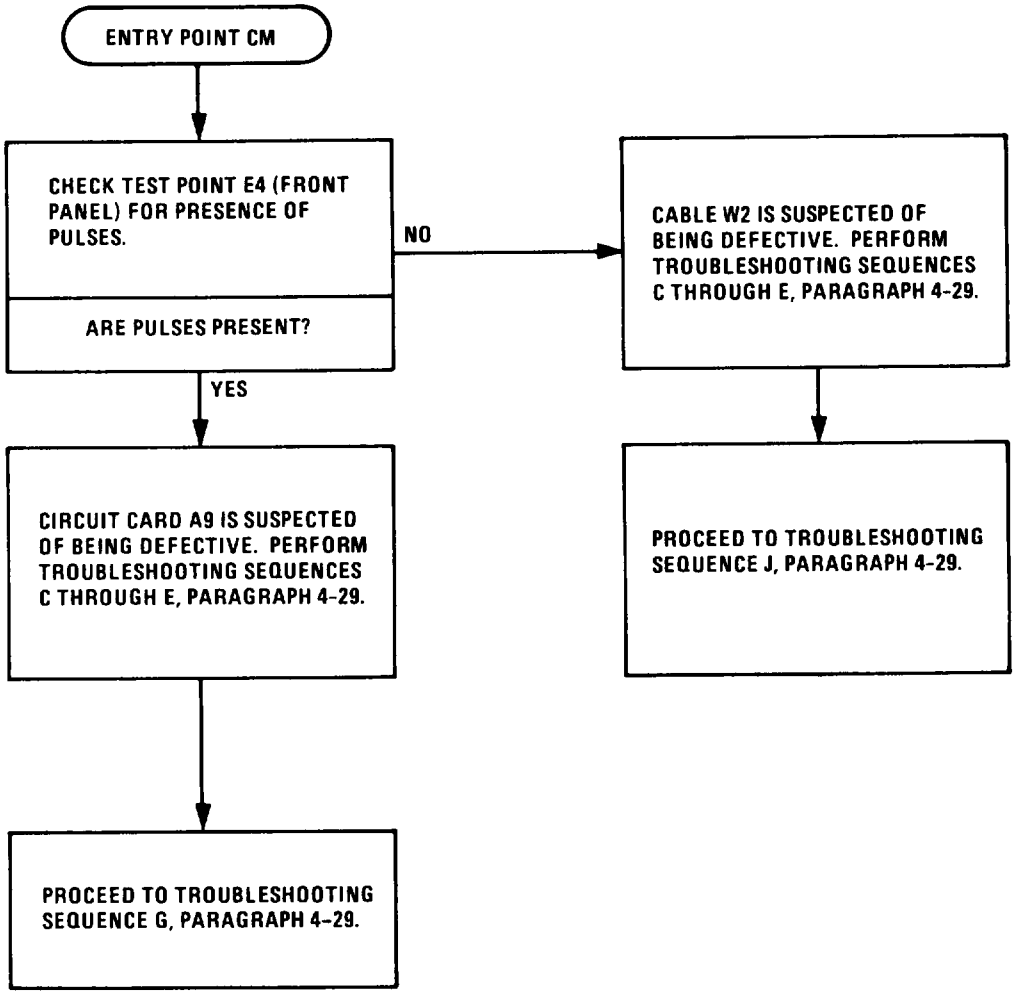
Troubleshooting Flow Chart - Entry Point CJ



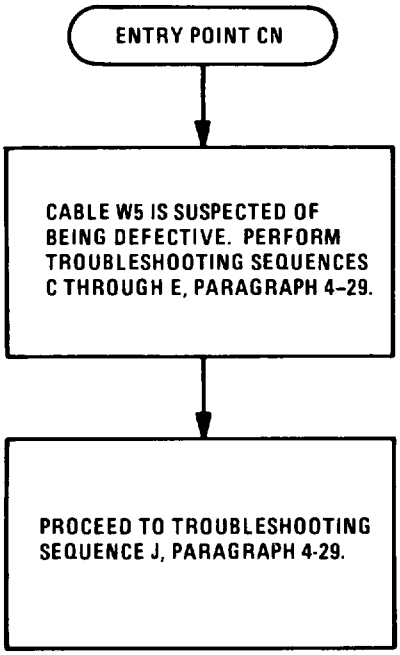
Troubleshooting Flow Chart - Entry Point CK



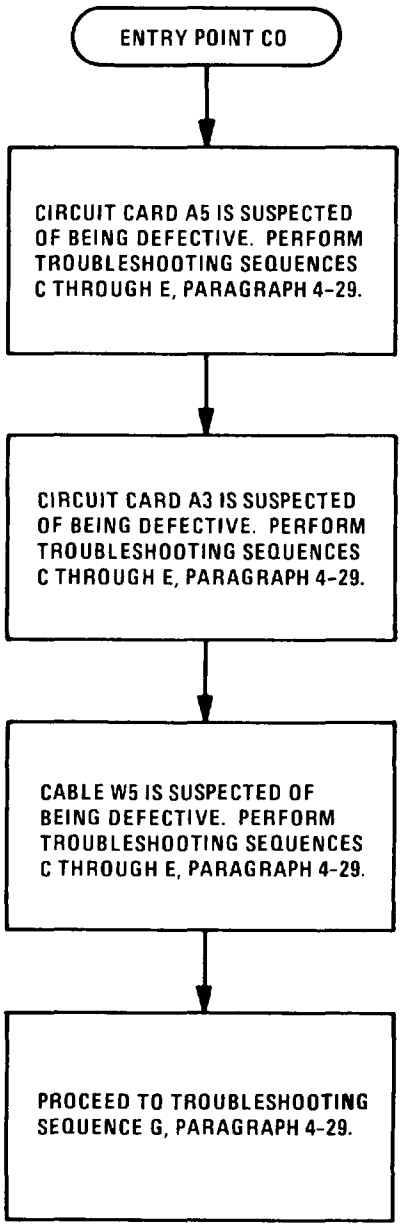
Troubleshooting Flow Chart - Entry Point CL



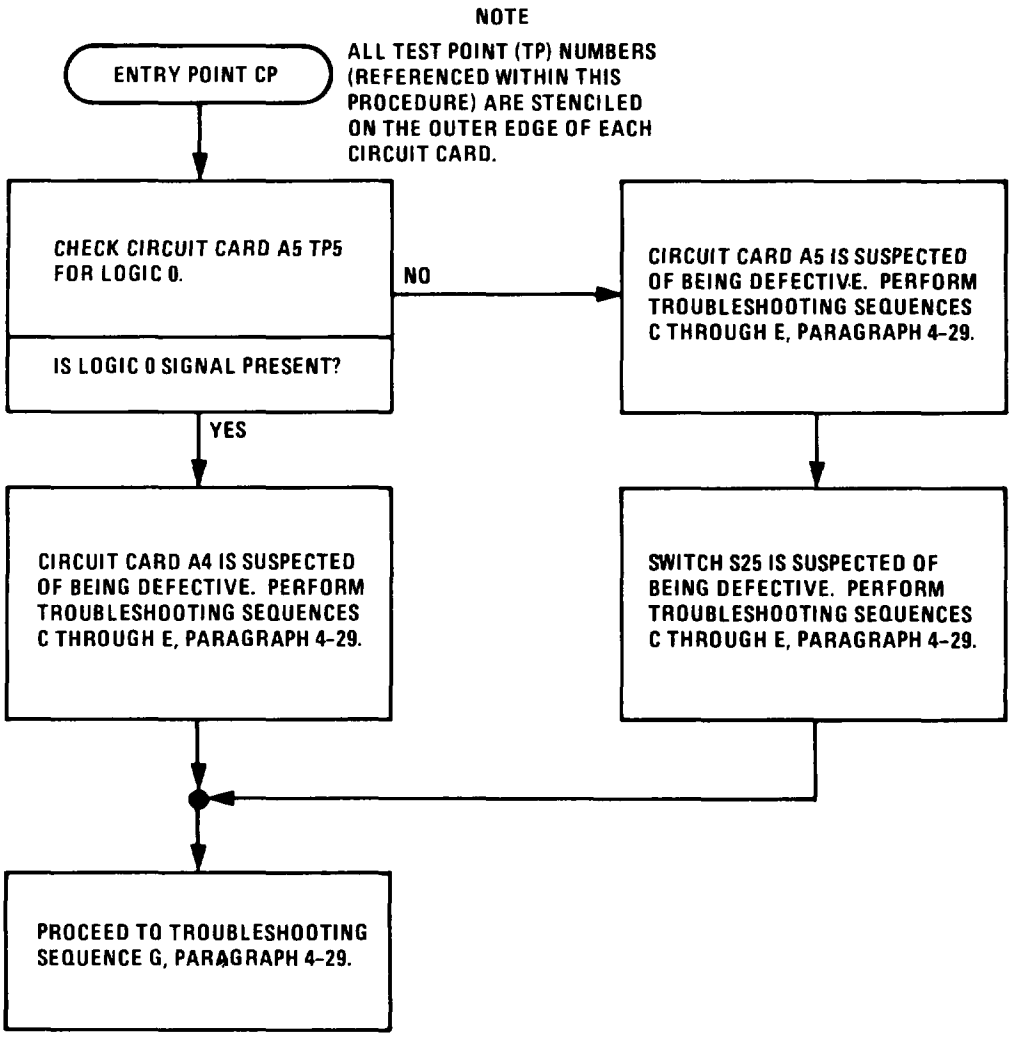
Troubleshooting Flow Chart - Entry Point CM



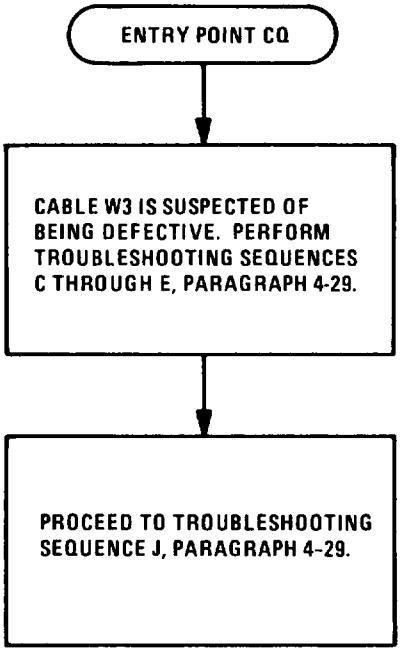
Troubleshooting Flow Chart - Entry Point CN



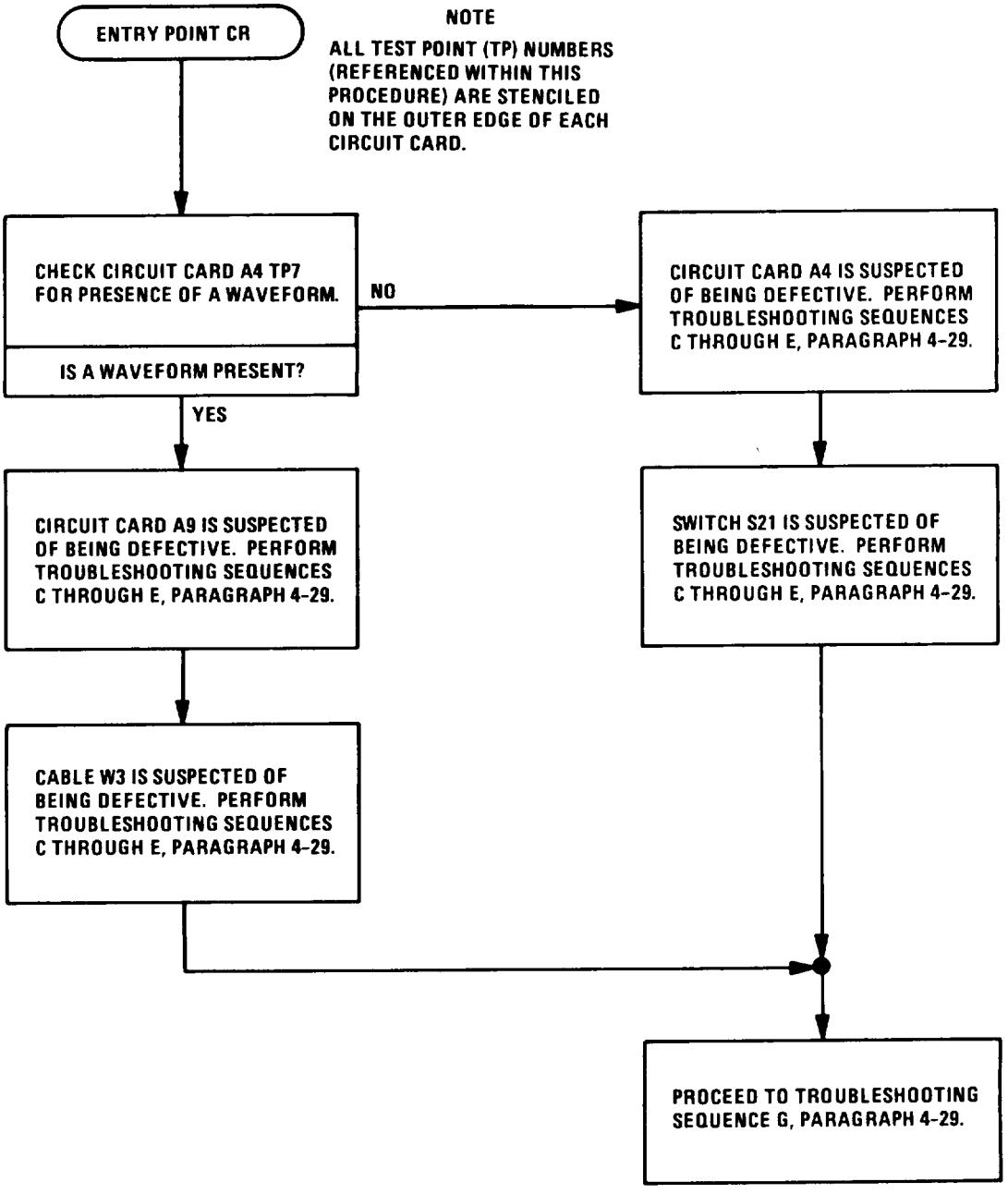
Troubleshooting Flow Chart - Entry Point CO



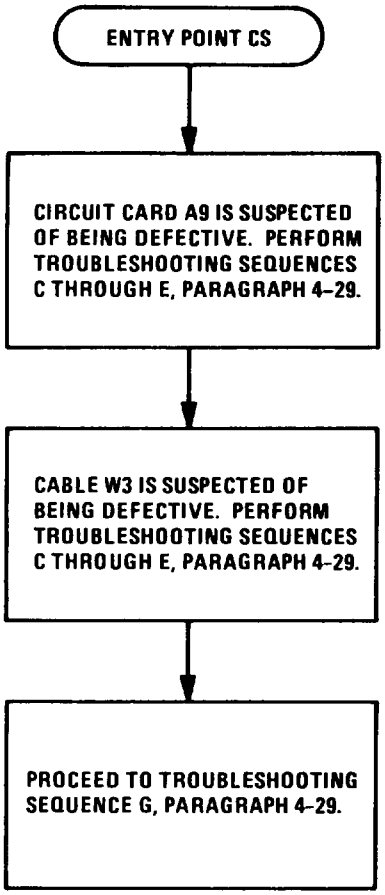
Troubleshooting Flow Chart - Entry Point CP



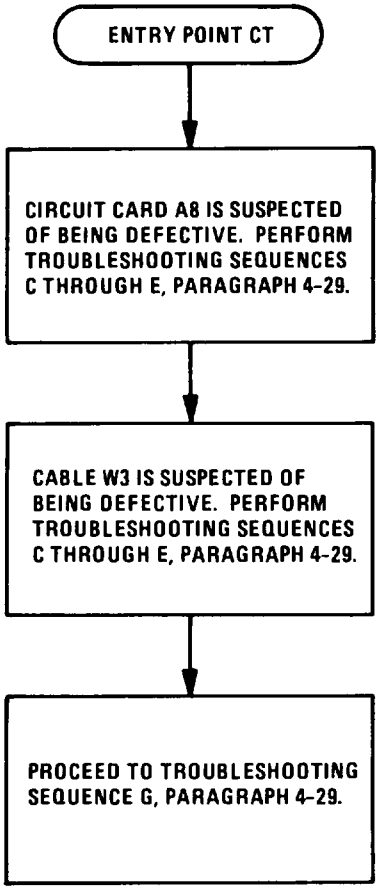
Troubleshooting Flow Chart - Entry Point CQ



Troubleshooting Flow Chart - Entry Point CR

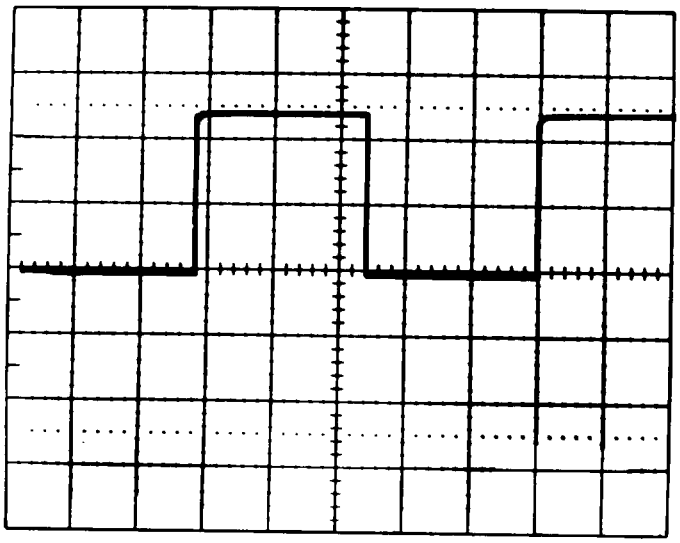


Troubleshooting Flow Chart - Entry Point CS



Troubleshooting Flow Chart - Entry Point CT

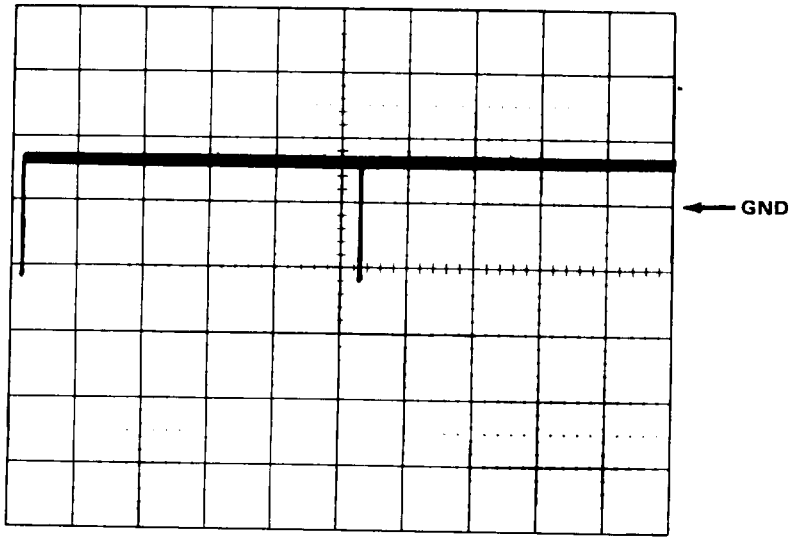
WAVEFORM A



OSCILLOSCOPE SETTINGS

VOLTS/DIV: 10
TIME/DIV: 0.1S
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

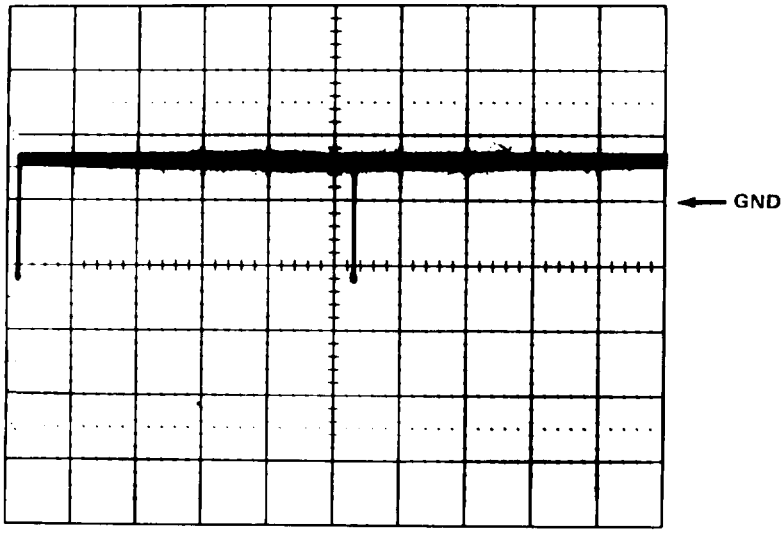
WAVEFORM B



OSCILLOSCOPE SETTINGS

VOLTS/DIV: 1
TIME/DIV: 0.1MS
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

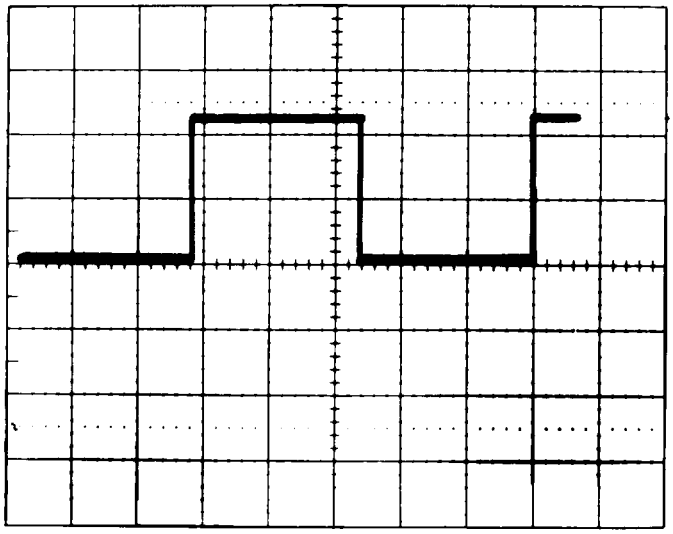
WAVEFORM C



OSCILLOSCOPE SETTINGS

VOLTS/DIV: 1
TIME/DIV: 0.1MS
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

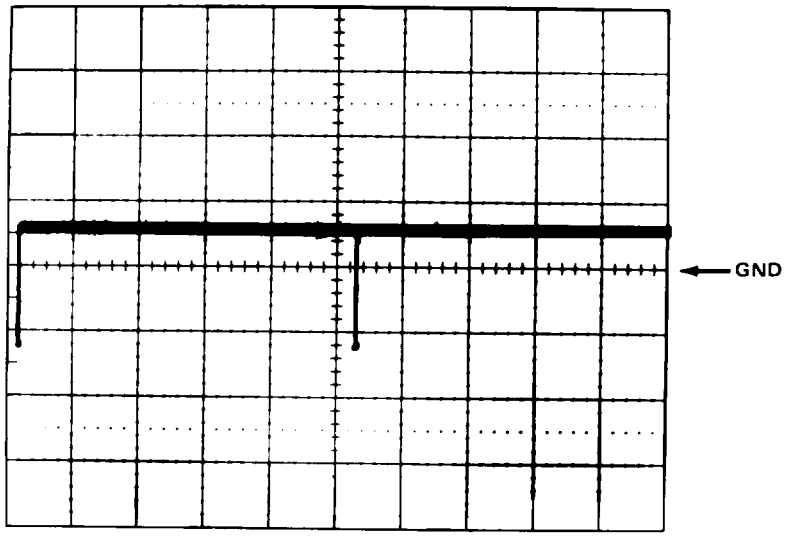
WAVEFORM D



OSCILLOSCOPE SETTINGS

VOLTS/DIV: 2
TIME/DIV: 0.1S
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

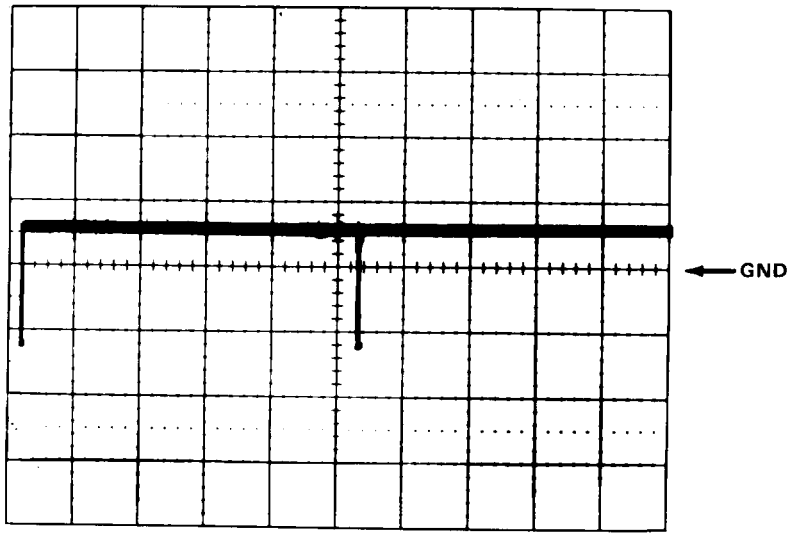
WAVEFORM E



OSCILLOSCOPE SETTINGS

VOLTS/DIV: 1
TIME/DIV: 0.1MS
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

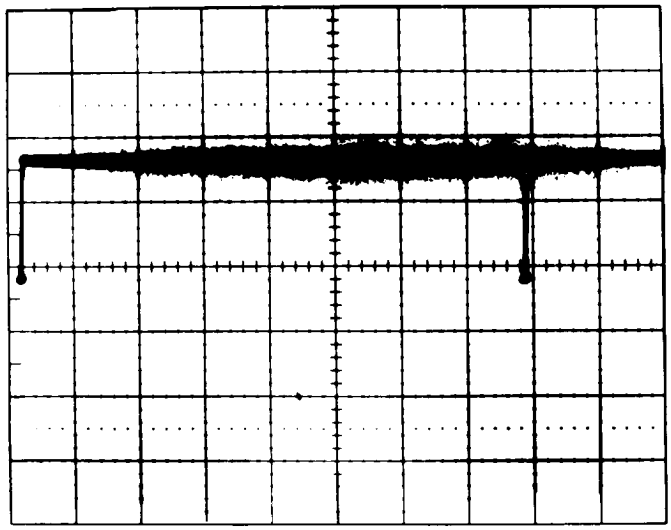
WAVEFORM F



OSCILLOSCOPE SETTINGS

VOLTS/DIV: 1
TIME/DIV: 0.1MS
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

WAVEFORM G



OSCILLOSCOPE SETTINGS

VOLTS/DIV: .2
TIME/DIV: 50 μS
SOURCE: CH 1
TRIGGER MODE: NORM
COUPLING: AC
SLOPE: –(MINUS)

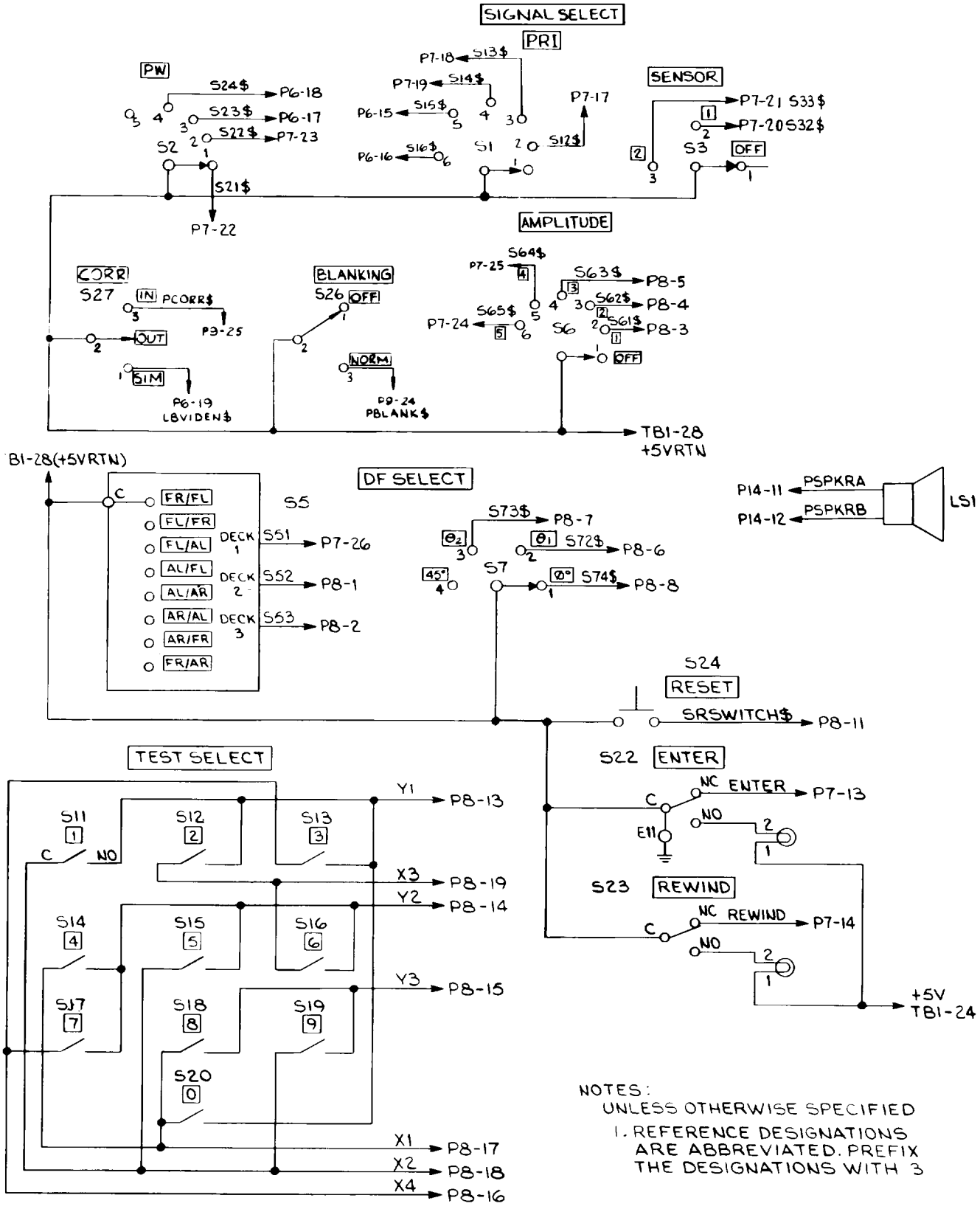
PTS ELECTRICAL SCHEMATIC DIAGRAM AND WIRING INFORMATION

4-32. The electrical schematic diagram and wiring information for the PTS is presented on the following pages.

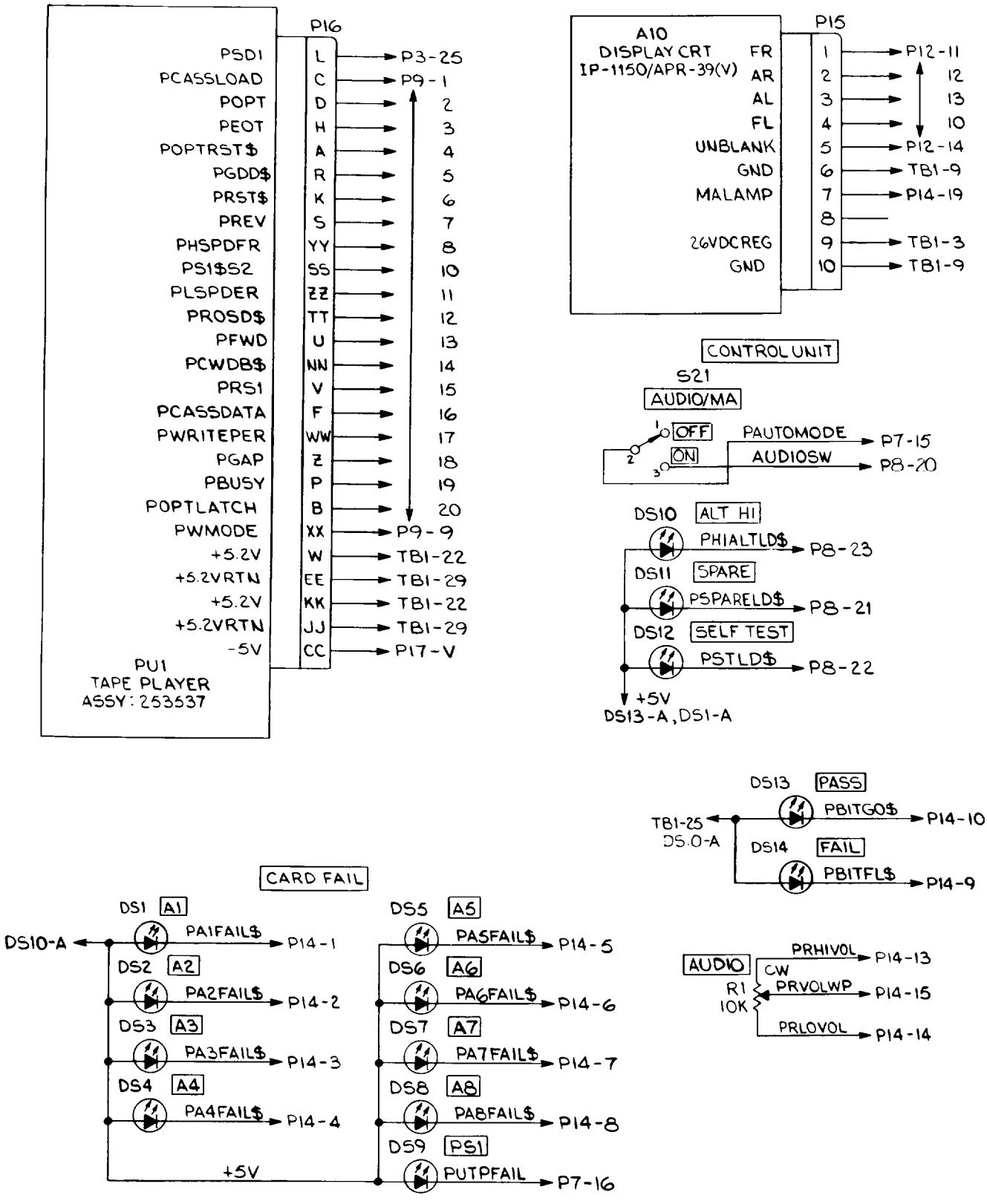
- The electrical schematic diagram for the PTS is provided to enable you to identify major assemblies of the PTS and the wiring between them. This diagram depicts all piece parts of the front panel and shows their electrical connections to the backplane assembly (A12) of the card cage. Use this diagram along with the PTS wiring information to perform continuity checks of the PTS wiring as called for in troubleshooting sequence J of paragraph 4-29.

- The PTS wiring information consists of a front panel (rear view) diagram, two wiring harness diagrams and wire run list of the choke assembly. This information is provided on the pages following the PTS electrical schematic diagram. The PTS front panel (rear view) diagram and associated jumper wire run list is provided to show you front panel piece part component layout and the jumper wiring between each of these components. A PTS front panel wiring harness diagram is provided to show you the point-to-point connection between each front panel component and the card cage connectors (P1 through P9 and P11, P12 and P14). A PTS power wiring harness diagram is also provided to show you the connections between the power supply connector (P18), the choke assembly and the RFI enclosure. In addition, a choke assembly wire run list is provided to show you the point-to-point connections of the choke assembly. Use these diagrams and wire run lists along with the PTS electrical schematic diagram to perform continuity checks of the PTS wiring as called for in troubleshooting sequence J of paragraph 4-29.

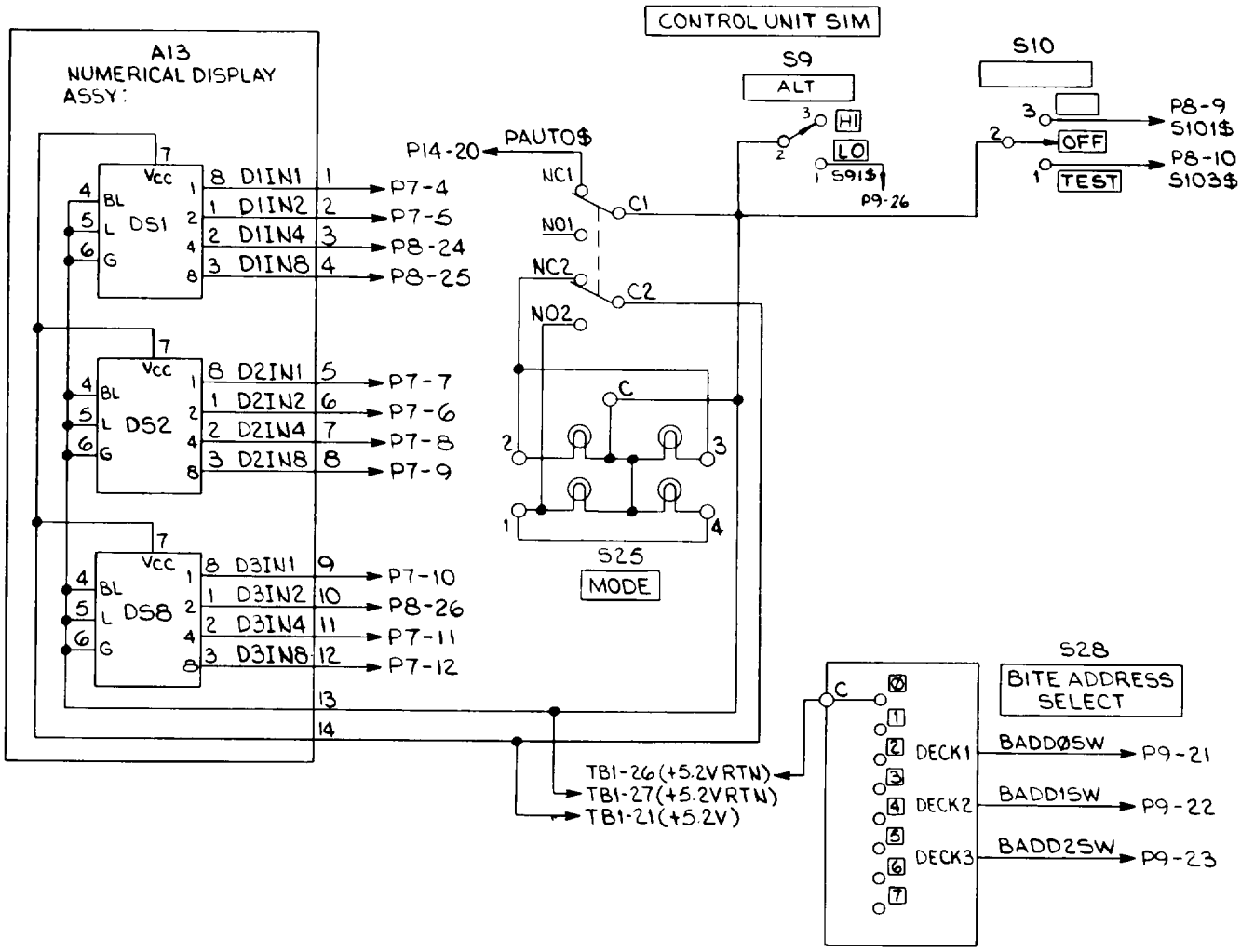
- Illustrations of test point (TP) layout for circuit cards A3 thru A5 and A7 thru A9 or pin number layout for numerical display A13, toggle switch S8 and pushbutton switch S30 are provided following the choke assembly wire run list. Use these illustrations to monitor the appropriate TP locations on these components, as called for in the troubleshooting flow charts of paragraph 4-31.



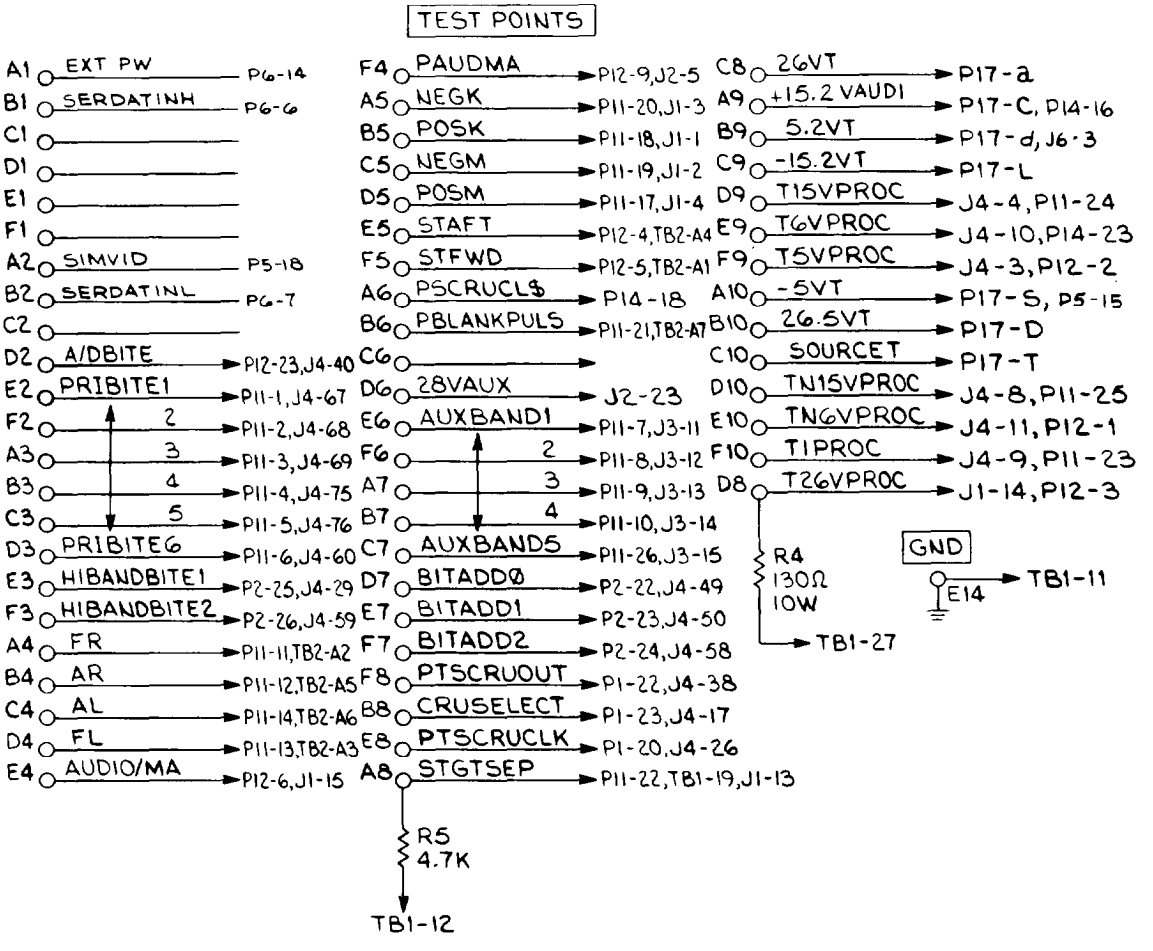
Processor Test Set Schematic Diagram (Sheet 1 of 15)



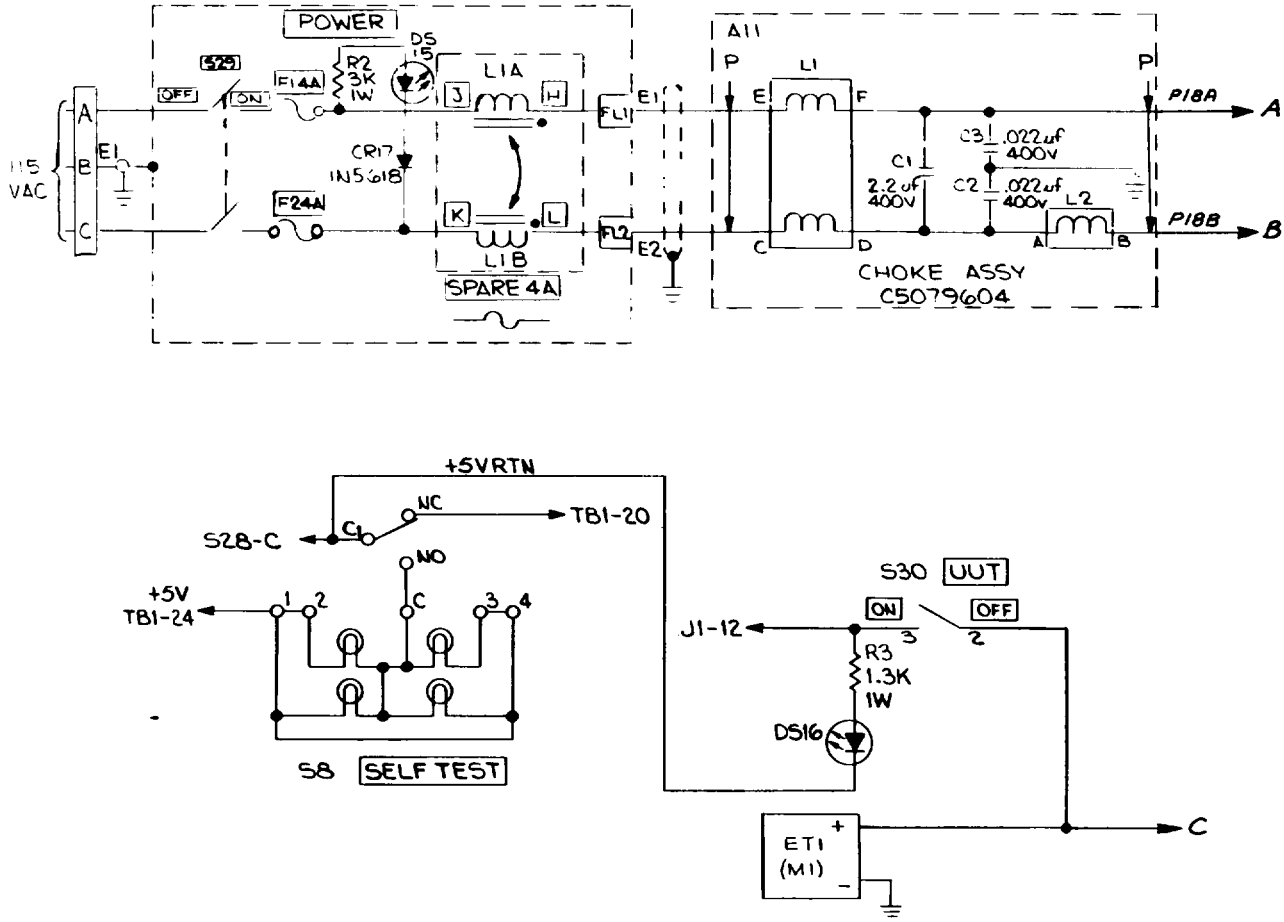
Processor Test Set Schematic Diagram (Sheet 2 of 15)



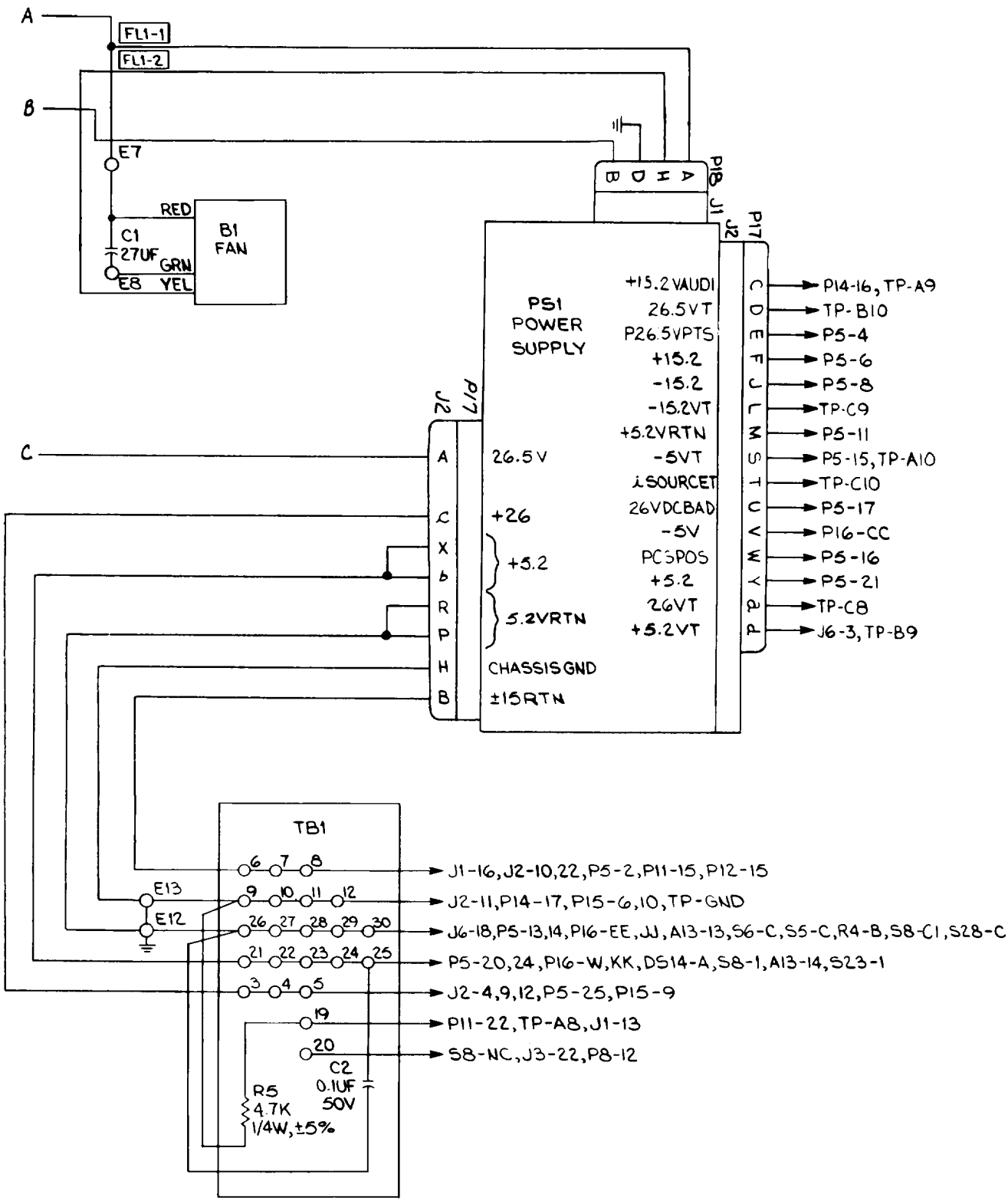
Processor Test Set Schematic Diagram (Sheet 3 of 15)



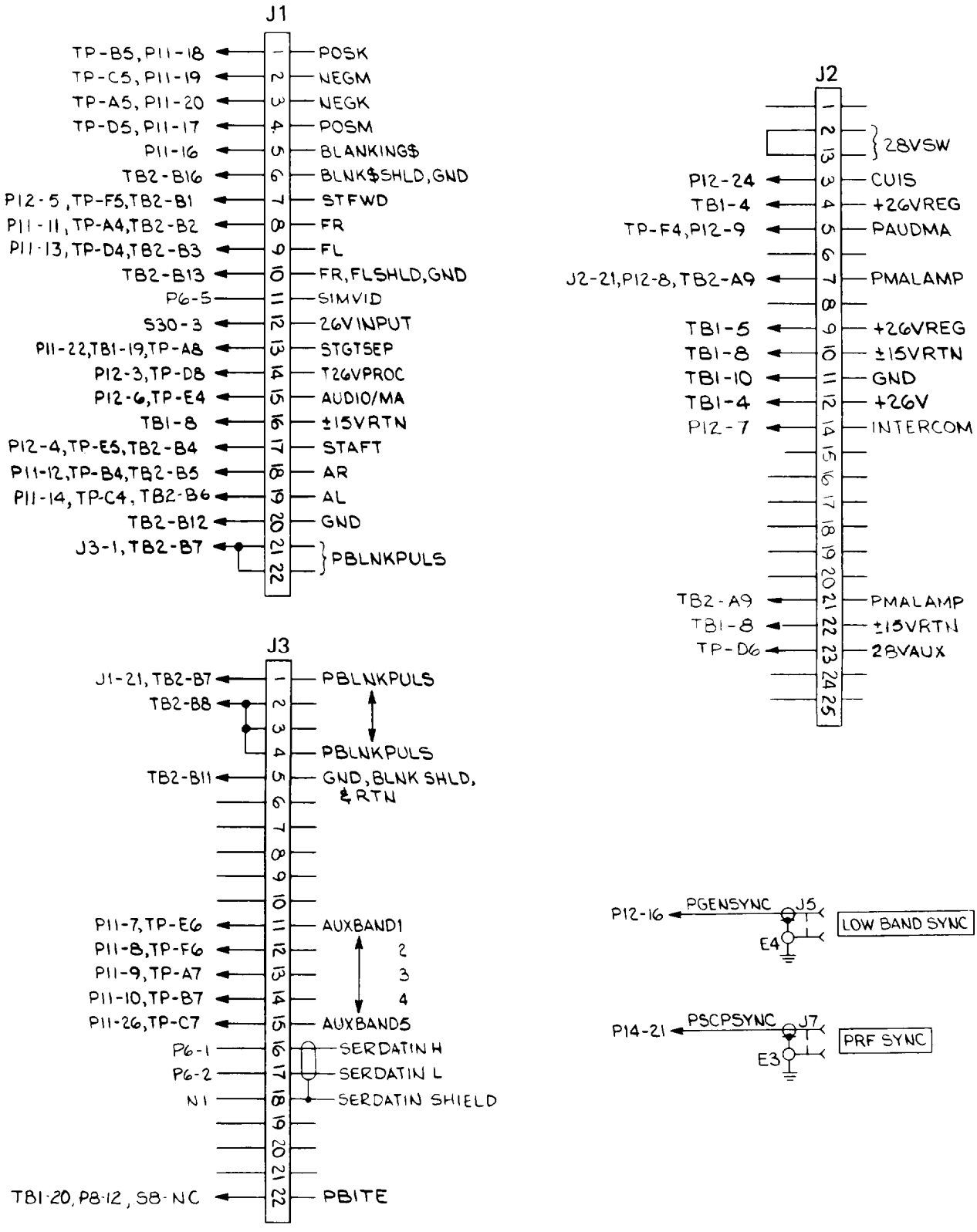
Processor Test Set Schematic Diagram (Sheet 4 of 15)



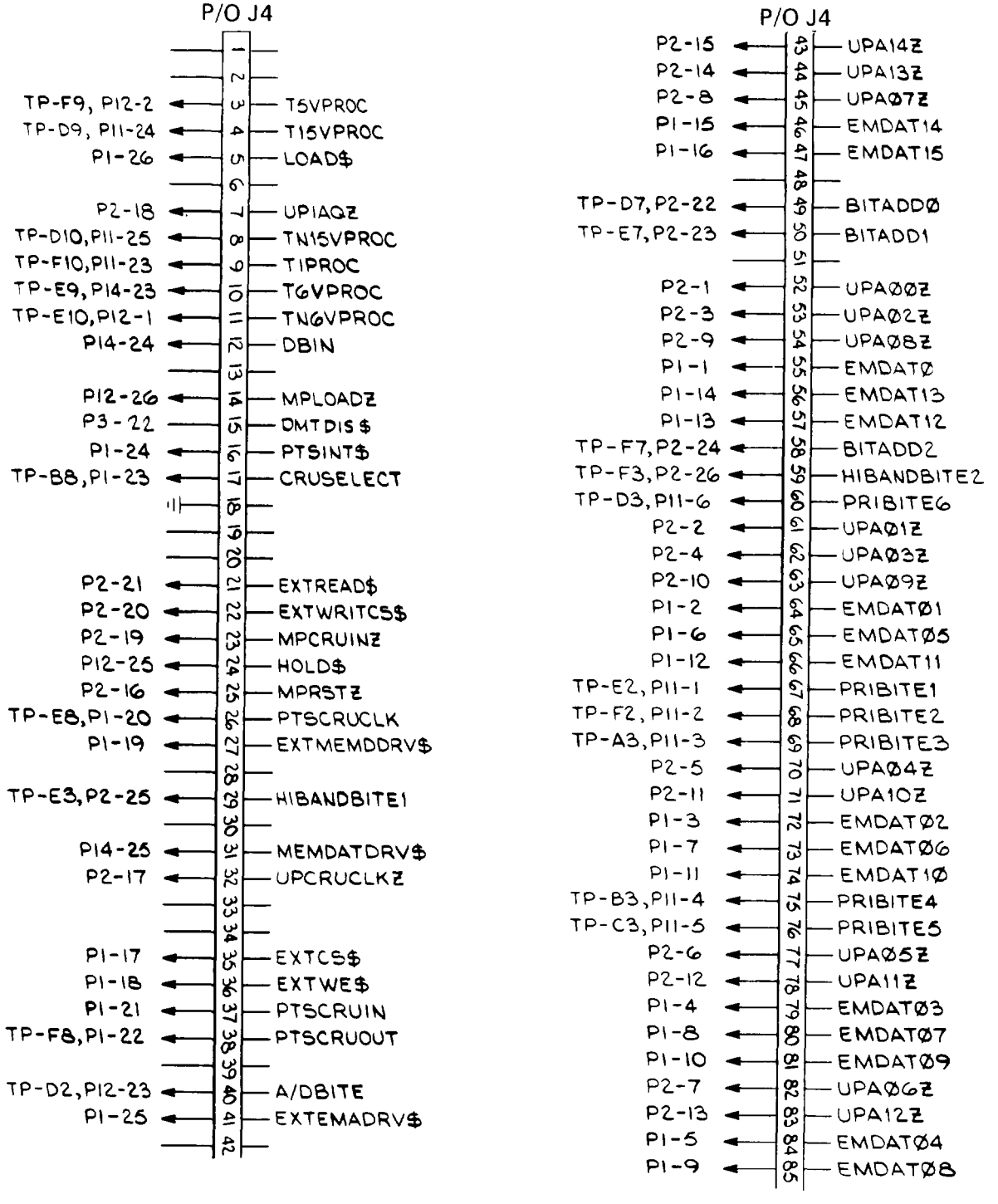
Processor Test Set Schematic Diagram (Sheet 5 of 15)



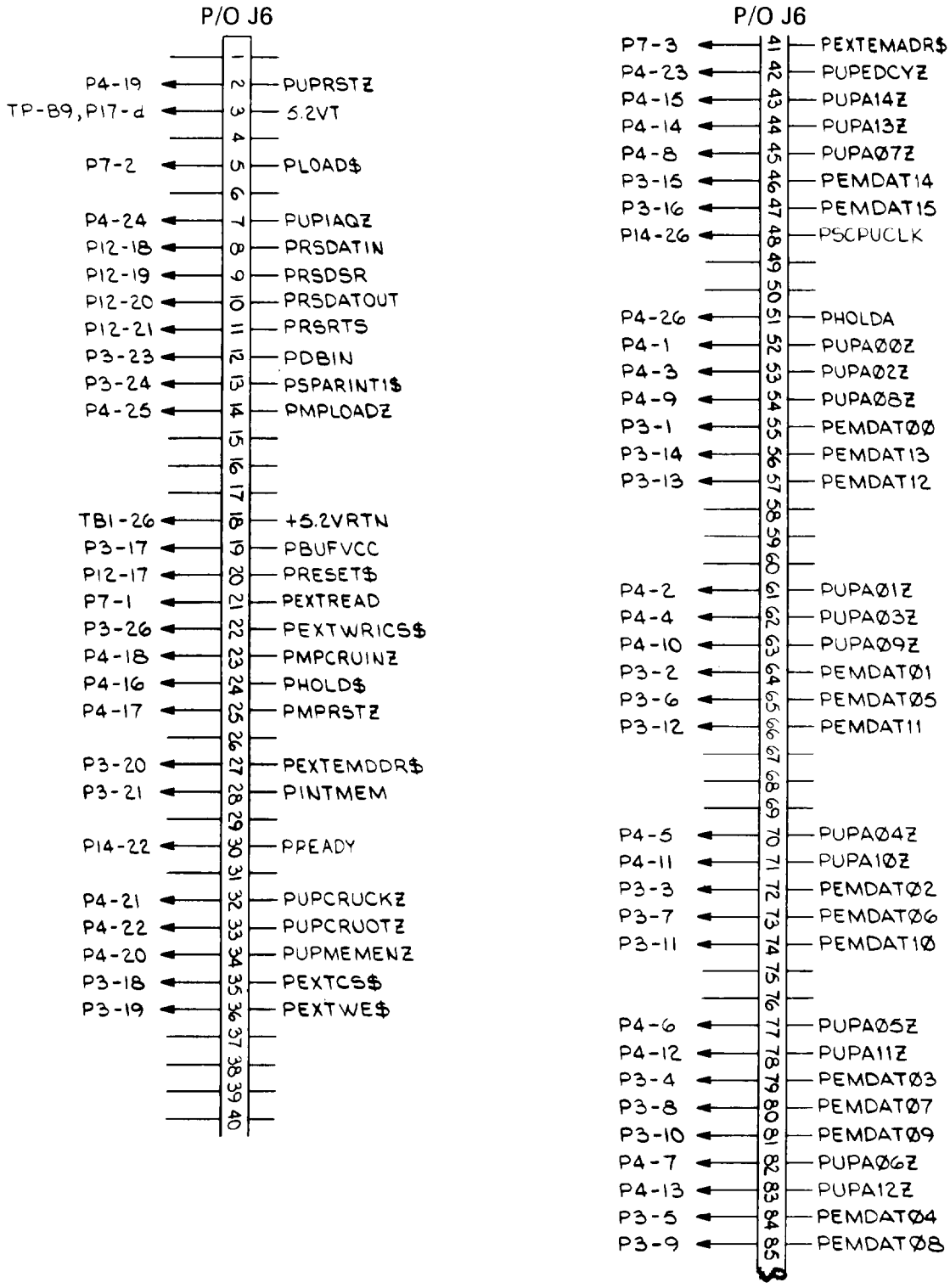
Processor Test Set Schematic Diagram (Sheet 6 of 15)



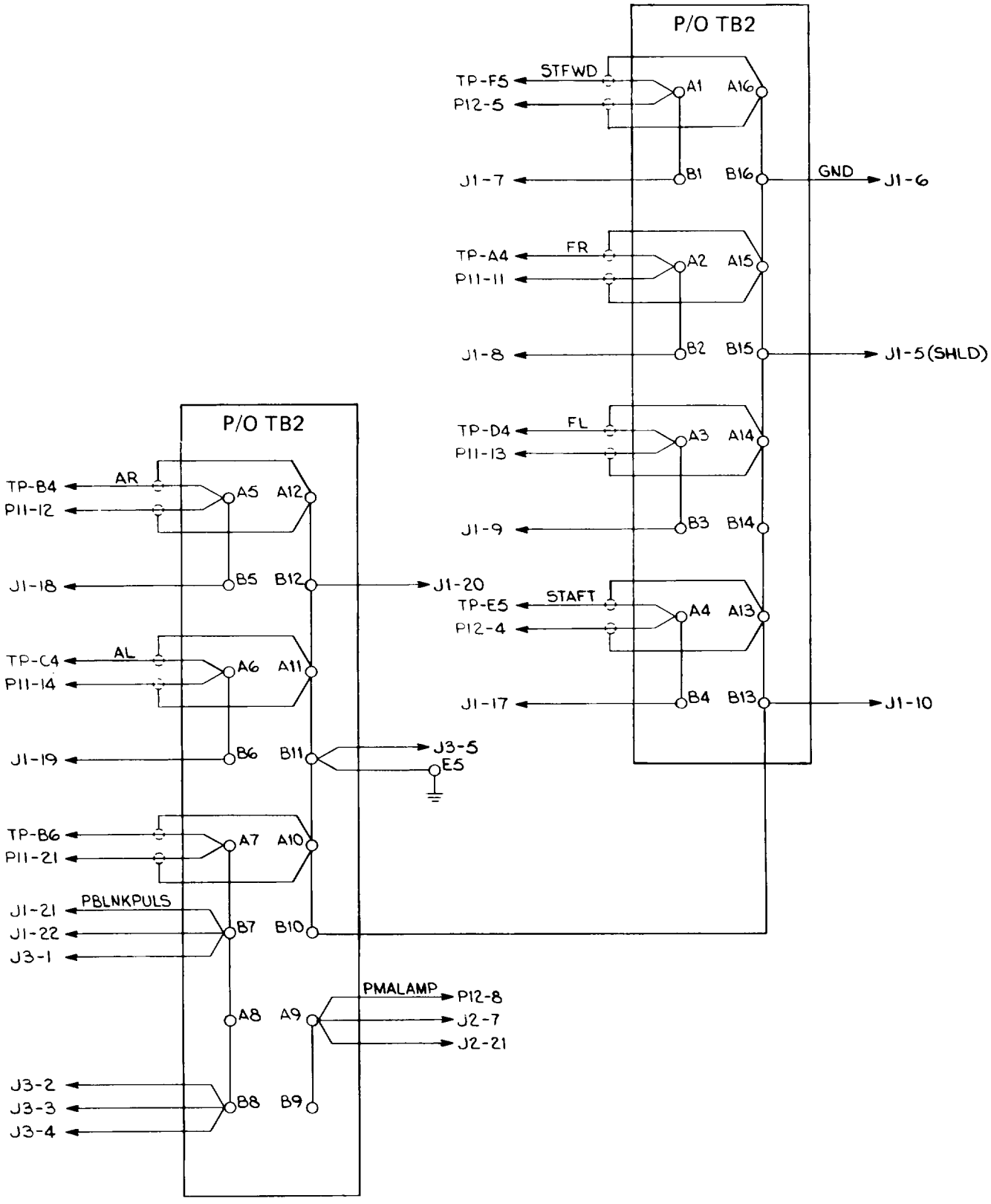
Processor Test Set Schematic Diagram (Sheet 7 of 15)



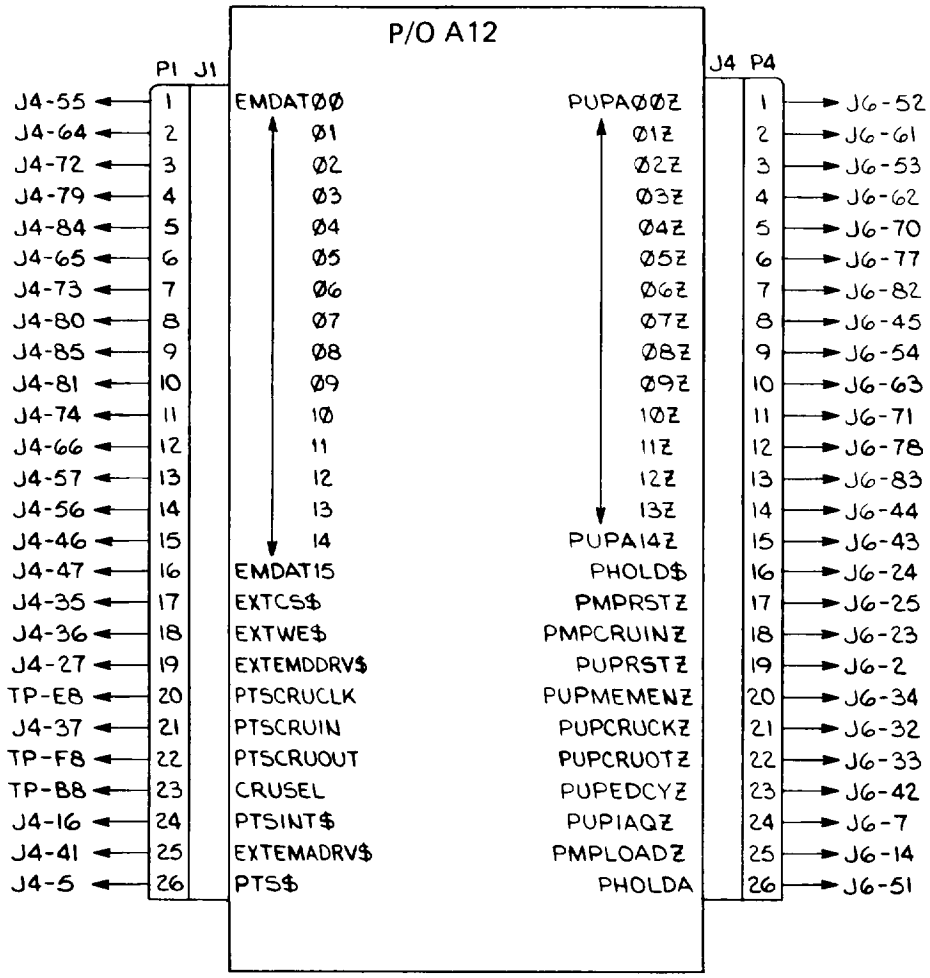
Processor Test Set Schematic Diagram (Sheet 8 of 15)



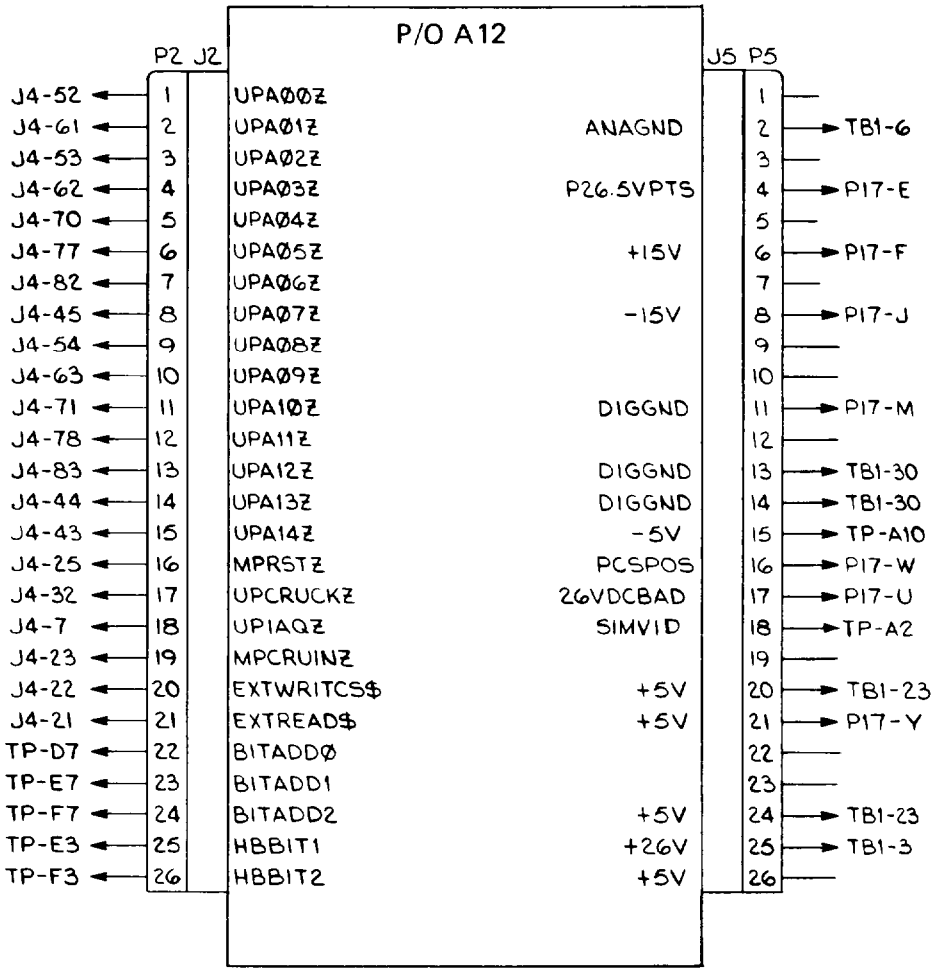
Processor Test Set Schematic Diagram (Sheet 9 of 15)



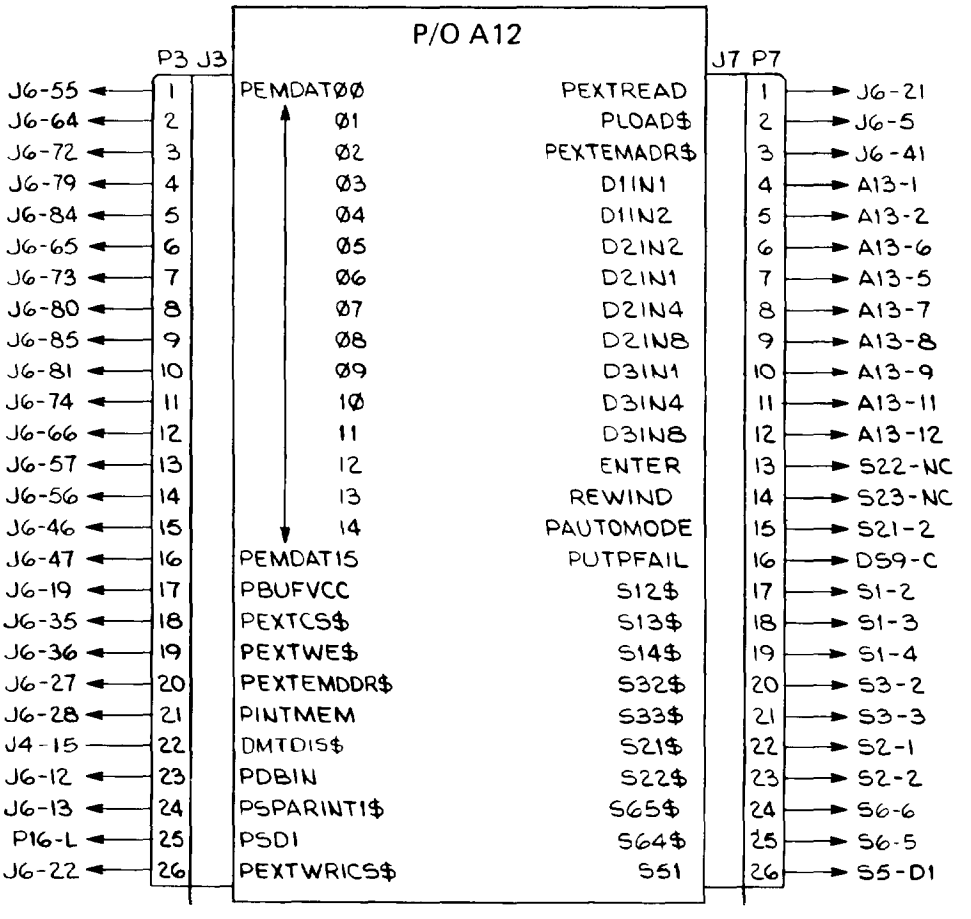
Processor Test Set Schematic Diagram (Sheet 10 of 15)



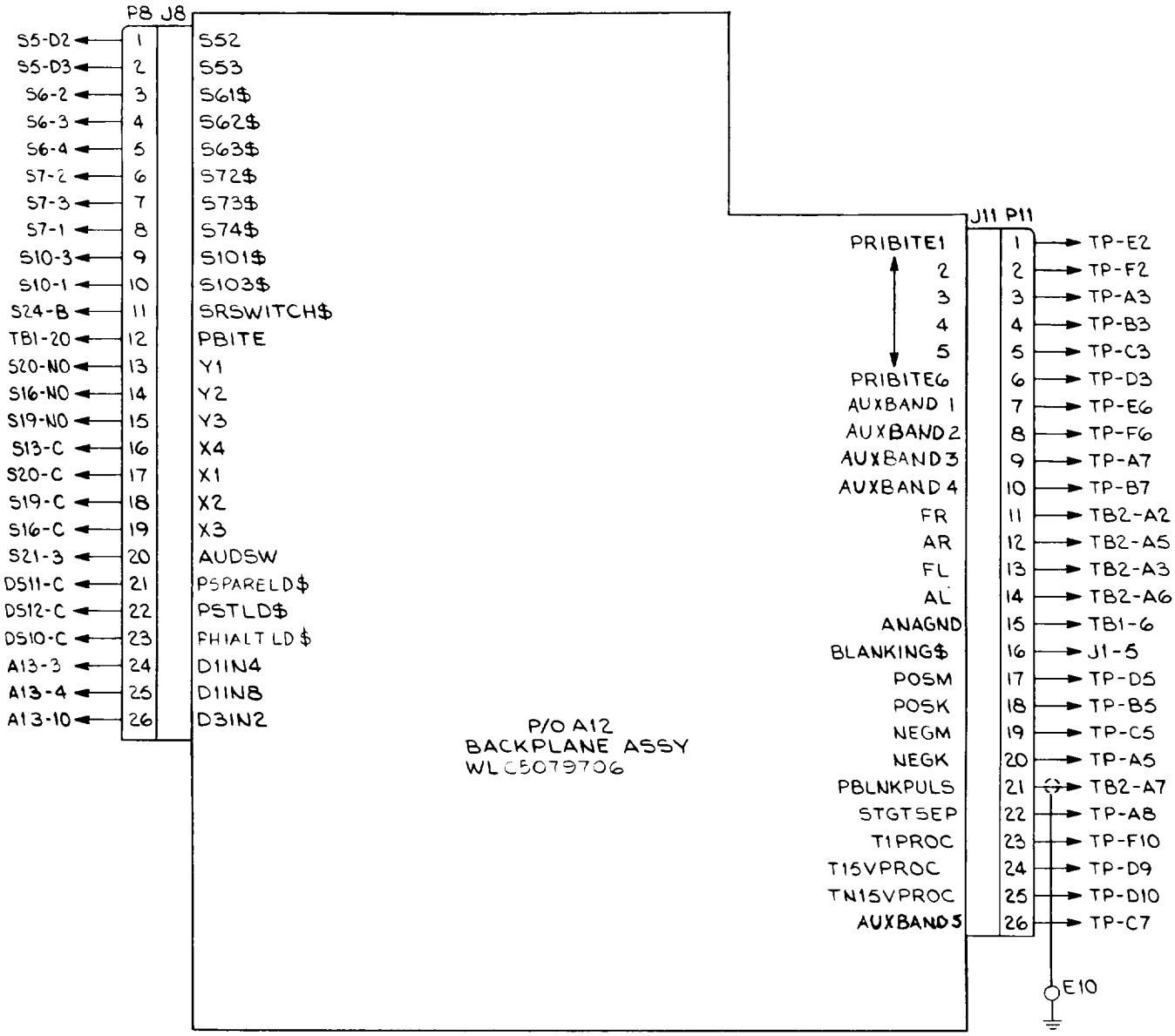
Processor TestSet Schematic Diagram (Sheet 11of15)



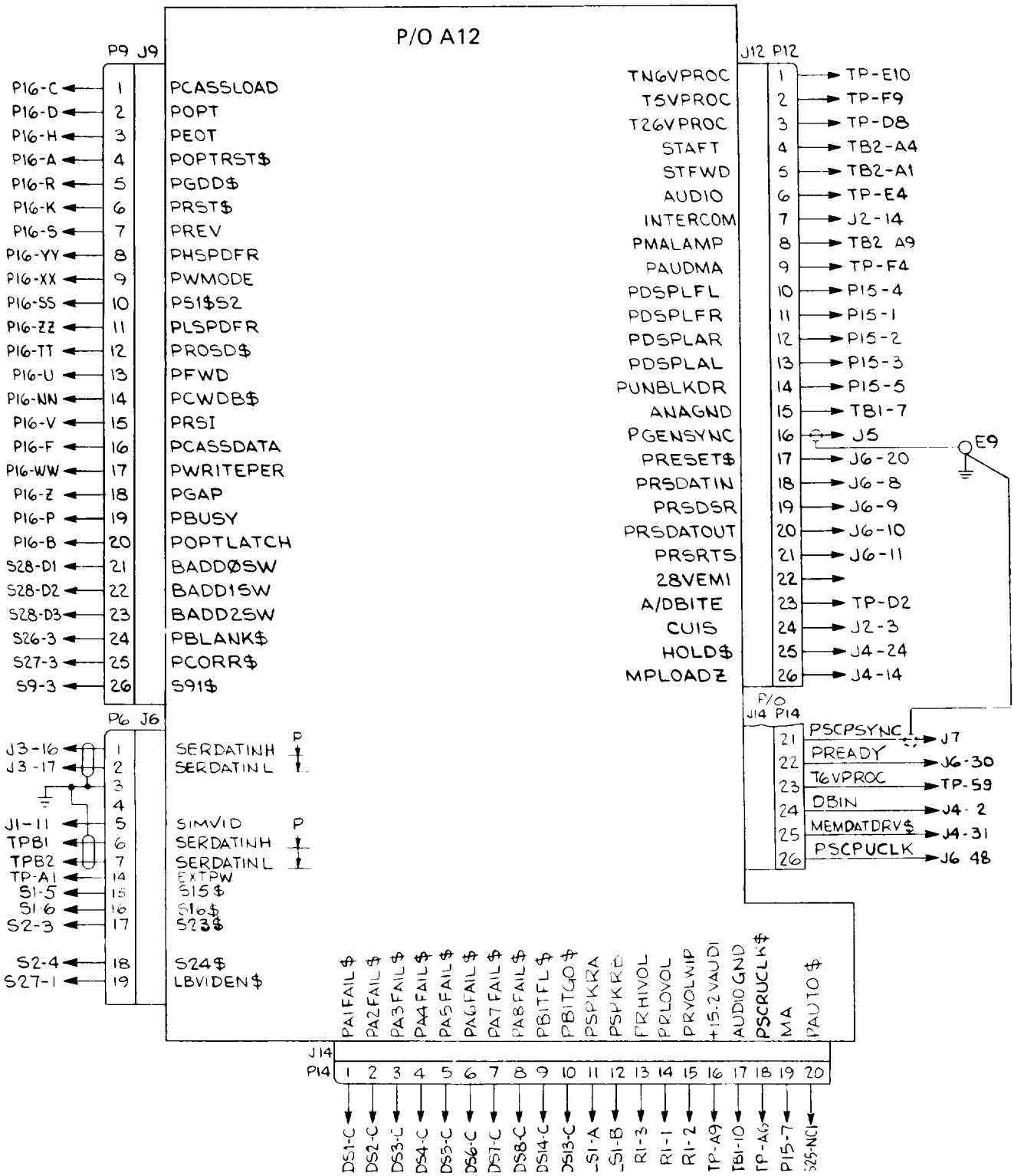
Processor Test Set Schematic Diagram (Sheet 12 of 15)



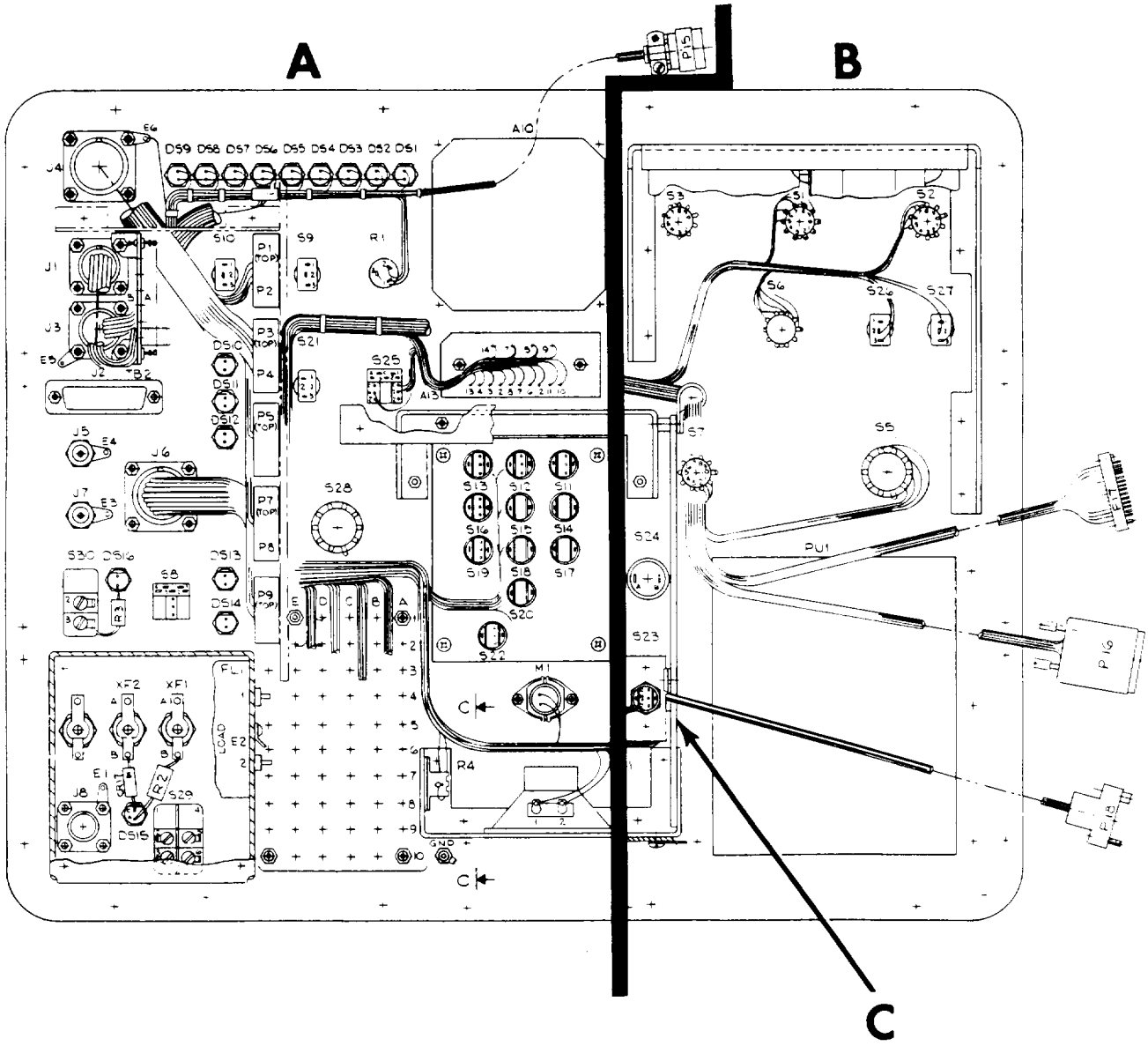
Processor Test Set Schematic Diagram (Sheet 13 of 15)



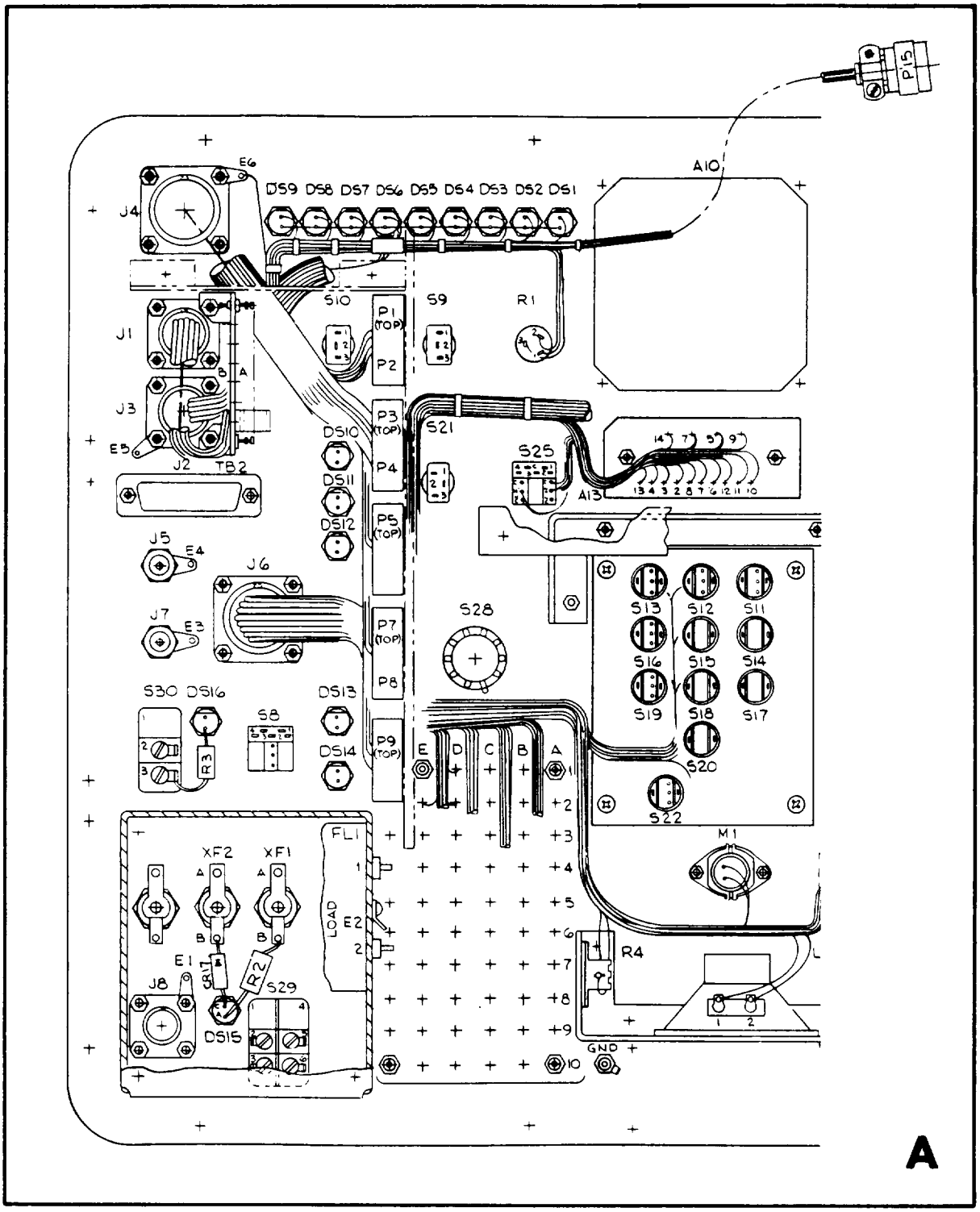
Processor Test Set Schematic Diagram (Sheet 14 of 15)



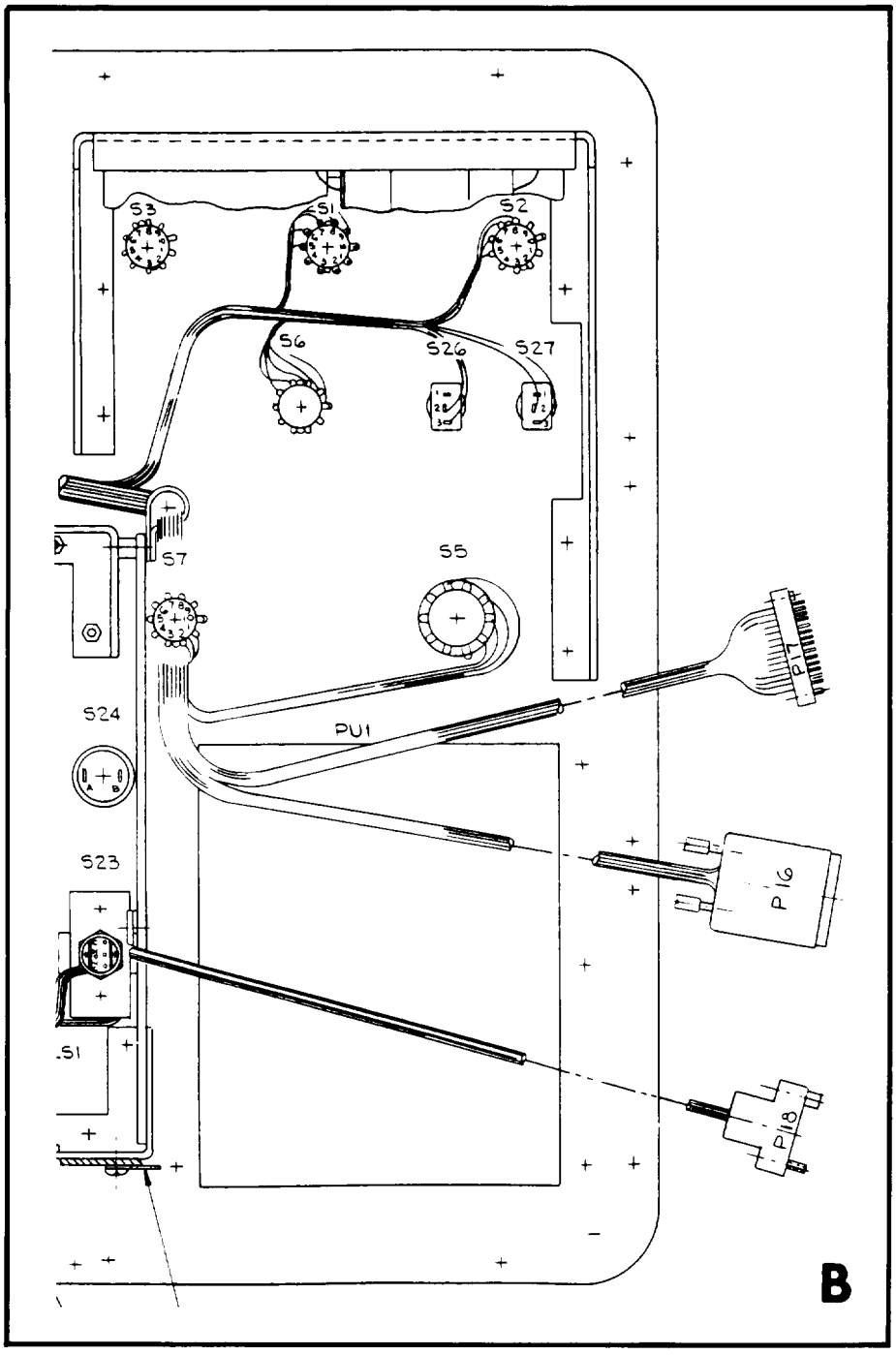
Processor Test Set Schematic Diagram (Sheet 15 of 15)

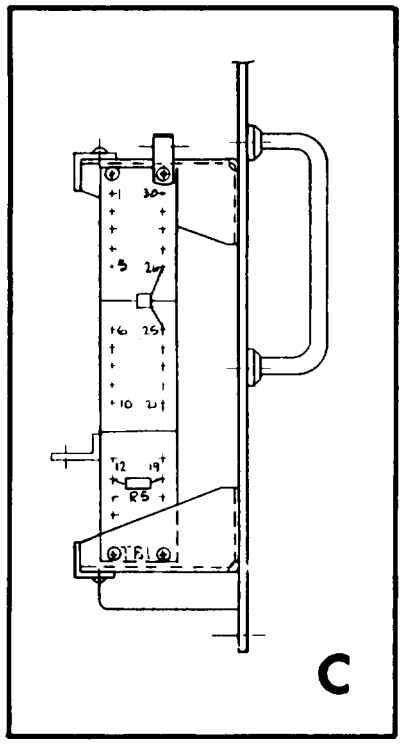


PTS Front Panel (Rear View) Diagram (Sheet 1 of 4)



PTS Front Panel (Rear View) Diagram (Sheet 2 of 4)

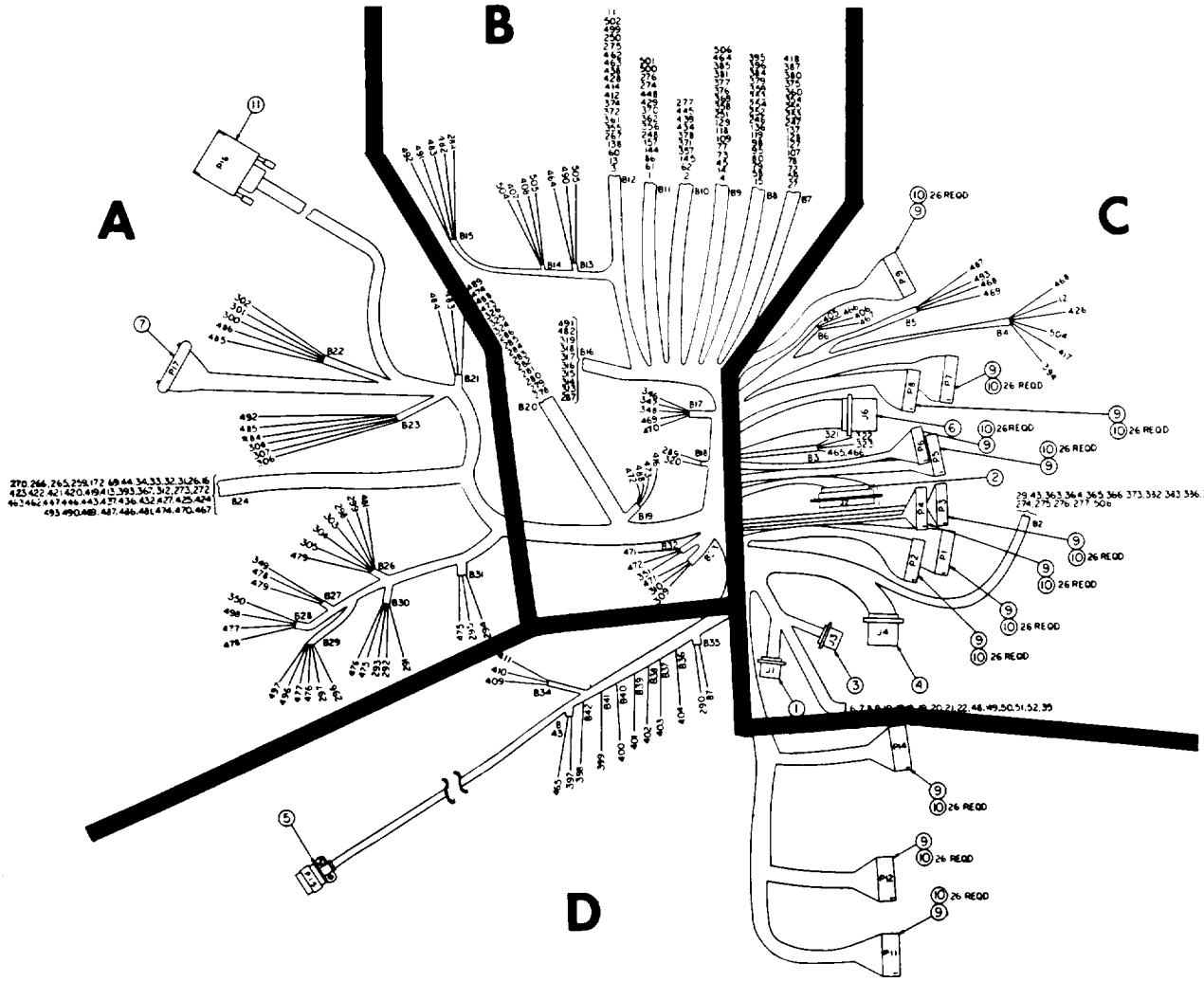




PTS Front Panel (Rear View) Diagram (Sheet 3 of 4)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
1	98	.60	DS1-A	N	DS2-A	N	BARE
2	98	.60	DS2-A	N	DS3-A	N	BARE
3	98	.60	DS3-A	N	DS4-A	N	BARE
4	98	.60	DS4-A	N	DS5-A	N	BARE
5	98	.60	DS5-A	N	DS6-A	N	BARE
6	98	.60	DS6-A	N	DS7-A	N	BARE
7	98	.60	DS7-A	N	DS8-A	N	BARE
8	98	.60	DS8-A	N	DS9-A	N	BARE
9	98	.40	S25-C1	N	S25-C	N	BARE
10	98	.25	S8-C	N	S8-NO	N	BARE
11	98	.40	S8-4	N	S8-5	N	BARE
12	98	.50	S8-3	N	S8-2	N	BARE
13	98	.30	S8-2	N	S8-1	N	BARE
14	98	.50	S25-3	N	S25-2	N	BARE
15	99	.80	S25-2	.19	S25-NC-2	.19	WHT
16	99	.70	S25-4	.19	S25-1	.19	WHT
17	99	.45	S25-1	.19	S25-NO2	.19	WHT
18	99	.35	S22-NO	N	S22-2	N	WHT
19	99	.35	S23-NO	N	S23-2	N	WHT
20	97	1.9	J8-A	.19	S29-OFF	.19	WHT
21	96	1.0	J8-B	.19	GND-E1	.19	BLK
22	95	2.2	J8-C	.19	S29-OFF	.19	WHT/BLK
23	98	.25	TB1-4	N	TB1-5	N	BARE
24	98	.25	TB1-6	N	TB1-7	N	BARE
25	98	.25	TB1-7	N	TB1-8	N	BARE
26	98	.25	TB1-9	N	TB1-10	N	BARE
27	98	.25	TB1-10	N	TB1-11	N	BARE
28	98	.50	TB1-11	N	TB1-12	N	BARE
29	98	.25	TB1-26	N	TB1-27	N	BARE
30	98	.25	TB1-27	N	TB1-28	N	BARE
31	98	.25	TB1-28	N	TB1-29	N	BARE
32	98	.25	TB1-29	N	TB1-30	N	BARE
33	95	2.9	S29-ON	.19	XF1-A	.19	WHT/BLK
34	99	3.1	S29 ON	.19	XF2-A	.19	WHT
35	95	2.7	XF1-B	.19	L1A-J	.19	WHT/BLK
36	99	3.0	XF2-B	.19	L1A-K	.19	WHT
37	99	.9	DS10-A	.19	DS11-A	.19	WHT
38	99	3.6	DS11-A	.19	DS12-A	.19	WHT
39	99	.9	DS13-A	.19	DS14-A	.19	WHT
40	98	1.0	TB1-21	N	TB1-22	N	BARE
41	98	1.0	TB1-22	N	TB1-23	N	BARE
42	98	1.0	TB1-23	N	TB1-24	N	BARE
43	98	1.0	TB1-24	N	TB1-25	N	BARE
44	98	2.0	S11-NO	N	S12-NO	N	BARE
45	98	2.0	S12-NO	N	S13-NO	N	BARE
46	99	3.0	S13-NO	.19	S20-NO	.19	WHT
47	99	2.0	S17-NO	.19	S14-NO	.19	WHT
48	99	2.0	S14-NO	.19	S15-NO	.19	WHT
49	99	3.0	S15-NO	.19	S16-NO	.19	WHT
50	99	2.0	S18-NO	.19	S19-NO	.19	WHT
51	99	2.0	S11-C	.19	S15-C	.19	WHT
52	99	2.0	S15-C	.19	S19-C	.19	WHT
53	99	2.0	S14-C	.19	S18-C	.19	WHT
54	99	1.0	S18-C	.19	S20-C	.19	WHT
55	99	2.0	S12-C	.19	S16-C	.19	WHT
56	99	3.0	S13-C	.19	S17-C	.19	WHT
57	96	5.0	S22-C	.19	E11-GND	.19	BLK
58	96	4.0	TB2-B11	.19	E5-GND	.19	BLK

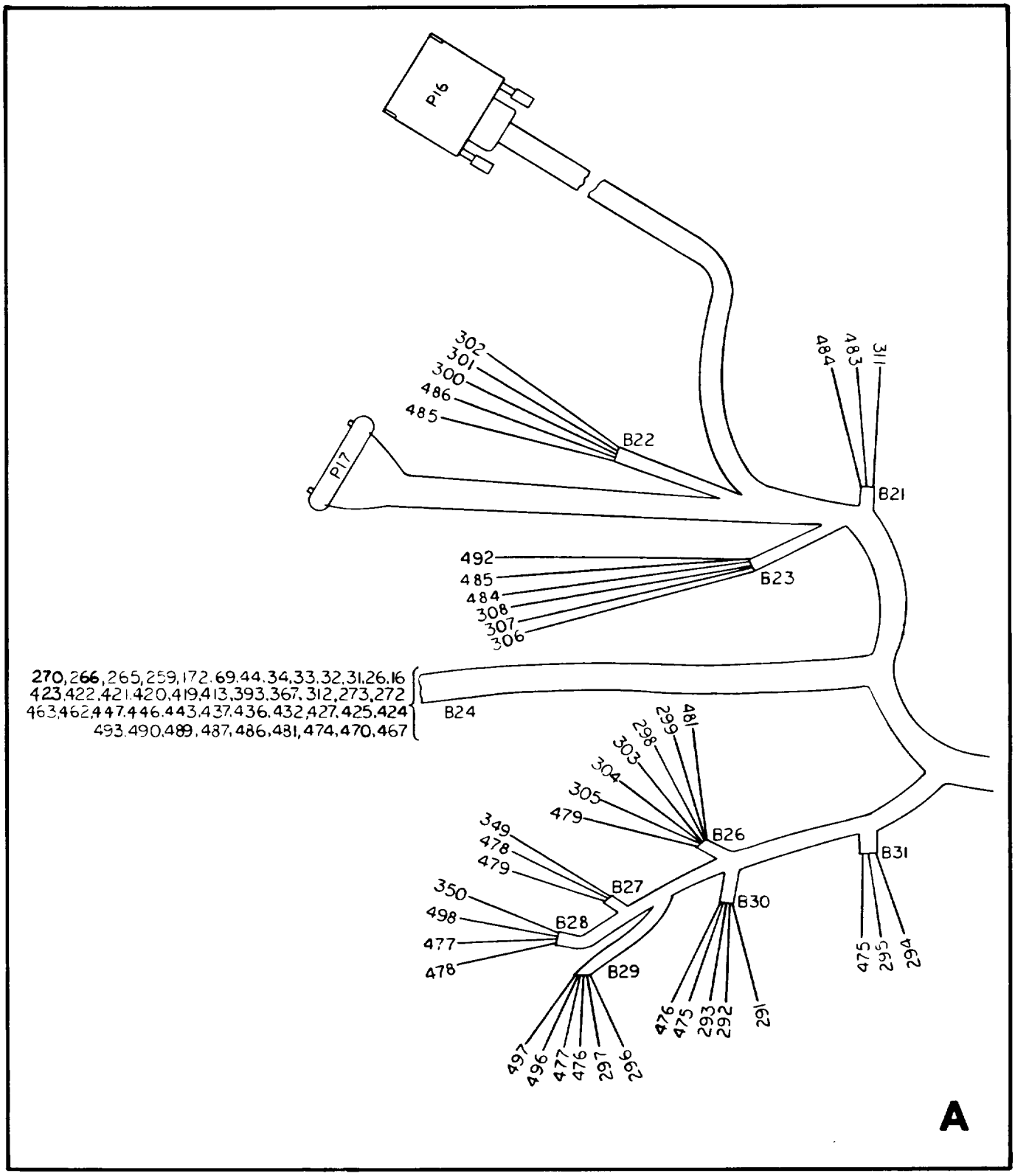
PTS Front Panel (Rear View) Diagram (Sheet 4 of 4)



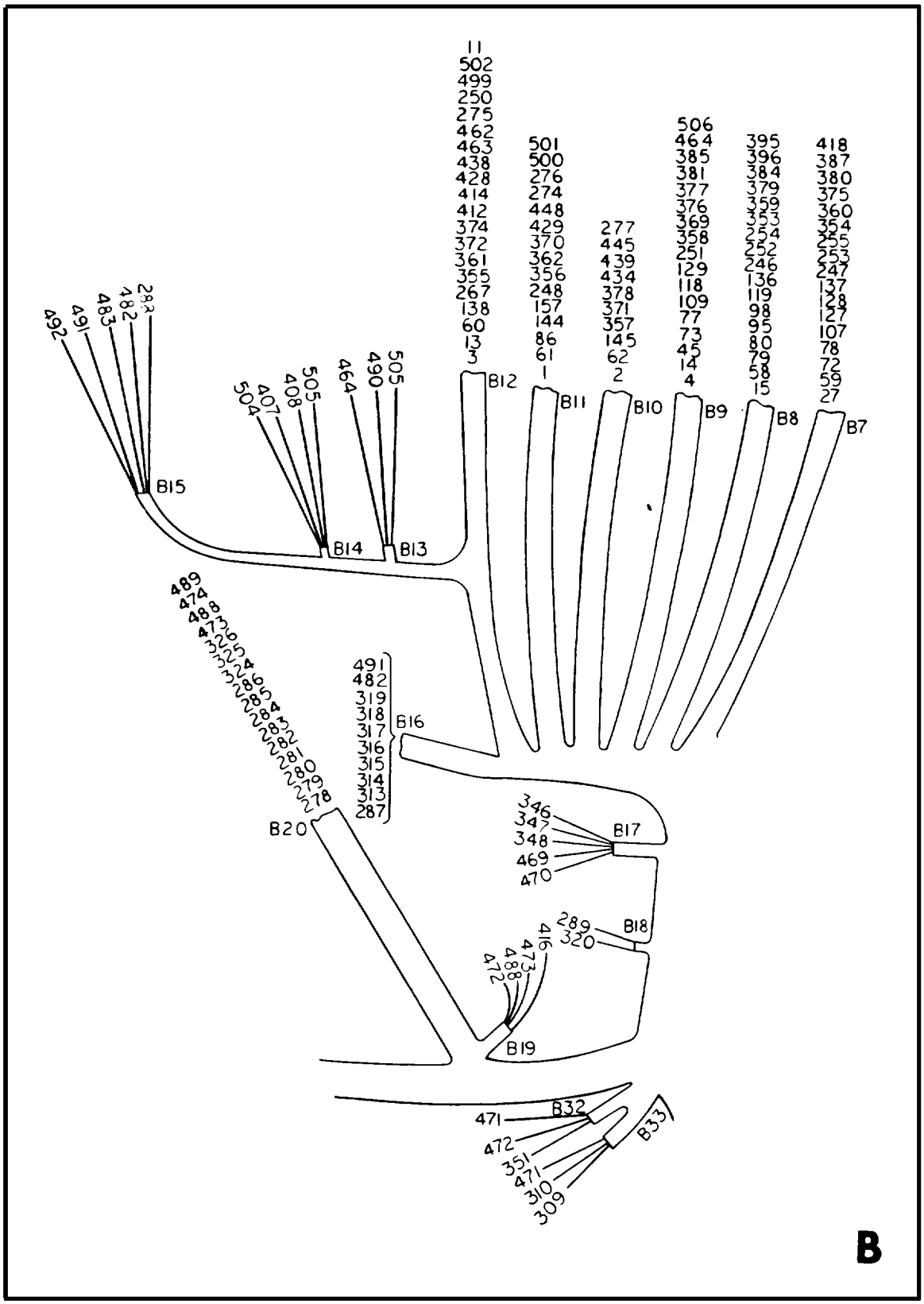
NOTES:

1. MARK REFERENCE DESIGNATION AND PIN NO.1 ON CONNECTORS P1 THRU P9, P11,P12 AND P14 IN .12 HIGH CHARACTERS USING WHITE MARKING INK FIND NO. 35.
2. MARK REFERENCE DESIGNATION ON CONNECTORS P15,P16 AND P17 IN .12 HIGH CHARACTERS USING BLACK MARKING INK FIND NO. 32.
3. NUMBERS ON CONNECTORS J1,J2,J3 J4 AND J6 ARE FOR REF. ONLY.
4. SOLDER IN ACCORDANCE WITH MIL-STD-454 REQUIREMENT 5 USING QQ-S-571 FIND NO. 33.
5. HARNESS SHALL BE LACED WITH FIND NO. 34.
6. WORKMANSHIP SHALL COMPLY WITH REQUIREMENT 9 OF MIL-STD-454.

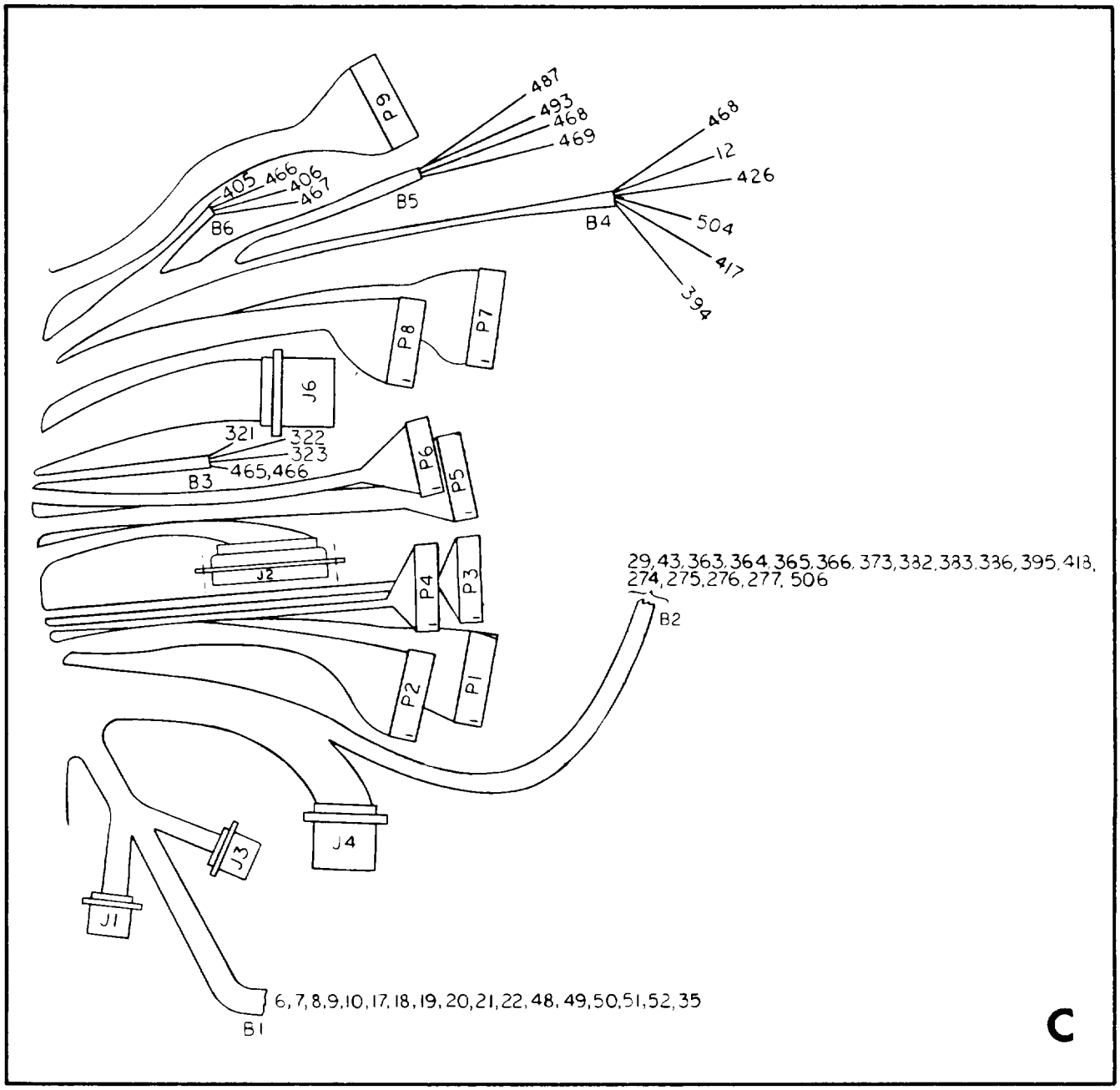
PTS Front Panel Wiring Diagram (Sheet 1 of 17)



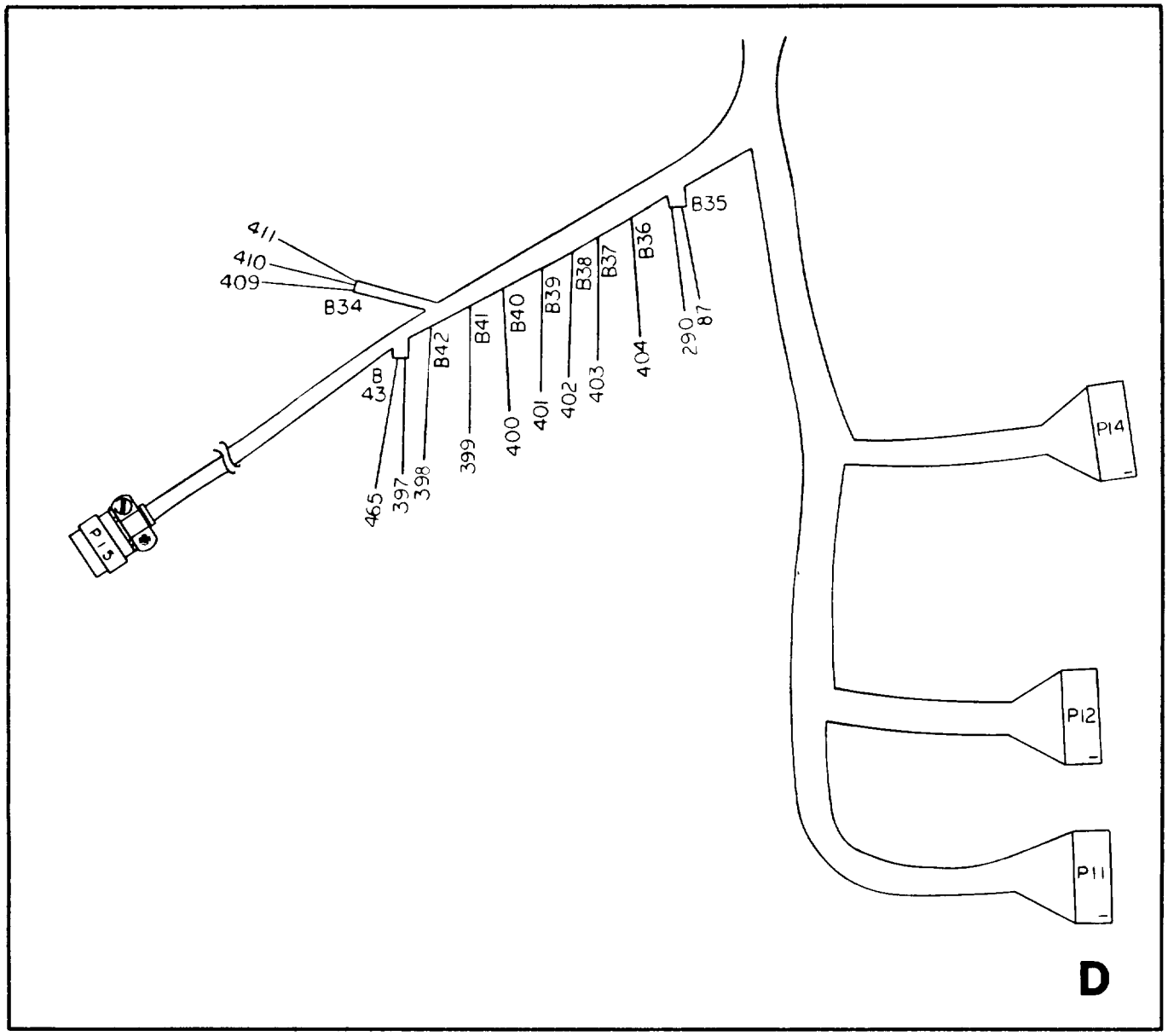
PTS Front Panel Wiring Diagram (Sheet 2 of 17)



PTS Front Panel Wiring Diagram (Sheet 3 of 17)



PTS Front Panel Wiring Diagram (Sheet 4 of 17)



PTS Front Panel Wiring Diagram (Sheet 5 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
1	14	18.00	J1-1	.19	B11(TP-B5)	N	WHT
2		18.00	J1-2	.19	B10(TP-C5)	N	WHT
3		19.00	J1-3	.19	B12(TP-A5)	N	WHT
4	14	15.00	J1-4	.19	B9(TP-D5)	N	WHT
5	13	23.00	J1-5	.19	P11-16	19	SHLD
6	14	9.00	J1-6	.19	B1(TB2-B16)	N	WHT
7		9.00	J1-7	.19	B1(TB2-B1)	N	WHT
8		9.00	J1-8	.19	B1(TB2-B2)	N	WHT
9		9.00	J1-9	.19	B1(TB2-B3)	N	WHT
10	14	9.00	J1-10	.19	B1(TB2-B13)	N	WHT
11	14	23.00	J1-11	.19	B12(TP-A2)	N	
12	14	19.00	J1-12		B4(S30-3)	N	WHT
13		19.50	J1-13	.19	B12(TP-A8)	N	WHT
14		15.50	J1-14	.19	B9(TP-D8)	N	WHT
15	14	18.50	J1-15	.19	B8(TP-E4)	N	WHT
16	29	25.00	J1-16	.19	B24(TB1-8)	N	WHT/BRN
17	14	9.00	J1-17	.19	B1(TB2-B4)	N	WHT
18		9.00	J1-18	.19	B1(TB2-B5)	N	WHT
19		9.00	J1-19	.19	B1(TB2-B6)	N	WHT
20		9.00	J1-20	.19	B1(TB2-B12)	N	WHT
21		9.00	J1-21	.19	B1(TB2-B7)	N	WHT
22	14	9.00	J1-22	.19	B1(TB2-B7)	N	WHT
23	NOT	USED	J2-1				
24	14	4.00	J2-2	.19	J2-13	.19	WHT
25	14	21.00	J2-3	.19	P12-24	.19	WHT
26	16	25.00	J2-4	.19	B24(TB1-4)	N	ORN
27	14	15.00	J2-5	.19	B7(TP-F4)	N	WHT
28	NOT	USED	J2-6				
29	14	12.00	J2-7	.19	B2(TB2-A9)	N	WHT
30	NOT	USED	J2-8				
31	23	25.00	J2-9	.19	B24(TB1-5)	N	ORN
32	29	25.00	J2-10	.19	B24(TB1-8)	N	WHT/BRN
33	17	25.00	J2-11	.19	B24(TB1-10)	N	BLK
34	23	25.00	J2-12	.19	B24(TB1-4)	N	ORN
35	15	9.00	J1-5(SH)	.19	B1(TB2-B15)	N	BLK
36	14	21.00	J2-14	.19	P12-7	.19	WHT
37	NOT	USED	J2-15				
38	NOT	USED	J2-16				
39	NOT	USED	J2-17				
40	NOT	USED	J2-18				
41	NOT	USED	J2-19				
42	NOT	USED	J2-20				
43	14	15.00	J2-21	.19	B2(TB2-A9)	N	WHT
44	29	25.00	J2-22	.19	B24(TB1-8)	N	WHT/BRN

PTS Front Panel Wiring Diagram (Sheet 6 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
45	14	18.00	J2-23	.19	B9(TP-D6)	N	WHT
46	NOT	USED	J2-24				
47	NOT	USED	J2-25				
48	14	10.00	J3-1	.19	B1(TB2-B7)	N	WHT
49		10.00	J3-2	.19	B1(TB2-B8)	N	WHT
50		10.00	J3-3	.19	B1(TB2-B8)	N	WHT
51		10.00	J3-4	.19	B1(TB2-B8)	N	WHT
52	14	10.00	J3-5	.19	B1(TB2-B11)	N	WHT
53	NOT	USED	J3-6				
54	NOT	USED	J3-7				
55	NOT	USED	J3-8				
56	NOT	USED	J3-9				
57	NOT	USED	J3-10				
58	14	19.00	J3-11	.19	B8(TP-E6)	N	WHT
59		14.00	J3-12	.19	B7(TP-F6)	N	WHT
60		14.00	J3-13	.19	B12(TP-A7)	N	WHT
61		16.00	J3-14	.19	B11(TP-B7)	N	WHT
62	14	16.00	J3-15	.19	B10(TP-C7)	N	WHT
63	14	13.00	J3-16	.19	P6-1	.19	
64	14	13.00	J3-17	.19	P6-2	.19	
65	NOT	USED	J3-18				
66	NOT	USED	J3-19				
67	NOT	USED	J3-20				
68	NOT	USED	J3-21				
69	14	26.00	J3-22	.19	B24(TB1-20)	N	WHT
70	NOT	USED	J4-1				
71	NOT	USED	J4-2				
72	14	23.00	J4-3	.19	B7(TP-F9)	N	WHT
73	14	25.00	J4-4	.19	B9(TP-D9)	N	WHT
74	14	23.00	J4-5	.19	P1-26	.19	
75	NOT	USED	J4-6				
76	14	26.00	J4-7	.19	P2-18	.19	WHT
77		25.00	J4-8	.19	B9(TP-D10)	N	WHT
78		23.00	J4-9	.19	B7(TP-F10)	N	WHT
79		24.00	J4-10	.19	B8(TP-E9)	N	WHT
80		24.00	J4-11	.19	B8(TP-E10)	N	WHT
81	14	17.00	J4-12	.19	P14-24	.19	WHT
82	NOT	USED	J4-13				
83	14	19.00	J4-14	.19	P12-26	.19	WHT
84	14	18.00	J4-15	.19	P3-22	.19	WHT
85	14	17.00	J4-16	.19	P1-24	.19	WHT
86	14	25.00	J4-17	.19	B11(TP-B8)	N	WHT
87	17	10.00	J4-18	.19	B35(GND-E6)	N	BLK
88	NOT	USED	J4-19				

PTS Front Panel Wiring Diagram (Sheet 7 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
89	NOT	USED	J4-20				
90	14	17.00	J4-21	.19	P2-21	.19	WHT
91		17.00	J4-22	.19	P2-20	.19	WHT
92		17.00	J4-23	.19	P2-19	.19	WHT
93		19.00	J4-24	.19	P12-25	.19	WHT
94		17.00	J4-25	.19	P2-16	.19	WHT
95		20.00	J4-26	.19	B8(TP-E8)	N	WHT
96	14	17.00	J4-27	.19	P1-19	.19	WHT
97	NOT	USED	J4-28				
98	14	20.00	J4-29	.19	B8(TP-E3)	N	WHT
99	NOT	USED	J4-30				
100	14	17.00	J4-31	.19	P14-25	.19	WHT
101	14	17.00	J4-32	.19	P2-17	.19	WHT
102	NOT	USED	J4-33				
103	NOT	USED	J4-34				
104	14	17.00	J4-35	.19	P1-17	.19	WHT
105		17.00	J4-36	.19	P1-18	.19	WHT
106		17.00	J4-37	.19	P1-21	.19	WHT
107	14	19.00	J4-38	.19	B7(TP-F8)	N	WHT
108	NOT	USED	J4-39				
109	14	22.00	J4-40	.19	B9(TP-D2)	N	WHT
110	14	17.00	J4-41	.19	P1-25	.19	WHT
111	NOT	USED	J4-42				
112	14	17.00	J4-43	.19	P2-15	.19	WHT
113		17.00	J4-44	.19	P2-14	.19	WHT
114		17.00	J4-45	.19	P2-8	.19	WHT
115		17.00	J4-46	.19	P1-15	.19	WHT
116	14	17.00	J4-47	.19	P1-16	.19	WHT
117	NOT	USED	J4-48				
118	14	22.00	J4-49	.19	B9 (TP-D7)	N	WHT
119	14	20.00	J4-50	.19	B8(TP-E7)	N	WHT
120	NOT	USED	J4-51				
121	14	17.00	J4-52	.19	P2-1	.19	WHT
122		17.00	J4-53	.19	P2-3	.19	WHT
123		17.00	J4-54	.19	P2-9	.19	WHT
124		17.00	J4-55	.19	P1-1	.19	WHT
125		17.00	J4-56	.19	P1-14	.19	WHT
126		17.00	J4-57	.19	P1-13	.19	WHT
127		19.00	J4-58	.19	B7(TP-F7)	N	WHT
128		19.00	J4-59	.19	B7(TP-F3)	N	WHT
129		22.00	J4-60	.19	B9(TP-D3)	N	WHT
130		17.00	J4-61	.19	P2-2	.19	WHT
131		17.00	J4-62	.19	P2-4	.19	WHT
132	14	17.00	J4-63	.19	P2-10	.19	WHT

PTS Front Panel Wiring Diagram (Sheet 8 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
133	14	17.00	J4-64	.19	P1-2	.19	WHT
134		17.00	J4-65	.19	P1-6	.19	WHT
135		17.00	J4-66	.19	P1-12	.19	WHT
136		20.00	J4-67	.19	B8(TP-E2)	N	WHT
137		19.00	J4-68	.19	B7(TP-F2)	N	WHT
138		24.00	J4-69	.19	B12(TP-A3)	N	WHT
139		17.00	J4-70	.19	P2-5	.19	WHT
140	14	17.00	J4-71	.19	P2-11	.19	WHT
141	14	17.00	J4-72	.19	P1-3	.19	WHT
142		17.00	J4-73	.19	P1-7	.19	WHT
143		17.00	J4-74	.19	P1-11	.19	WHT
144		23.00	J4-75	.19	B11(TP-B3)	N	WHT
145		22.00	J4-76	.19	B10(TP-C3)	N	WHT
146		17.00	J4-77	.19	P2-6	.19	WHT
147		17.00	J4-78	.19	P2-12	.19	WHT
148		17.00	J4-79	.19	P1-4	.19	WHT
149		17.00	J4-80	.19	P1-8	.19	WHT
150		17.00	J4-81	.19	P1-10	.19	WHT
151		17.00	J4-82	.19	P2-7	.19	WHT
152		17.00	J4-83	.19	P2-13	.19	WHT
153		17.00	J4-84	.19	P1-5	.19	WHT
154	14	17.00	J4-85	.19	P1-9	.19	WHT
155	NOT	USED	J6-1				
156	14	24.00	J6-2	.19	P4-19	.19	WHT
157	14	18.00	J6-3	.19	B11(TP-B9)	N	WHT
158	NOT	USED	J6-4				
159	14	17.00	J6-5	.19	P7-2	.19	WHT
160	NOT	USED	J6-6				
161	14	19.00	J6-7	.19	P4-24	.19	WHT
162		30.00	J6-8	.19	P12-18	.19	WHT
163		30.00	J6-9	.19	P12-19	.19	WHT
164		30.00	J6-10	.19	P12-20	.19	WHT
165		30.00	J6-11	.19	P12-21	.19	WHT
166		19.00	J6-12	.19	P3-23	.19	WHT
167		19.00	J6-13	.19	P3-24	.19	WHT
168	14	19.00	J6-14	.19	P4-25	.19	WHT
169	NOT	USED	J6-15				
170	NOT	USED	J6-16				
171	NOT	USED	J6-17				
172	12	26.00	J6-18	.19	B24(TB1-26)	N	WHT/BLU
173	14	19.00	J6-19	.19	P3-17	.19	WHT
174		30.00	J6-20	.19	P12-17	.19	WHT
175		17.00	J6-21	.19	P7-1	.19	WHT
176	14	19.00	J6-22	.19	P3-26	.19	WHT

PTS Front Panel Wiring Diagram (Sheet 9 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
177		19.00	J6-23	.19	P4-18	.19	WHT
178		19.00	J6-24	.19	P4-16	.19	WHT
179	14	19.00	J6-25	.19	P4-17	.19	WHT
180	NOT	USED	J6-26				
181	14	19.00	J6-27	.19	P3-20	.19	WHT
182	14	19.00	J6-28	.19	P3-21	.19	WHT
183	NOT	USED	J6-29				
184	14	22.00	J6-30	.19	P14-22	.19	WHT
185	NOT	USED	J6-31				
186	14	19.00	J6-32	.19	P4-21	.19	WHT
187		19.00	J6-33	.19	P4-22	.19	WHT
188		19.00	J6-34	.19	P4-20	.19	WHT
189		19.00	J6-35	.19	P3-18	.19	WHT
190	14	19.00	J6-36	.19	P3-19	.19	WHT
191	NOT	USED	J6-37				
192	NOT	USED	J6-38				
193	NOT	USED	J6-39				
194	NOT	USED	J6-40				
195	14	17.00	J6-41	.19	P7-3	.19	WHT
196		19.00	J6-42	.19	P4-23	.19	WHT
197		19.00	J6-43	.19	P4-15	.19	WHT
198		19.00	J6-44	.19	P4-14	.19	WHT
199		19.00	J6-45	.19	P4-8	.19	WHT
200		19.00	J6-46	.19	P3-15	.19	WHT
201		19.00	J6-47	.19	P3-16	.19	WHT
202	14	22.00	J6-48	.19	P14-26	.19	WHT
203	NOT	USED	J6-49				
204	NOT	USED	J6-50				
205	14	19.00	J6-51	.19	P4-26	.19	WHT
206		19.00	J6-52	.19	P4-1	.19	WHT
207		19.00	J6-53	.19	P4-3	.19	WHT
208		19.00	J6-54	.19	P4-9	.19	WHT
209		19.00	J6-55	.19	P3-1	.19	WHT
210		19.00	J6-56	.19	P3-14	.19	WHT
211	14	19.00	J6-57	.19	P3-13	.19	WHT
212	NOT	USED	J6-58				
213	NOT	USED	J6-59				
214	NOT	USED	J6-60				
215	14	19.00	J6-61	.19	P4-2	.19	WHT
216		19.00	J6-62	.19	P4-4	.19	WHT
217		19.00	J6-63	.19	P4-10	.19	WHT
218		19.00	J6-64	.19	P3-2	.19	WHT
219		19.00	J6-65	.19	P3-6	.19	WHT
220	14	19.00	J6-66	.19	P3-12	.19	WHT

PTS Front Panel Wiring Diagram (Sheet 10 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
221	NOT	USED	J6-67				
222	NOT	USED	J6-68				
223	NOT	USED	J6-69				
224	14	19.00	J6-70	.19	P4-5	.19	WHT
225		19.00	J6-71	.19	P4-11	.19	WHT
226		19.00	J6-72	.19	P3-3	.19	WHT
227		19.00	J6-73	.19	P3-7	.19	WHT
228	14	19.00	J6-74	.19	P3-11	.19	WHT
229	NOT	USED	J6-75				
230	NOT	USED	J6-76				
231	14	19.00	J6-77	.19	P4-6	.19	WHT
232		19.00	J6-78	.19	P4-12	.19	WHT
233		19.00	J6-79	.19	P3-4	.19	WHT
234		19.00	J6-80	.19	P3-8	.19	WHT
235		19.00	J6-81	.19	P3-10	.19	WHT
236		19.00	J6-82	.19	P4-7	.19	WHT
237		19.00	J6-83	.19	P4-13	.19	WHT
238		19.00	J6-84	.19	P3-5	.19	WHT
239	14	19.00	J6-85	.19	P3-9	.19	WHT
240	NOT	USED					
241	NOT	USED	P5-1				
242	NOT	USED	P5-3				
243	NOT	USED	P5-5				
244	NOT	USED	P5-7				
245	NOT	USED	P5-9				
246	14	22.00	P1-20	.19	B8(TP-E8)	N	WHT
247	14	21.00	P1-22	.19	B7(TP-F8)	N	WHT
248	14	23.00	P1-23	.19	B11(TP-B8)	N	WHT
249	NOT	USED	P5-12				
250	14	23.00	P5-18	.19	B12-(TP-A2)	N	WHT
251	14	22.00	P2-22	.19	B9(TP-D7)	N	WHT
252		22.00	P2-23	.19	B8(TP-E7)	N	WHT
253		21.00	P2-24	.19	B7(TP-F7)	N	WHT
254		22.00	P2-25	.19	B8(TP-E3)	N	WHT
255	14	21.00	P2-26	.19	B7(TP-F3)	N	WHT
256	NOT	USED	P5-19				
257	14	36.00	P3-25	.19	P16-L	.19	WHT
258	NOT	USED	P5-22				
259	30	25.00	P5-2	.19	B24(TB1-6)	N	WHT/BRN
260	NOT	USED	P5-23				
261	NOT	USED	P5-26				
262	NOT	USED					
263	NOT	USED	P15-8				
264	NOT	USED	P5-10				

PTS Front Panel Wiring Diagram (Sheet 11 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
265	12	27.00	P5-13	.19	B24(TB1-30)	N	WHT/BLU
266	12	27.00	P5-14	.19	B24(TB1-30)	N	WHT/BLU
267	31	21.00	P5-15	.19	B12(TP-A10)	N	WHT/YEL
268	NOT	USED	P15-11				
269	NOT	USED	P15-12				
270	21	32.00	P5-20	.19	B24(TB1-23)	N	RED
271	NOT	USED	P15-13				
272	21	32.00	P5-24	.19	B24(TB1-23)	N	RED
273	23	29.00	P5-25	.19	B24(TB1-3)	N	ORN
274	13	25.00	B11(TP-B6)	N	B2(TB2-A7)	N	SHLD
275	13	25.00	B12(TP-A4)	N	B2(TB2-A2)	N	SHLD
276	13	25.00	B11(TP-B4)	N	B2(TB2-A5)	N	SHLD
277	13	25.00	B10(TP-C4)	N	B2(TB2-A6)	N	SHLD
278	14	21.00	P7-4	.19	B20(A13-1)	N	WHT
279	|	21.00	P7-5	.19	B20(A13-2)	N	WHT
280	|	21.00	P7-6	.19	B20(A13-6)	N	WHT
281	|	21.00	P7-7	.19	B20(A13-5)	N	WHT
282	|	21.00	P7-8	.19	B20(A13-7)	N	WHT
283	|	21.00	P7-9	.19	B20(A13-8)	N	WHT
284	|	21.00	P7-10	.19	B20(A13-9)	N	WHT
285	|	21.00	P7-11	.19	B20(A13-11)	N	WHT
286	|	21.00	P7-12	.19	B20(A13-12)	N	WHT
287	|	20.00	P7-13	.19	B16(S22-NC)	N	WHT
288	|	27.00	P7-14	.19	B15(S23-NC)	N	WHT
289	|	17.00	P7-15	.19	B18(S21-2)	N	WHT
290	|	20.00	P7-16	.19	B35(DS9-C)	N	WHT
291	|	27.00	P7-17	.19	B30(S1-2)	N	WHT
292	|	27.00	P7-18	.19	B30(S1-3)	N	WHT
293	|	27.00	P7-19	.19	B30(S1-4)	N	WHT
294	|	25.00	P7-20	.19	B31(S3-2)	N	WHT
295	|	25.00	P7-21	.19	B31(S3-3)	N	WHT
296	|	30.00	P7-22	.19	B29(S2-1)	N	WHT
297	|	30.00	P7-23	.19	B29(S2-2)	N	WHT
298	|	35.00	P7-24	.19	B26(S6-6)	N	WHT
299	|	35.00	P7-25	.19	B26(S6-5)	N	WHT
300	|	35.00	P7-26	.19	B22(S5-D1)	N	WHT
301	|	35.00	P8-1	.19	B22(S5-D2)	N	WHT
302	|	35.00	P8-2	.19	B22(S5-D3)	N	WHT
303	|	27.00	P8-3	.19	B26(S6-2)	N	WHT
304	|	27.00	P8-4	.19	B26(S6-3)	N	WHT
305	|	27.00	P8-5	.19	B26(S6-4)	N	WHT
306	|	27.00	P8-6	.19	B23(S7-2)	N	WHT
307	14	27.00	P8-7	.19	B23(S7-3)	N	WHT

PTS Front Panel Wiring Diagram (Sheet 12 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
308	14	27.00	P8-8	.19	B23(S7-1)	N	WHT
309		19.00	P8-9	.19	B33(S10-3)	N	WHT
310		19.00	P8-10	.19	B33(S10-1)	N	WHT
311		34.00	P8-11	.19	B21(S24-B)	N	WHT
312		35.00	P8-12	.19	B24(TB1-20)	N	WHT
313		21.00	P8-13	.19	B16(S20-NO)	N	WHT
314		22.00	P8-14	.19	B16(S16-NO)	N	WHT
315		22.00	P8-15	.19	B16(S19-NO)	N	WHT
316		22.00	P8-16	.19	B16(S13-C)	N	WHT
317		21.00	P8-17	.19	B16(S20-C)	N	WHT
318		22.00	P8-18	.19	B16(S19-C)	N	WHT
319		22.00	P8-19	.19	B16(S16-C)	N	WHT
320		16.00	P8-20	.19	B18(S21-3)	N	WHT
321		20.00	P8-21	.19	B3(DS11-C)	N	WHT
322	▼	20.00	P8-22	.19	B3(DS12-C)	N	WHT
323	14	20.00	P8-23	.19	B3(DS10-C)	N	WHT
324	23	26.00	P8-24	.19	B20(A13-3)	N	WHT
325	14	26.00	P8-25	.19	B20(A13-4)	N	WHT
326		26.00	P8-26	.19	B20(A13-10)	N	WHT
327		33.00	P9-1	.19	P16-C	.19	WHT
328		33.00	P9-2	.19	P16-D	.19	WHT
329		33.00	P9-3	.19	P16-H	.19	WHT
330		33.00	P9-4	.19	P16-A	.19	WHT
331		33.00	P9-5	.19	P16-R	.19	WHT
332		33.00	P9-6	.19	P16-K	.19	WHT
333		33.00	P9-7	.19	P16-S	.19	WHT
334		33.00	P9-8	.19	P16-YY	.19	WHT
335		33.00	P9-10	.19	P16-SS	.19	WHT
336		33.00	P9-11	.19	P16-ZZ	.19	WHT
337		33.00	P9-12	.19	P16-TT	.19	WHT
338		33.00	P9-13	.19	P16-U	.19	WHT
339		33.00	P9-14	.19	P16-NN	.19	WHT
340		33.00	P9-15	.19	P16-V	.19	WHT
341		33.00	P9-16	.19	P16-F	.19	WHT
342		33.00	P9-17	.19	P16-WW	.19	WHT
343		33.00	P9-18	.19	P16-Z	.19	WHT
344		33.00	P9-19	.19	P16-P	.19	WHT
345		33.00	P9-20	.19	P16-B	.19	WHT
346		20.00	P9-21	.19	B17(S28-D1)	N	WHT
347		20.00	P9-22	.19	B17(S28-D2)	N	WHT
348		20.00	P9-23	.19	B17(S28-D3)	N	WHT
349	▼	27.00	P9-24	.19	B27(S26-3)	N	WHT
350	14	29.00	P9-25	.19	B28(S27-3)	N	WHT

PTS Front Panel Wiring Diagram (Sheet 13 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
351	14	19.00	P9-26	.19	B32(S9-3)	N	WHT
352		33.00	P9-9	.19	P16-XX	.19	WHT
353		33.00	P11-1	.19	B8(TP-E2)	N	WHT
354		32.00	P11-2	.19	B7(TP-F2)	N	WHT
355		36.00	P11-3	.19	B12(TP-A3)	N	WHT
356		35.00	P11-4	.19	B11(TP-B3)	N	WHT
357		34.00	P11-5	.19	B10(TP-C3)	N	WHT
358		34.00	P11-6	.19	B9(TP-D3)	N	WHT
359		33.00	P11-7	.19	B8(TP-E6)	N	WHT
360		32.00	P11-8	.19	B7(TP-F6)	N	WHT
361		36.00	P11-9	.19	B12(TP-A7)	N	WHT
362	14	35.00	P11-10	.19	B11(TP-B7)	N	WHT
363	13	37.00	P11-11	.19	B2(TB2-A2)	N	SHLD
364	13	37.00	P11-12	.19	B2(TB2-A5)	N	SHLD
365	13	37.00	P11-13	.19	B2(TB2-A3)	N	SHLD
366	13	37.00	P11-14	.19	B2(TB2-A6)	N	SHLD
367	29	40.00	P11-15	.19	B24(TB1-6)	N	WHT/BRN
368	NOT	USED					
369	14	34.00	P11-17	.19	B9(TP-D5)	N	WHT
370		35.00	P11-18	.19	B11(TP-B5)	N	WHT
371		34.00	P11-19	.19	B10(TP-C5)	N	WHT
372	14	36.00	P11-20	.19	B12(TP-A5)	N	WHT
373	13	37.00	P11-21	.19	B2(TB2-A7)	N	SHLD
374	14	36.00	P11-22	.19	B12(TP-A8)	N	WHT
375		33.00	P11-23	.19	B7(TP-F10)	N	WHT
376		34.00	P11-24	.19	B9(TP-D9)	N	WHT
377		34.00	P11-25	.19	B9(TP-D10)	N	WHT
378		34.00	P11-26	.19	B10(TP-C7)	N	WHT
379		33.00	P12-1	.19	B8(TP-E10)	N	WHT
380		32.00	P12-2	.19	B7(TP-F9)	N	WHT
381	14	34.00	P12-3	.19	B9(TP-D8)	N	WHT
382	13	37.00	P12-4	.19	B2(TB2-A4)	N	SHLD
383	13	37.00	P12-5	.19	B2(TB2-A1)	N	SHLD
384	14	33.00	P12-6	.19	B8(TP-E4)	N	WHT
385		34.00	P12-23	.19	B9(TP-D2)	N	WHT
386		37.00	P12-8	.19	B2(TB2-A9)	N	WHT
387		32.00	P12-9	.19	B7(TP-F4)	N	WHT
388		37.00	P12-10	.19	P15-4	.19	WHT
389		37.00	P12-11	.19	P15-1	.19	WHT
390		37.00	P12-12	.19	P15-2	.19	WHT
391		37.00	P12-13	.19	P15-3	.19	WHT
392	14	37.00	P12-14	.19	P15-5	.19	WHT
393	29	42.00	P12-15	.19	B24(TB1-7)	N	WHT/BRN
394	13	35.00	P12-16	.19	B4(J5)	N	SHLD

PTS Front Panel Wiring Diagram (Sheet 14 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
395	13	25.00	B8(TP-E5)	N	B2(TB2-A4)	N	SHLD
396	14	32.00	P14-23	.19	B8(TP-E9)	N	WHT
397		25.00	P14-1	.19	B43(DS1-C)	N	WHT
398		25.00	P14-2	.19	B42(DS2-C)	N	WHT
399		25.00	P14-3	.19	B41(DS3-C)	N	WHT
400		25.00	P14-4	.19	B40(DS4-C)	N	WHT
401		24.00	P14-5	.19	B39(DS5-C)	N	WHT
402		24.00	P14-6	.19	B38(DS6-C)	N	WHT
403		24.00	P14-7	.19	B37(DS7-C)	N	WHT
404		23.00	P14-8	.19	B36(DS8-C)	N	WHT
405		31.00	P14-9	.19	B6(DS14-C)	N	WHT
406		31.00	P14-10	.19	B6(DS13-C)	N	WHT
407		40.00	P14-11	.19	B14(LS1-A)	N	WHT
408		40.00	P14-12	.19	B14(LS1-B)	N	WHT
409		30.00	P14-13	.19	B34(R1-3)	N	WHT
410		30.00	P14-14	.19	B34(R1-1)	N	WHT
411	14	30.00	P14-15	.19	B34(R1-2)	N	WHT
412	24	32.00	P14-16	.19	B12(TP-A9)	N	WHT/ORN/VIO
413	17	39.00	P14-17	.19	B24(TB1-10)	N	BLK
414	14	32.00	P14-18	.19	B12(TP-A6)	N	WHT
415	14	34.00	P14-19	.19	P15-7	.19	WHT
416	14	29.00	P14-20	.19	B19(S25-NC1)	N	WHT
417	13	29.00	P14-21	.19	B4(J7)	N	SHLD
418	13	25.00	B7(TP-F5)	N	B2(TB2-A1)	N	SHLD
419	15	39.00	P15-6	.19	B24(TB1-9)	N	BLK
420	16	39.00	P15-9	.19	B24(TB1-3)	N	ORN
421	15	39.00	P15-10	.19	B24(TB1-9)	N	BLK
422	21	29.00	P16-W	.19	B24(TB1-22)	N	RED
423	12	29.00	P16-EE	.19	B24(TB1-29)	N	WHT/BLU
424	21	29.00	P16-KK	.19	B24(TB1-22)	N	RED
425	12	29.00	P16-JJ	.19	B24(TB1-29)	N	WHT/BLU
426	8	40.00	P17-A	.19	B4(S30-2)	N	WHT/GRN
427	29	39.00	P17-B	.19	B24(TB1-7)	N	WHT/BRN
428	20	37.00	P17-C	.19	B12(TP-A9)	N	WHT/BRN/VIO
429	19	36.00	P17-D	.19	B11(TP-B10)	N	BRN
430	25	31.00	P17-E	.19	P5-4	.19	YEL
431	26	31.00	P17-F	.19	P5-6	.19	GRN
432	17	39.00	P17-H	.19	B24(TB1-11)	N	BLK
433	27	31.00	P17-J	.19	P5-8	.19	VIO
434	18	35.00	P17-L	.19	B10(TP-C9)	N	WHT/BLK/VIO
435	12	31.00	P17-M	.19	P5-11	.19	WHT/BLU
436	12	39.00	P17-P	.19	B24(TB1-27)	N	WHT/BLU
437	12	39.00	P17-R	.19	B24(TB1-26)	N	WHT/BLU
438	31	37.00	P17-S	.19	B12(TP-A10)	N	WHT/YEL

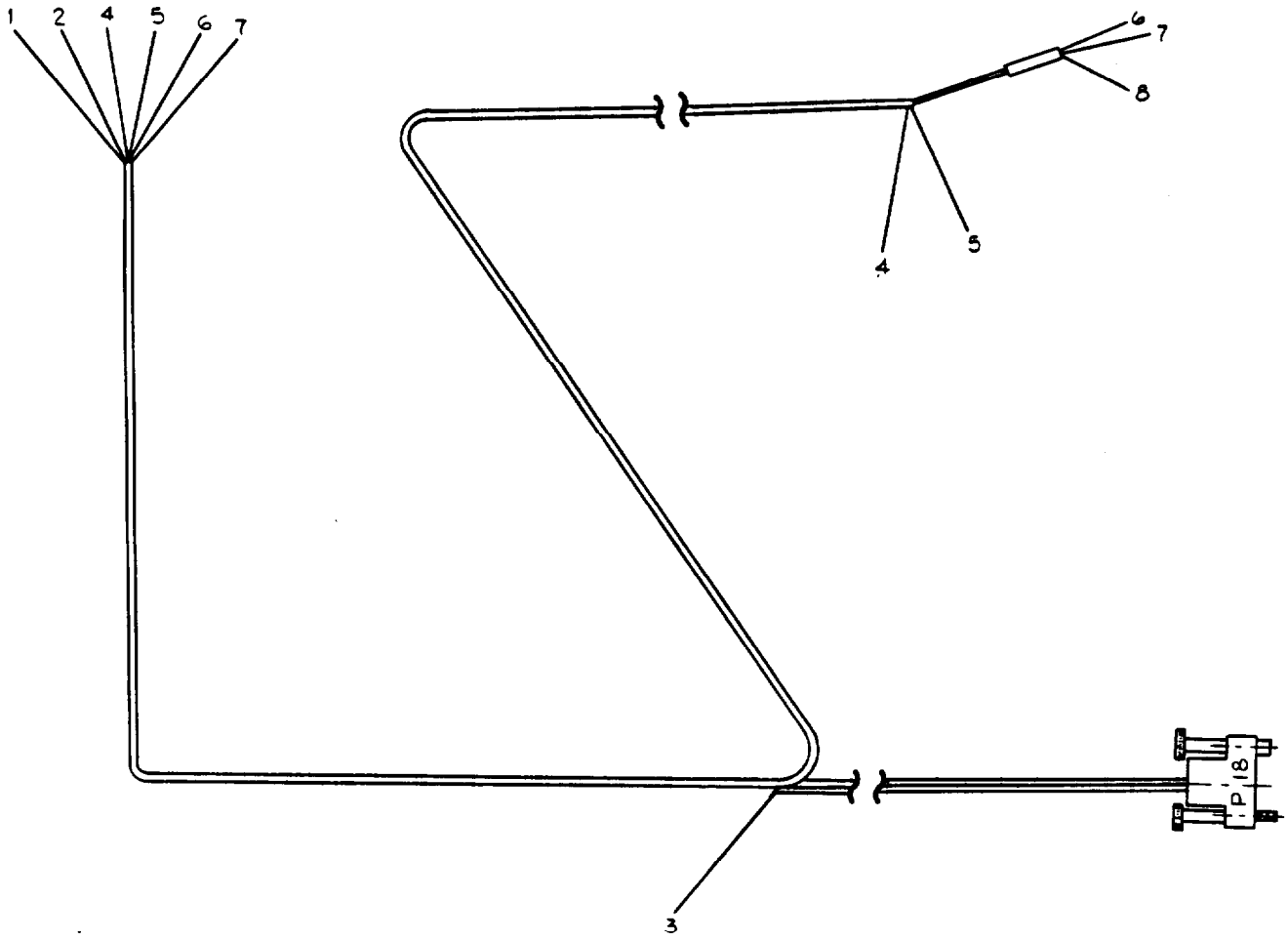
PTS Front Panel Wiring Diagram (Sheet 15 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
439	14	35.00	P17-T	.19	B10(TP-C10)	N	WHT
440	14	31.00	P17-U	.19	P5-17	.19	WHT
441	28	22.00	P17-V	.19	P16-CC	.19	GRA
442	14	31.00	P17-W	.19	P5-16	.19	WHT
443	21	39.00	P17-X	.19	B24(TB1-21)	N	RED
444	21	31.00	P17-Y	.19	P5-21	N	RED
445	30	35.00	P17-a	.19	B10(TP-C8)	N	WHT/ORN
446	21	39.00	P17-b	.19	B24(TB1-25)	N	RED
447	23	39.00	P17-c	.19	B24(TB1-5)	N	ORN
448	20	36.00	P17-d	.19	B11(TP-B9)	N	WHT/BRN/VIO
449	NOT	USED	P17-K				
450	NOT	USED	P17-N				
451	NOT	USED	P17-Z				
452	NOT	USED	P16-E				
453	NOT	USED	P16-Y				
454	NOT	USED	P16-X				
455	NOT	USED	P16-BB				
456	NOT	USED	P16-FF				
457	NOT	USED	P16-HH				
458	NOT	USED	P16-LL				
459	NOT	USED	P16-J				
460	NOT	USED	P16-DD				
461	NOT	USED	P16-M				
462	22	37.00	B12(TP-A8)	N	B24(TB1-19)	N	WHT/BLK
463	17	35.00	B12(TP-GND)	N	B24(TB1-11)	N	BLK
464	14	19.00	B9(TP-D8)	N	B13(R4-A)	N	WHT
465	21	21.00	B43(DS1-A)	N	B3(DS10-A)	N	RED
466	21	17.00	B3(DS12-A)	N	B6(DS13-A)	N	RED
467	21	33.00	B6(DS14-A)	N	B24(TB1-25)	N	RED
468	12	10.00	B4(DS16-C)	N	B5(S8-c1)	N	WHT/BLU
469		11.00	B5(S8-c1)	N	B17(S28-C)	N	WHT/BLU
470		30.00	B17(S28-c)	N	B24(TB1-26)	N	WHT/BLU
471		9.00	B33(S10-2)	N	B32(S9-2)	N	WHT/BLU
472		13.00	B32(S9-2)	N	B19(S25-c1)	N	WHT/BLU
473		15.00	B19(S25-C)	N	B20(A13-13)	N	WHT/BLU
474		27.00	B20(A13-13)	N	B24(TB1-27)	N	WHT/BLU
475		11.00	B31(S3-C)	N	B30(S1-C)	N	WHT/BLU
476		11.00	B30(S1-C)	N	B29(S2-C)	N	WHT/BLU
477		9.00	B29(S2-C)	N	B28(S27-2)	N	WHT/BLU
478	▼	11.00	B28(S27-2)	N	B27(S26-2)	N	WHT/BLU
479	12	11.00	B27(S26-2)	N	B26(S6-C)	N	WHT/BLU
480	NOT	USED					
481	12	23.00	B26(S6-C)	N	B24(TB1-28)	N	WHT/BLU
482	12	19.00	B16(S22-C)	N	B15(S23-C)	N	WHT/BLU
483	12	35.00	B15(S23-C)	N	B21(S24-A)	N	WHT/BLU

PTS Front Panel Wiring Diagram (Sheet 16 of 17)

WIRE RUNS							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
484	12	11.00	B21(S24-A)	N	B23(S7-C)	N	WHT/BLU
485	↓	15.00	B23(S7-C)	N	B22(S5-C)	N	WHT/BLU
486	12	23.00	B22(S5-C)	N	B24(TB1-28)	N	WHT/BLU
487	21	33.00	B5(S8-1)	N	B24(TB1-24)	N	RED
488	21	15.00	B19(S25-C2)	N	B20(A13-14)	N	RED
489	21	13.00	B20(A13-14)	N	B24(TB1-21)	N	RED
490	12	37.00	B13(R4-B)	N	B24(TB1-27)	N	WHT/BLU
491	21	19.00	B16(S22-1)	N	B15(S23-1)	N	RED
492	21	40.00	B15(S23-1)	N	B23(TB1-24)	N	RED
493	14	33.00	B5 (S8-NC)	N	B24(TB1-20)	N	WHT
494	14	21.00	P6-15	.19	B30(S1-5)	N	WHT
495	14	21.00	P6-16	.19	B30 (S1-6)	N	WHT
496	14	24.00	P6-17	.19	B29(S2-3)	N	WHT
497	14	24.00	P6-18	.19	B29(S2-4)	N	WHT
498	14	21.00	P6-19	.19	B28(S27-1)	N	WHT
499	14	22.00	P6-14	.19	B12(TP-A1)	N	WHT
500	14	22.00	P6-6	.19	B11(TP-B1)	N	WHT
501	14	22.00	P6-7	.19	B11(TP-B2)	N	WHT
502	14	22.00	P6-5	.19	B12(TP-A2)	N	WHT
503	NOT	USED					
504	8	24.00	B14 ET1 (+)	N	B4(S30-2)	N	WHT/GRN
505	12	11.00	B14 ET1 (-)	N	B13 GND R4B	N	WHT/BLK
506	13	26.00	R9 TP-D4	N	B2(TB2-A3)	N	COAX
507	NOT	USED	P6-3				
508	NOT	USED	P6-4				
509	NOT	USED	P6-8				
510	NOT	USED	P6-9				
511	NOT	USED	P6-10				
512	NOT	USED	P6-11				
513	NOT	USED	P6-12				
514	NOT	USED	P6-13				
515	NOT	USED	P6-20				
516	NOT	USED	P6-21				
517	NOT	USED	P6-22				
518	NOT	USED	P6-23				
519	NOT	USED	P6-24				
520	NOT	USED	P6-25				
521	NOT	USED	P6-26				
522	NOT	USED	P16-N				
523	NOT	USED	P16-T				
524	NOT	USED	P16-AA				
525	NOT	USED	P16-MM				
526	NOT	USED	P16-PP				
527	NOT	USED	P16-RR				
528	NOT	USED	P16-UU				
529	NOT	USED	P16-VV				

PTS Front Panel Wiring Diagram (Sheet 17 of 17)



WIRE RUN							
WIRE NO.	FIND NO.	LENGTH INCHES	FROM		TO		COLOR REF
			REF DES	STRIP	REF DES	STRIP	
1	2	26	P18-A	.19	L1-F	N	WHT
2	3	26	P18-H	.19	L2-B	N	WHT/BLK
3	4	14	P18-D	.19	TB1-GND	N	BLK
4	5	41	E19	N	B1-RED	N	WHT
5	6	41	E15	N	B1-YEL	N	WHT/BLK
6	7	40	L1-E	N	FL1	N	WHT
7			L1-C	N	FL2	N	BLK
8	8	3	SHLD OF WIRES 6&7	.19	E20	N	BLK

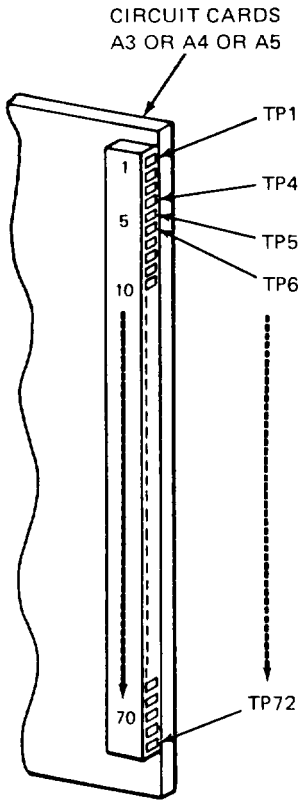
NOTES

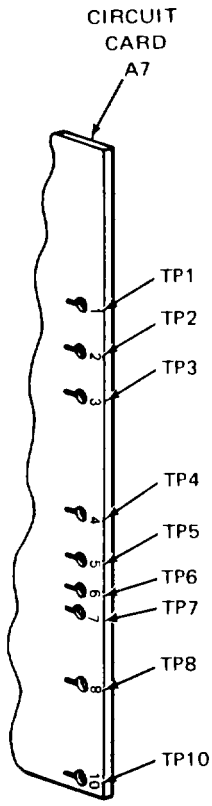
1. MARK REFERENCE DESIGNATION ,P18 IN 12 HIGH CHARACTERS USING BLACK MARKING INK , FIND NO. II
2. SOLDER IN ACCORDANCE WITH MIL-STD-454 REQUIREMENT 5 USING QQ5-571 FIND NO.9
3. HARNESS SHALL BE LACED WITH FIND NO 10
4. WORKMANSHIP SHALL COMPLY WITH REQUIREMENTS OF MIL-STD-454.

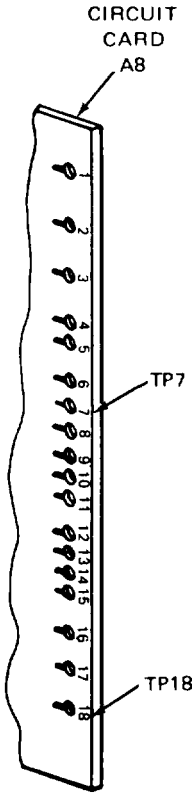
PTS Power Wiring Harness Diagram

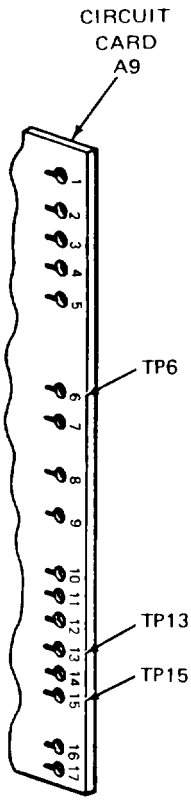
CHOKE ASSEMBLY WIRE RUN LIST						
WIRE NO	LENGTH INCHES	FROM		TO		COLOR REF
		REF DES	STRIP	REF DES	STRIP	
1	3	L1-D	.19	E-15	.19	WHT
2	2	L1-F	.19	E-19	.19	WHT
3	4	L2-A	.19	E-21	.19	WHT
4	4	E-21	.19	E-15	.19	WHT
5	1	E-16	.19	E-19	.19	WHT
6	1	E-17	N	E-13	N	BUSS
7	2	E-18	N	E-20 GND	N	BUSS

Choke Assembly Wire Run List

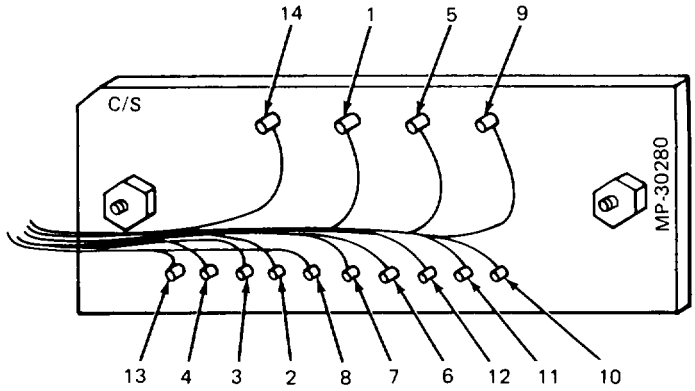




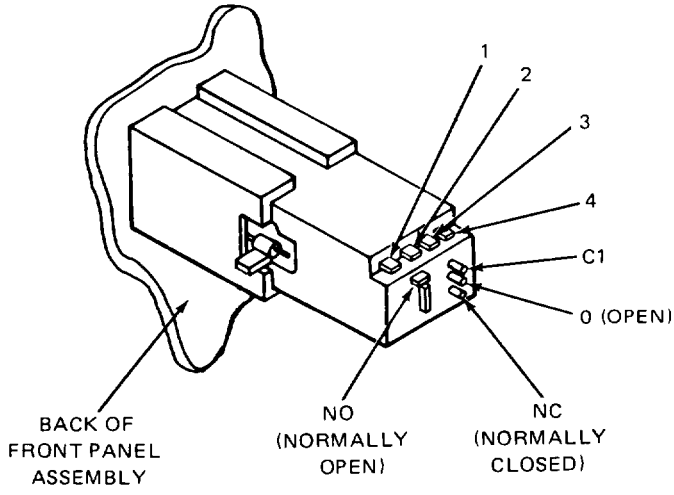




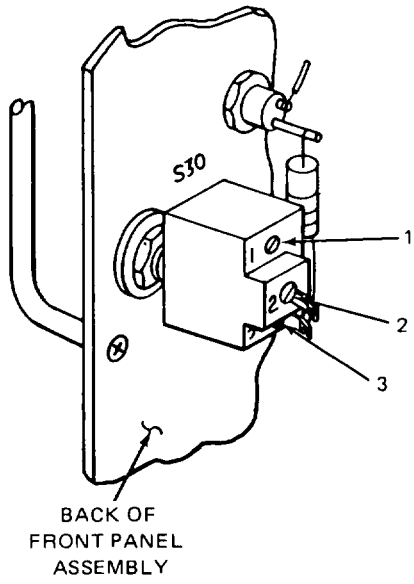
Test Point Layout



NUMERICAL DISPLAY A13



SWITCH S8



SWITCH S30

Pin Number Layout

SECTION VI

MAINTENANCE PROCEDURES

SECTION CONTENTS

SECTION CONTENTS PAGE

GENERAL

4-33. Maintenance of the PTS includes cleaning, touchup painting, and repair as needed. You will perform maintenance whenever you find bent, broken, dirty, or corroded items before, during or after operation or during preventive maintenance checks and services.

INSPECTION

4-34. In addition to inspecting the PTS as a part of normal operation, you should inspect it after a long period of storage or after it has had rough treatment (such as a long, difficult move). Look for damage, dirt, corrosion or rust, scratches, dents, and missing items. Be sure your PTS is operationally ready. If you do find something wrong, repair the test set and get it into top shape.

CLEANING

4-35. Proper cleaning will prevent dirt, grease, fungus, and other materials from building up and eventually disabling the test set.

CAUTION

Do not press on the radar signal indicator glass during cleaning; you could cause an implosion.

- Clean the PTS with a soft, clean cloth. Use a soft brush to clean the lamp, meter, switches, and connectors.

- When dirt and dust are heavy, remove the PTS from its case and clean it with a vacuum cleaner; use a soft, brush type nozzle.

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be AVOIDED. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

- Remove fungus, ground-in dirt, and grease from metal surfaces and cables, using a cloth dampened (not wet) with TRICHLOROTRIFLUOROETHANE.

- Use a soft bristle brush to remove dust and dirt from cable and PTS receptacles.

- Clean other non-metal surfaces with a clean, dry cloth. To remove dirt, dampen the cloth with a mild soap and water solution.

TOUCH-UP PAINTING

4-36. Look at TB 43-0118, Field Instructions for Painting and Preserving Electronics Command Equipment for touchup painting instructions.

REPAIR

4-37. Repair consists of taking the necessary action to fix items of the PTS. Within the limits of your spare parts supply, your tools, and your experience, you may do these repairs, using normal shop practices. Here are the jobs you may perform:

- Replacement of front panel components:
  - Switches
  - Lamp bulbs, lenses and LEDs
  - Fuses
- Repair of transit case by replacement of major components
- Replacement of circuit cards
  - Computer/DMA circuit card A2
  - Video Generator circuit card A7
  - Display/ Protect circuit card A8
  - Analog Signal circuit card A9
  - Memory/Power Strobe circuit card A1
  - Analog Control Interface circuit card A4
  - Digital Signal Processor circuit card A3
  - Computer Interface circuit card A5
- Replacement of assemblies
  - Processor Test Set TS-3706A/APM-415
  - Magnetic Tape Cassette Transport
  - Low Voltage Power Supply PS1
  - Numeric Display Assembly
  - Radar Signal Indicator
  - Card Cage Assembly
  - Case
  - Cables W1 thru W5 and Power Adapter

NOTE

When you install any component parts using screw-type hardware, use Ioctite (Grade CV) Nut Lock on the threads.

CASE ASSEMBLY TOP COVER REMOVAL AND INSTALLATION

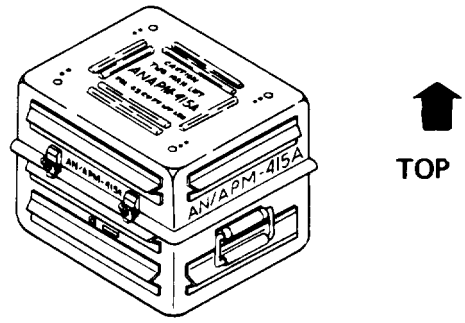
4-38. This paragraph provides you with instructions for removal and installation of the case assembly top cover.

a. Tools and Materials:

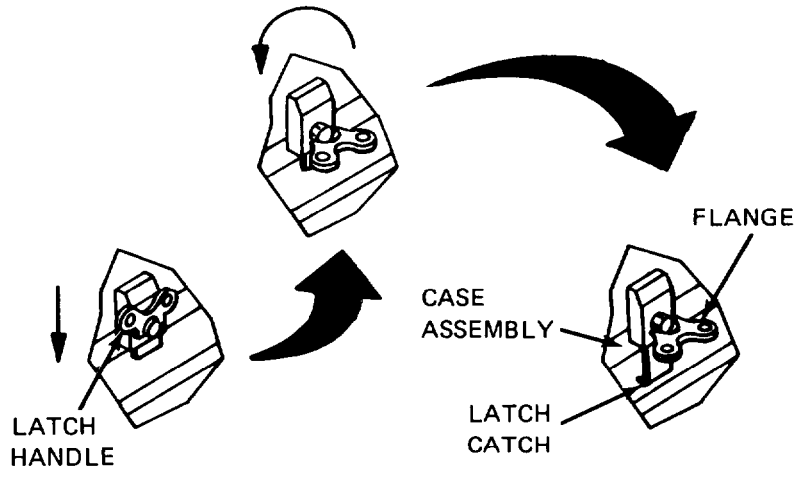
1. Tool Kit, Electronic Equipment TK-105/G
2. Case Assembly

b. Case Assembly top Cover Removal and Disassembly:

1 **Position PTS top up on a secure working surface.**

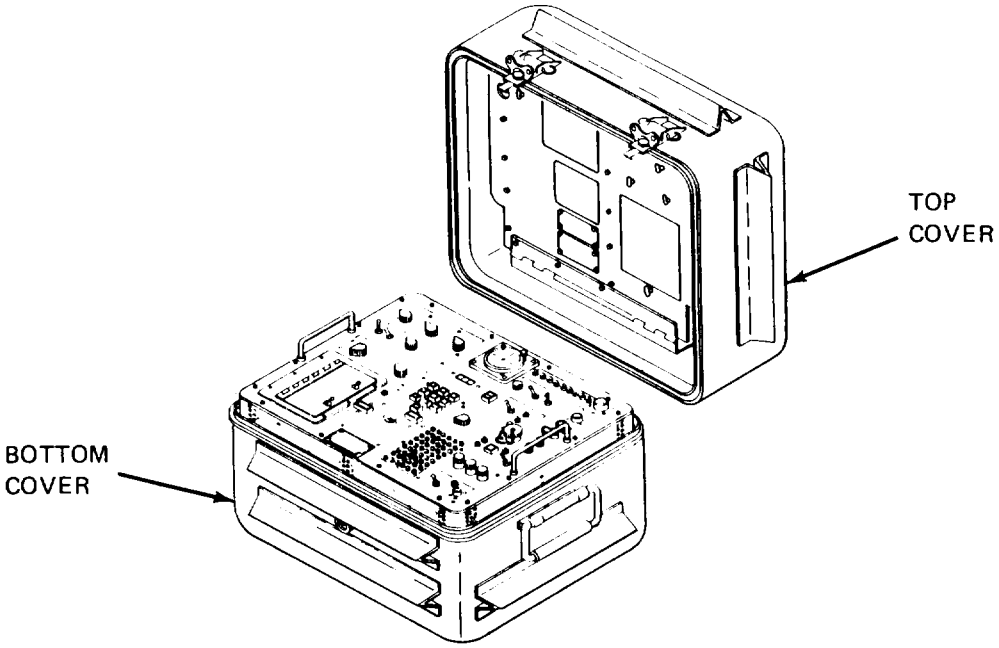


2 **Depress pressure relief valve to release internal pressure, then fold four latch handles to middle position and turn latch handles counterclockwise until latch catch releases fully from case assembly flange.**



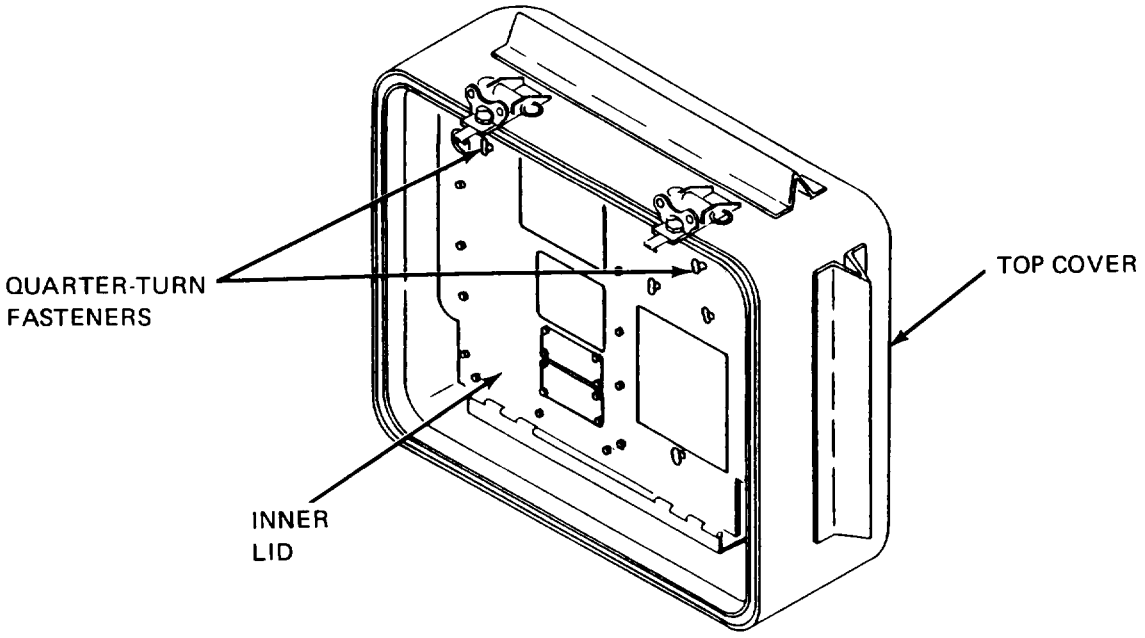
3

Lift case assembly top cover free from case assembly bottom cover. Place top cover on a secure surface, away from working area.



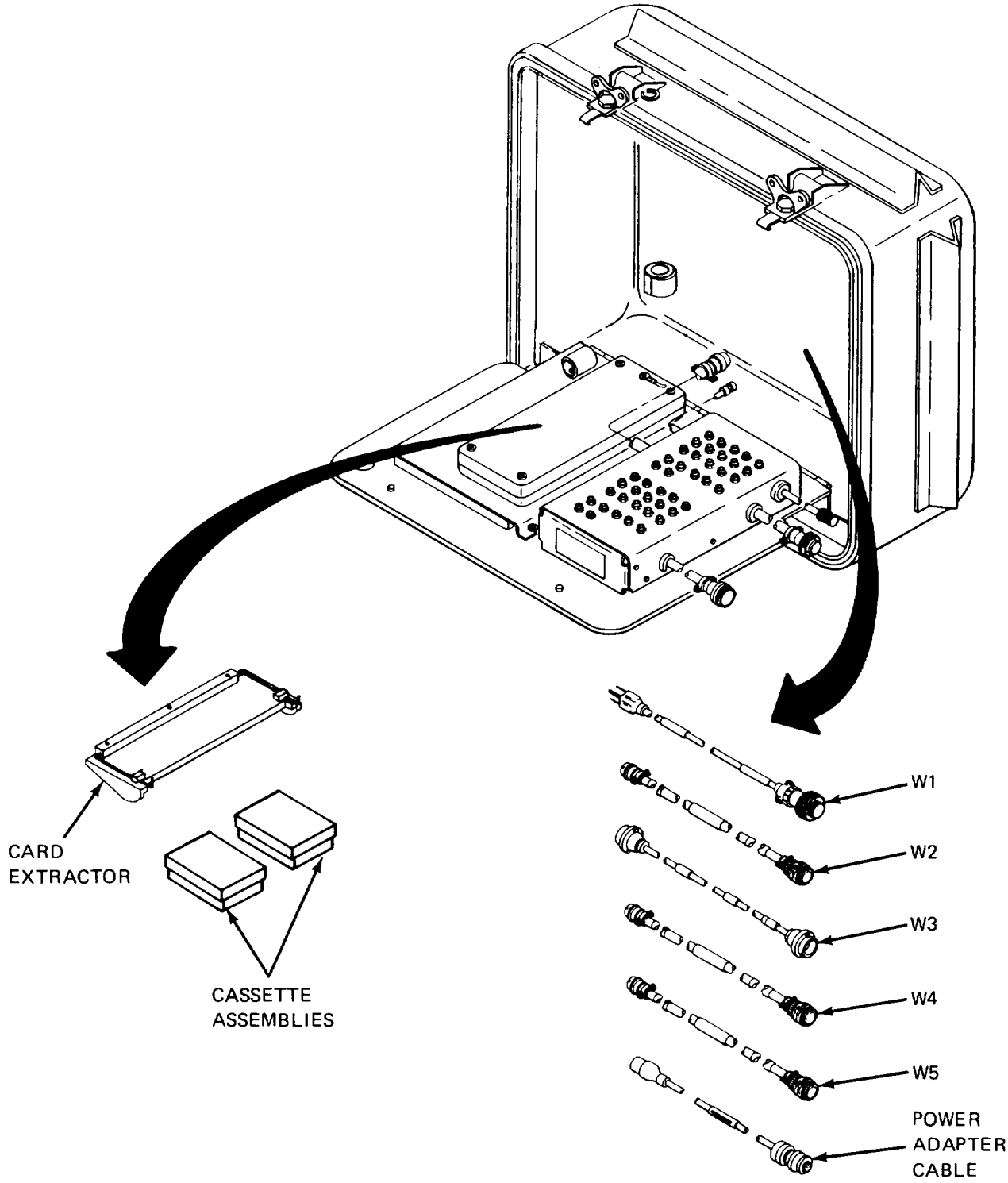
4

Release two quarter-turn fasteners and fold down inner lid.



5

Remove (as required) cable assemblies W1 thru W5, adapter cable, card extractor, and/or cassettes.



c. Case Assembly Top Cover Assembly and Installation:

1. Replace (as required) cable assemblies W1 thru W5, adapter cable, card extractor and /or cassettes.

2. Fold up inner lid and secure using two quarter-turn fasteners.

3. Position top cover on the bottom cover assembly.

4. Position latch catch so that it engages flange when latch is closed.

5. Turn four butterfly latch handles clockwise until latch catch engages flange and is finger tight. Fold latch handles upward.

FRONT PANEL ASSEMBLY REMOVAL AND INSTALLATION

4-39. This paragraph provides you with instructions for removal and installation of the front panel assembly.

a. Tools and Material:

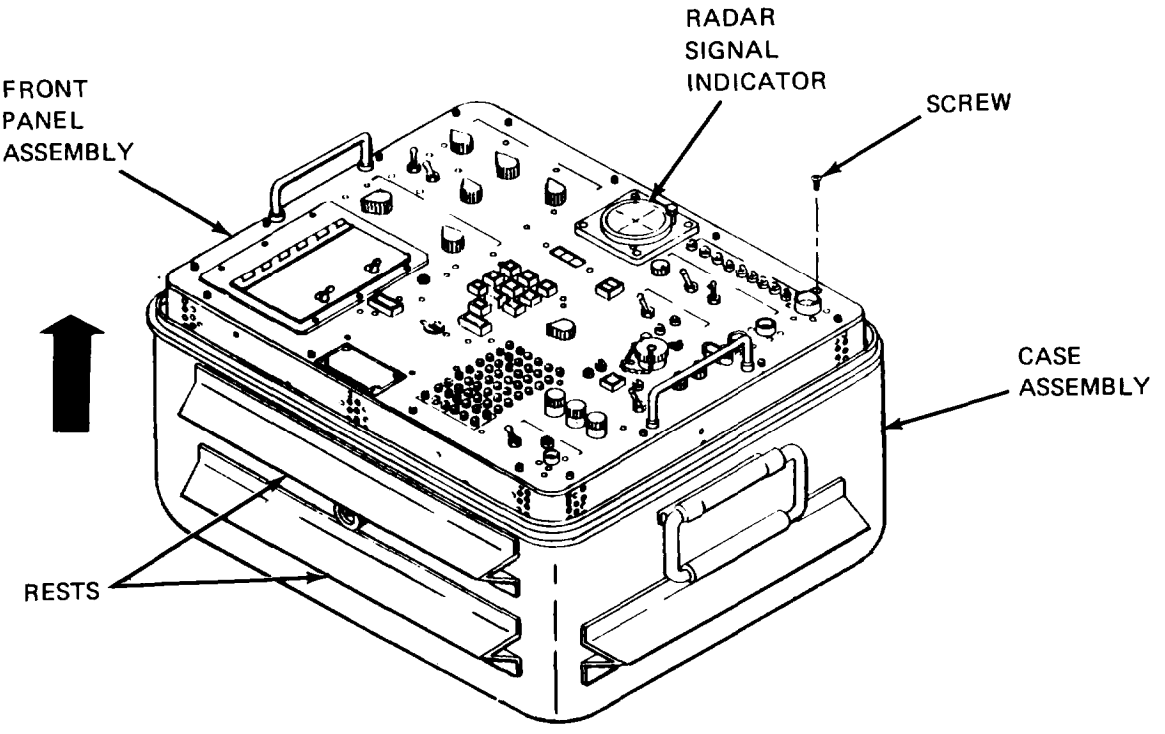
1. Tool Kit, Electronics Equipment TK-105/G
2. Front Panel Assembly
3. Case Assembly

b. Front Panel Assembly Removal:

1. Perform the removal procedures of paragraph 4-38b, then position PTS so that radar signal indicator is located at the top of the PTS and the PTS is sitting on the four rear dimples.

2. Remove 16 screws with flat and lockwashers, holding front panel assembly to case

3 Carefully lift front panel assembly free from case assembly and place unit in a convenient position on a secure surface.



c. Front Panel Assembly Installation:

4 Place case assembly on secure working surface, sitting on four rear dimples with pressure relief valve facing you.

5 Carefully lower front panel assembly into the case assembly with the radar signal indicator at the top (away from you).

6 Secure front panel assembly to case assembly using 1-8 screws.

7 Perform the installation procedure of paragraph 4-38c.

CIRCUIT CARD A1 THRU A5, AND A7 THRU A9 REMOVAL AND INSTALLATION

4-40. This paragraph provides you with instructions for removal and installation of circuit cards A1 thru A5 and A7 thru A9.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Circuit Cards (As Required)

- Memory/Power Strobe Circuit Card A1
- Computer/DMA Circuit Card A2
- Digital Signal Processor Circuit Card A3
- Analog Control Interface Circuit Card A4
- Computer Interface Circuit Card A5
- Video Generator Circuit Card A7
- Display Protect Circuit Card A8
- Analog Signal Interface Circuit Card A9

❑ Card Puller C5079575 (located inside top cover, refer to paragraph 4-38 Q).

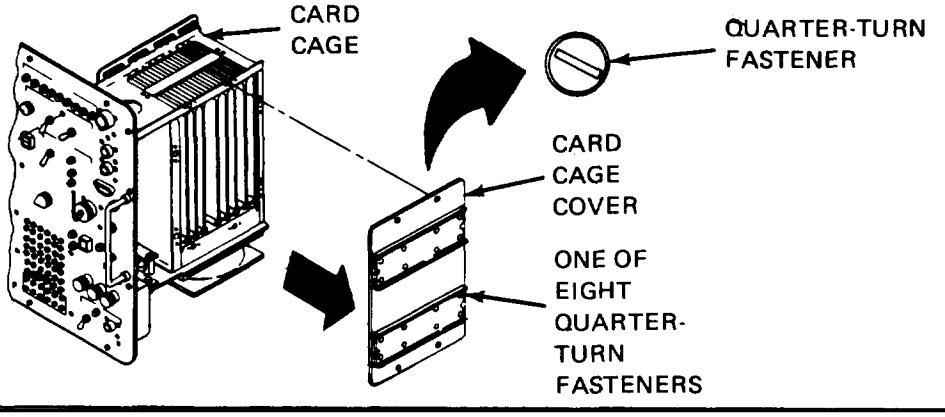
b. Circuit Card Removal:

1 Perform the removal procedures provided in paragraphs 4-38b and 4-39b.

NOTE

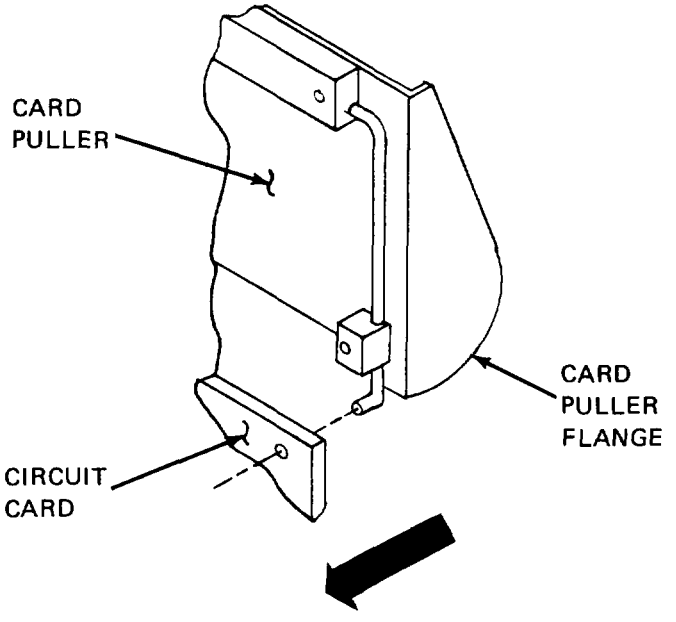
Be sure front panel is stable before proceeding to step 2,

2 On card cage cover, turn eight quarter-turn fasteners, one quarter turn each, counterclockwise. Then lift card cage cover free from card cage.



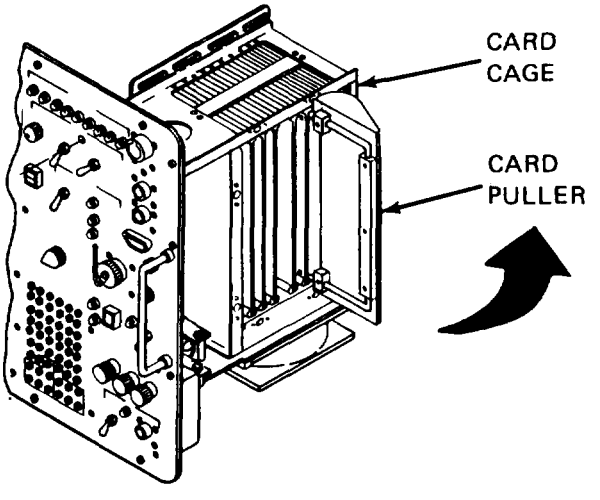
3

Gently insert card puller into two holes in top edge of circuit card to be removed from card cage.

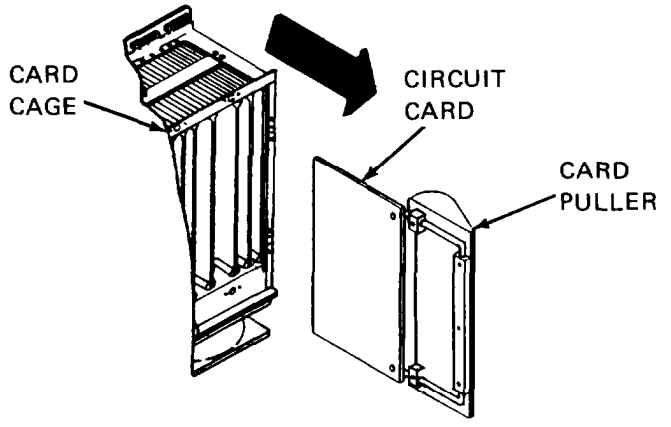


4

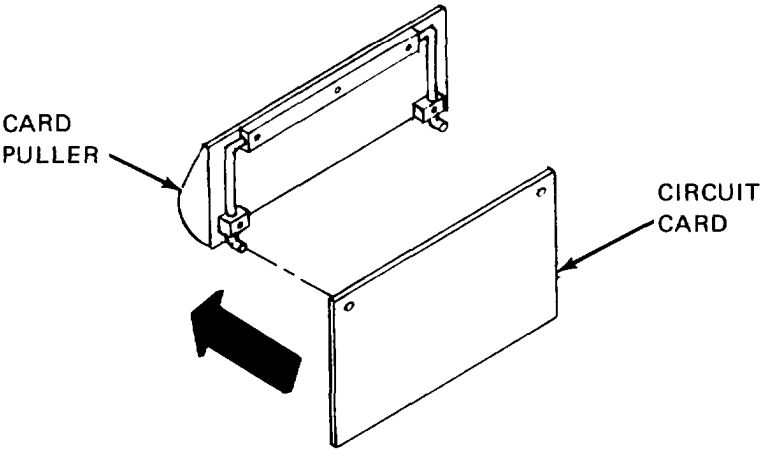
With flange of card puller resting on sides of card cage, push card puller sideways toward card puller flange until circuit card assembly is free of its mating connector.



5 Gently pull circuit card straight out of card cage.

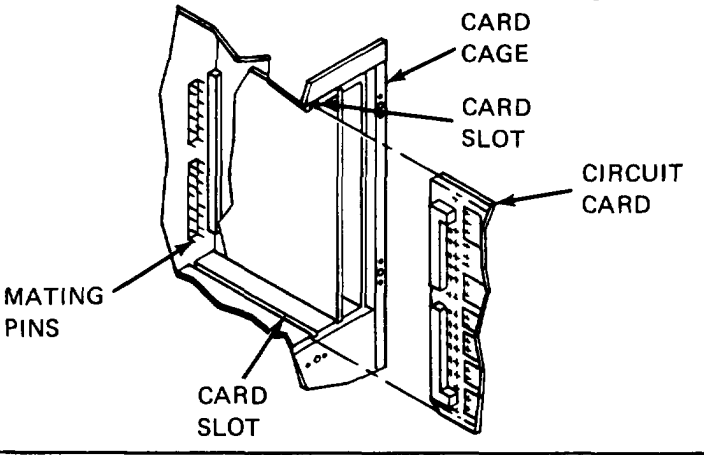


6 Separate the card puller from the removed circuit card.

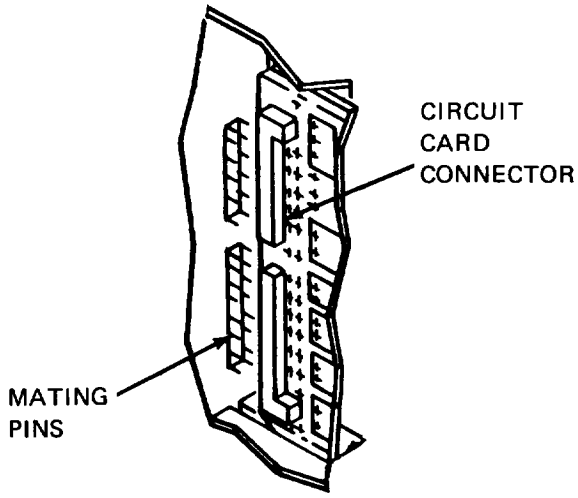


c. *Circuit Card Installation:*

1 With the circuit card components facing toward the front panel, position circuit card in the proper card slot and gently push the circuit card into the card cage until the circuit card assembly just touches the internal mating pins.



2 Maneuver circuit card for proper alignment between circuit card connector and internal mating pins. Then gently press circuit card into card cage.



3 Position the card cage cover over the card cage and secure with slotted screwdriver, using eight quarter-turn fasteners.

4 Perform the installation procedures provided in paragraph 4-39 c.

5 Perform the testing procedures provided in section IV of this chapter.

CARD CAGE REMOVAL AND INSTALLATION

4-41. This paragraph provides you with instructions for removal and installation of the card cage.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

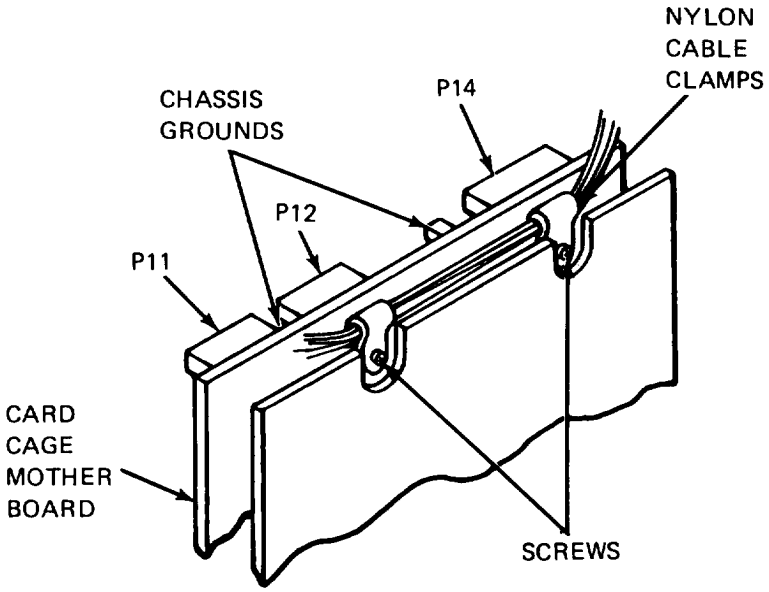
2 Card Cage

b. Card Cage Removal:

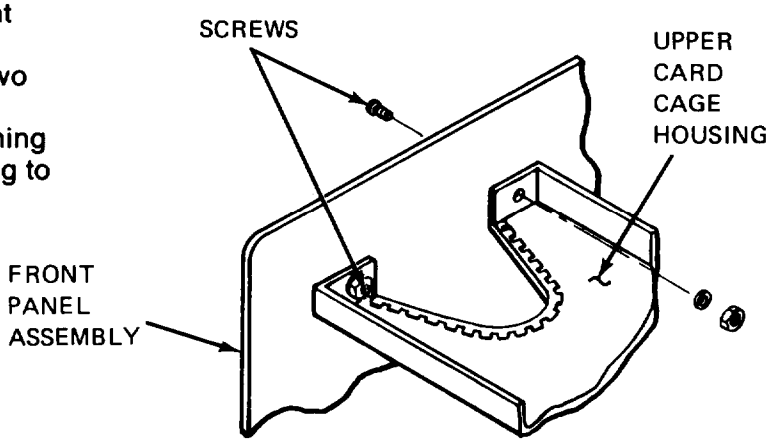
1 Perform the removal procedures of paragraphs 4-38 b, 4-39 b, 4-43 b, 4-44 b and 4-40 b.

2 Disconnect front panel cable harness connectors P11, P12, and P14, from card cage mother board, then disconnect two chassis grounds using offset phillips screwdriver.

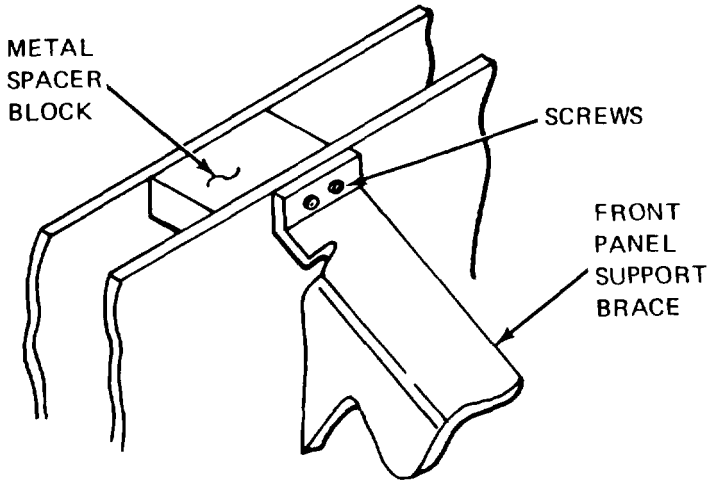
3 Remove two screws, lockwashers, and nylon cable clamps holding front panel cable harness to card cage.



4 Set front panel in upright position and brace to stabilize, then remove two flat head screws, nuts, and lockwashers, attaching upper card cage housing to front panel.

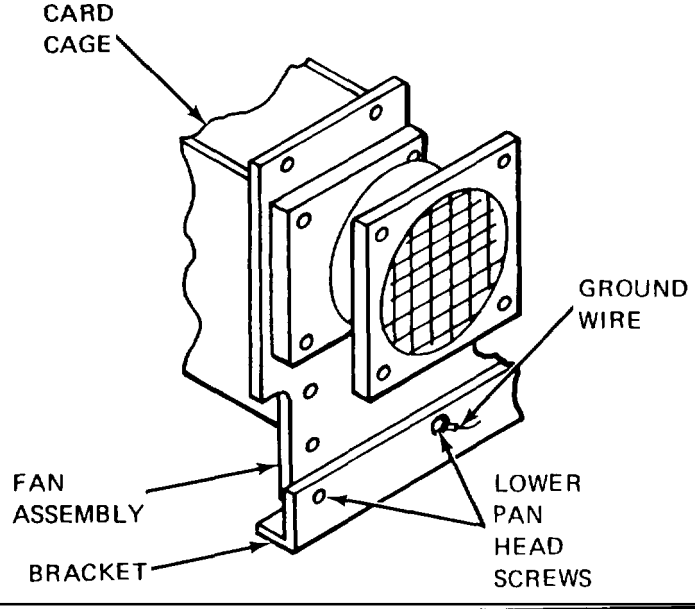


5 Remove two screws with nuts and lockwashers, and metal spacer block, fastening front panel support brace to rear of card cage.

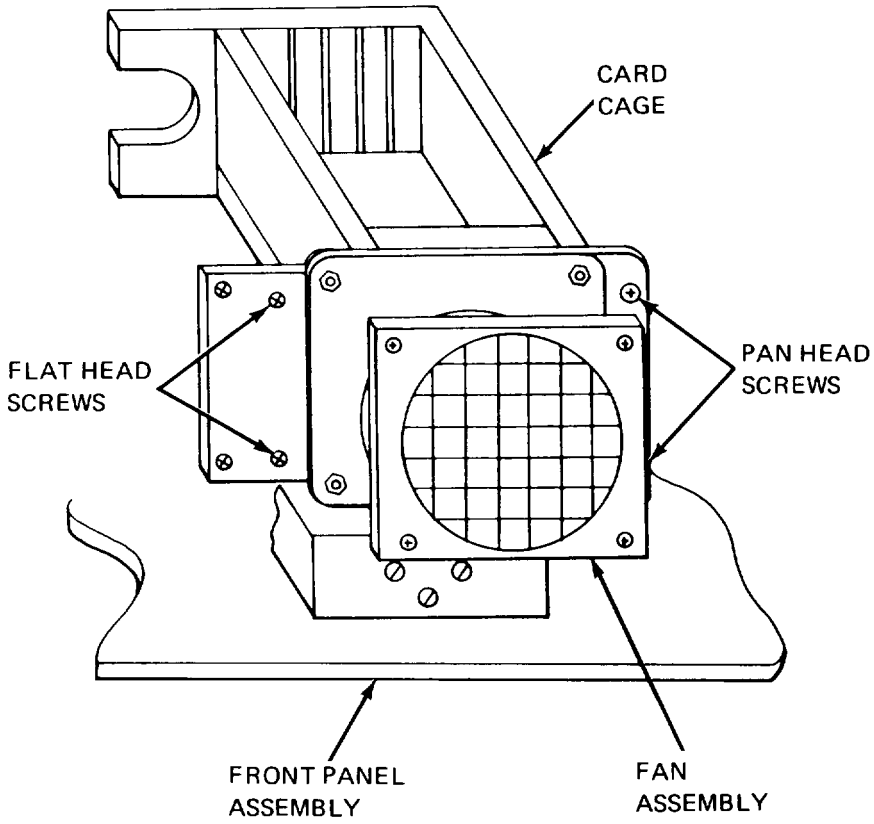


6 Disconnect front panel harness connectors PI thru P9 from card cage mother board

7 Remove two lower pan head screws, with nuts and lockwashers, fastening fan assembly to bracket.

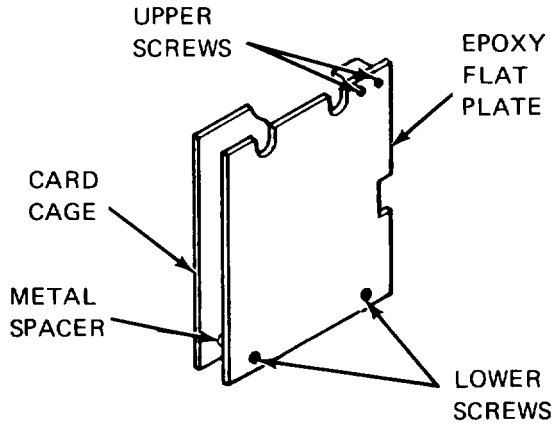


8 Carefully rotate card cage/fan assembly and place on top of power supply base.



9 Remove two pan head and two flat head screws fastening fan assembly to CARD CAGE.

10 Remove epoxy flat plate from card cage, as required, by removing upper and lower screws.



c. Card Cage Installation:

1. If epoxy flat plate was removed in step 10 of paragraph 4-41 b, reinstall using upper and lower screws.

2. Install fan assembly using four screws previously removed by step 9 of paragraph 4-41 b.

3. Carefully rotate card cage/fan assembly into position and insert connectors PI thru P9 into card cage mother board mating pins.

4. Install two lower pan head screws and ground wire, fastensing fan assembly to bracket, previously removed by step 7 of paragraph 4-41 b.

5. Install metal spacer block fastening front panel support brace to rear of card cage, using two screws with nuts and Iockwashers.

6. Fasten upper card cage housing to front panel, using two flat head screws, nuts, and Iockwashers.

7. Connect two chassis ground wires and nylon cable clamps previously removed by steps 2 and 3 of paragraph 4-41 b.

8. Connect front panel cable harness connectors P11, P12, and P14 to card cage mother board.

9. Perform the installation procedures of paragraphs 4-40 c, 4-44 c, 4-43 c, and 4-39 c,

10 Perform the testing procedures provided in section IV of this chapter.

11 Perform the installation procedures of paragraph 4-38 c, after successful completion of step 10.

MAGNETIC TAPE CASSETTE TRANSPORT (MTCT) REMOVAL AND INSTALLATION

4-42. This paragraph provides you with instructions for removal and installation of the MTCT.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

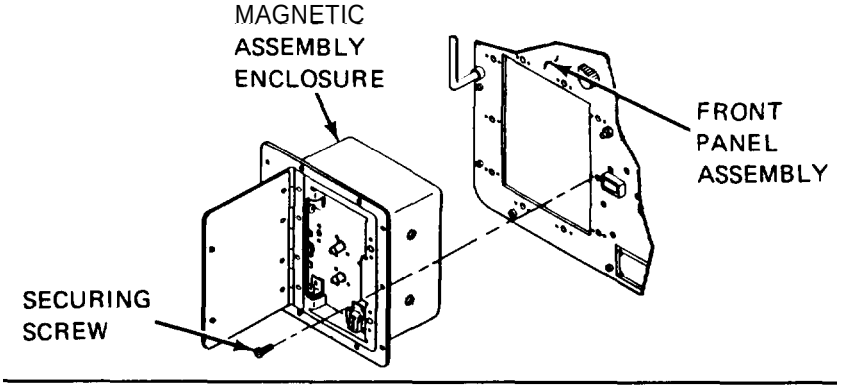
2 Magnetic Tape Cassette Transport (MTCT)

b. Magnetic Tape Cassette Transport Removal:

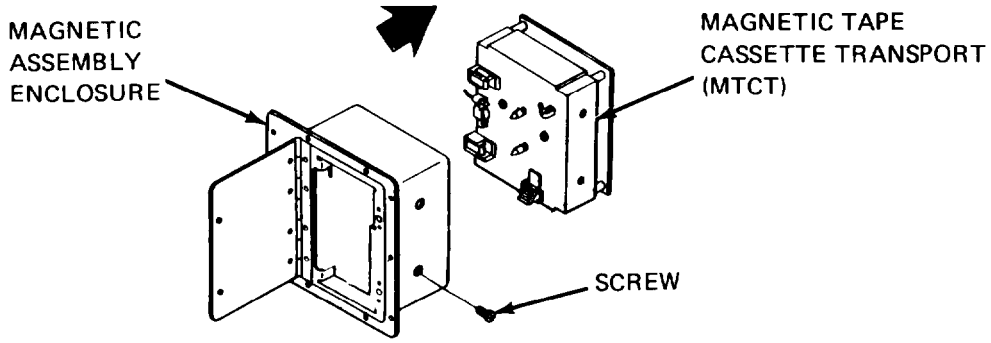
1 Perform the removal procedures of paragraphs 4-38 b and 4-39 b

2 Disconnect front panel assembly cable harness connector P16 from magnetic assembly enclosure.

3 Remove 10 screws securing magnetic assembly enclosure to front panel assembly and remove magnetic assembly enclosure.



4 Remove four screws securing MTCT to magnetic assembly enclosure.



c. Magnetic Tape Cassette Transport Installation:

1 Position the MTCT in the magnetic assembly enclosure and secure using four screws

2 Position the MTCT and magnetic assembly enclosure in the front panel assembly and secure using 10 securing screws.

3 Reconnect front panel assembly cable harness connector PI 6 to the magnetic assembly enclosure.

4 Perform the installation procedures provided in paragraph 4-39 c.

5 Perform the testing procedures provided in section IV of this chapter.

6. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 5.

RADAR SIGNAL INDICATOR UNIT A10 REMOVAL AND INSTALLATION

4-43. This paragraph provides you with instructions for removal and installation of the radar signal indicator.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

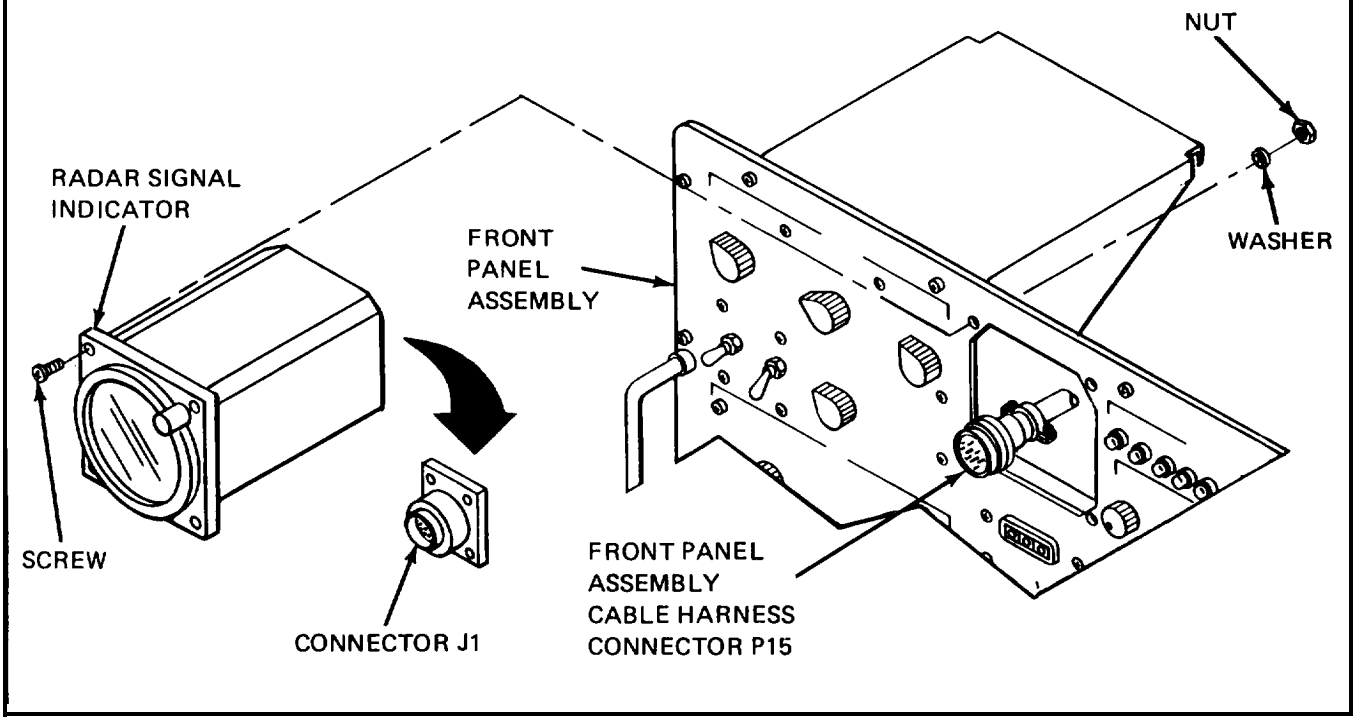
2 Radar Signal Indicator

b. Radar Signal Indicator Unit A10 Removal:

1 Perform the removal procedures of paragraphs 4-38 b and 4-39 b.

2 Disconnect front panel assembly cable harness connector P15 from the radar signal indicator connector J1.

3 Remove four screws and four lockwashers. Slide radar signal indicator out of front panel assembly.



c. Radar Signal Indicator Unit A10 Installation:

1. Position the radar signal indicator in the front panel assembly and secure using four screws and four washers.

2. Reconnect front panel assembly cable harness connector P15 to the radar signal

3. Perform the installation procedures provided in paragraph 4-39c.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 4.

POWER SUPPLY REMOVAL AND INSTALLATION

4-44. This paragraph provides you with instructions for removal and installation of the power supply.

a. Tools and Material:

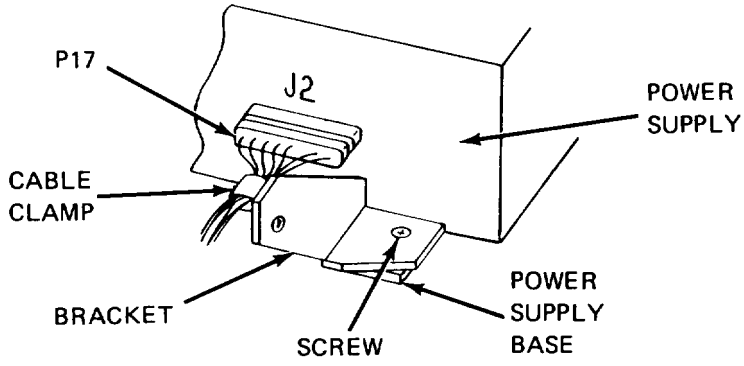
1. Tool Kit, Electronics Equipment TK-105/G
2. Power Supply

b. Power Supply Removal:

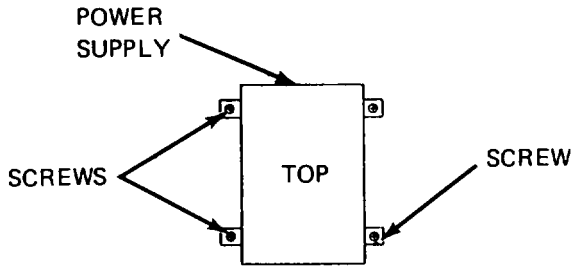
1. Perform the removal procedures of paragraphs 4-38 b and 4-39 b

2. Disconnect power cable connector P18 from the power supply connector J1.

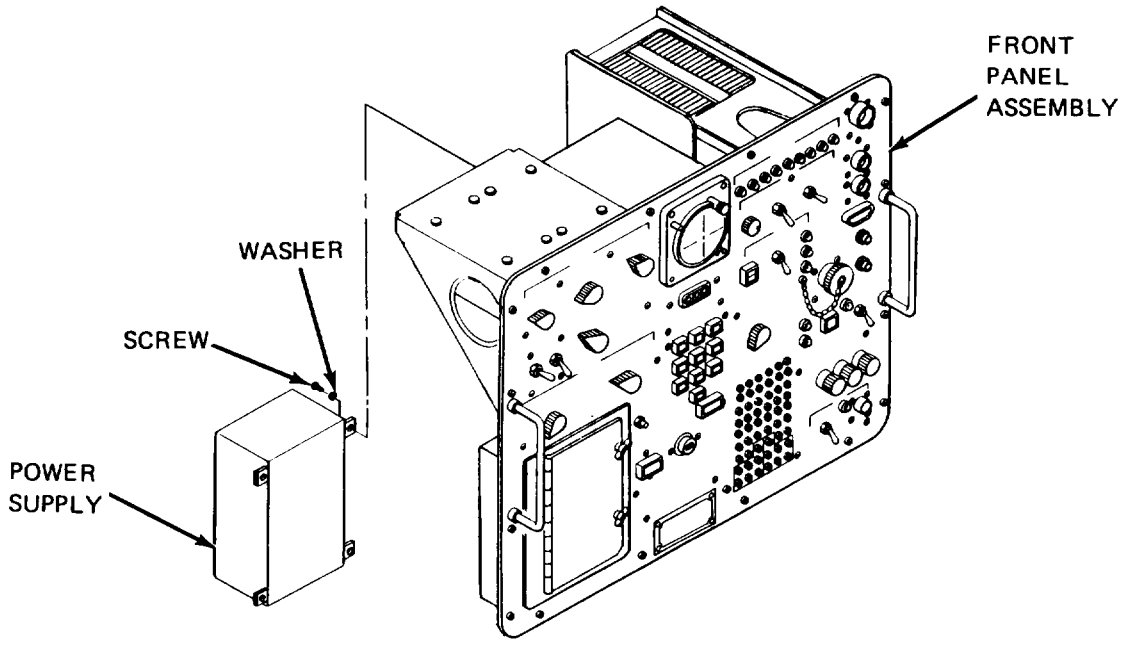
3 Remove screw fastening bracket to power supply base. Carefully disconnect connector plug P17 (plugged into J2) with cable clamp attached.



4 Remove remaining three screws and lockwashers.



5 Lift power supply free from front panel assembly.



c. Power Supply Installation:

1. Position the power supply on the front panel assembly and secure using four screws and four lockwashers.

2. Reconnect front panel assembly cable harness connector P17 and power cable connector P18 to the power supply.

3. Perform the installation procedures provided in paragraph 4-39 c.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 4.

RFI FILTER REMOVAL AND INSTALLATION

4-45. This paragraph provides you with instructions for removal and installation of the RFI filter.

a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. RFI Filter

b. RFI Filter Removal:

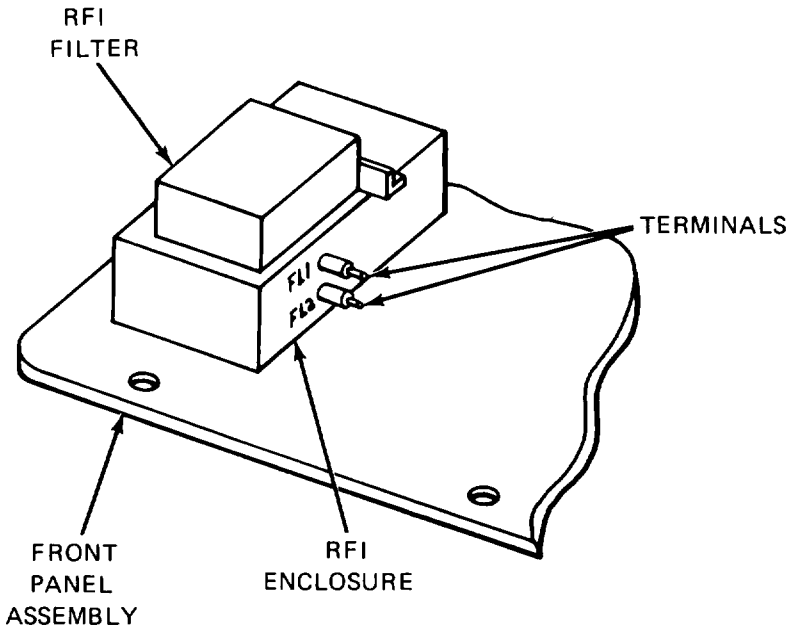
1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-43 b. 4-44 b. and 4-41 b. steps 1 thru 8 only.

CAUTION

Limit rated power of soldering iron used for terminals to a maximum of 37-1/2 watts.

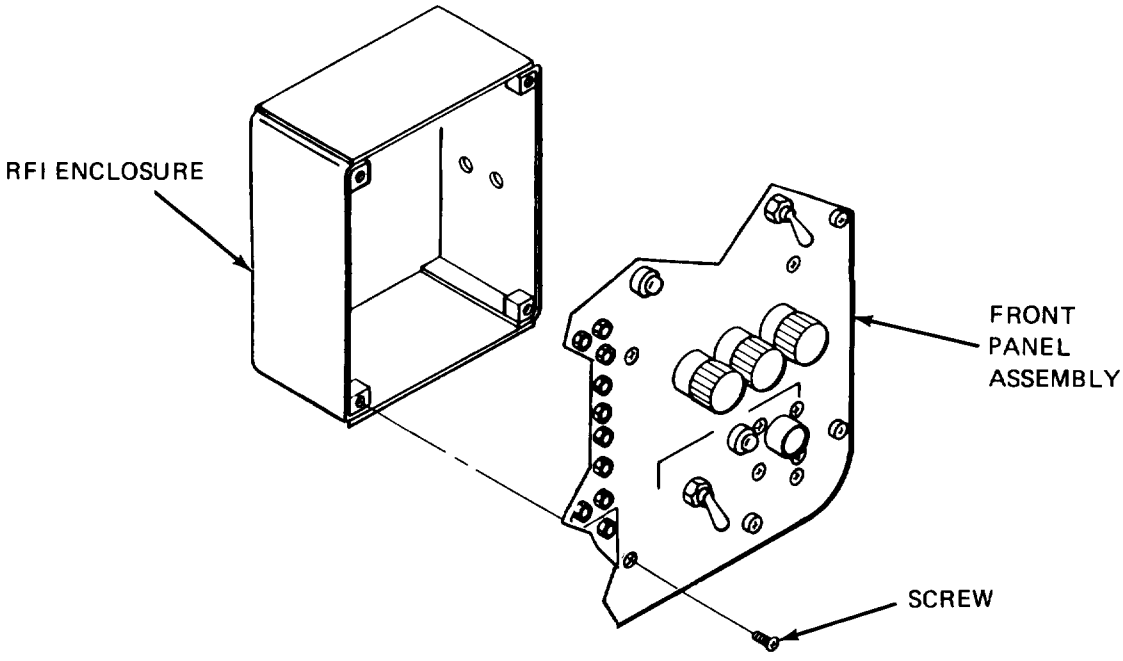
2

Tag and unsolder two wires to RFI enclosure terminals marked FL1 and FL2, as required.

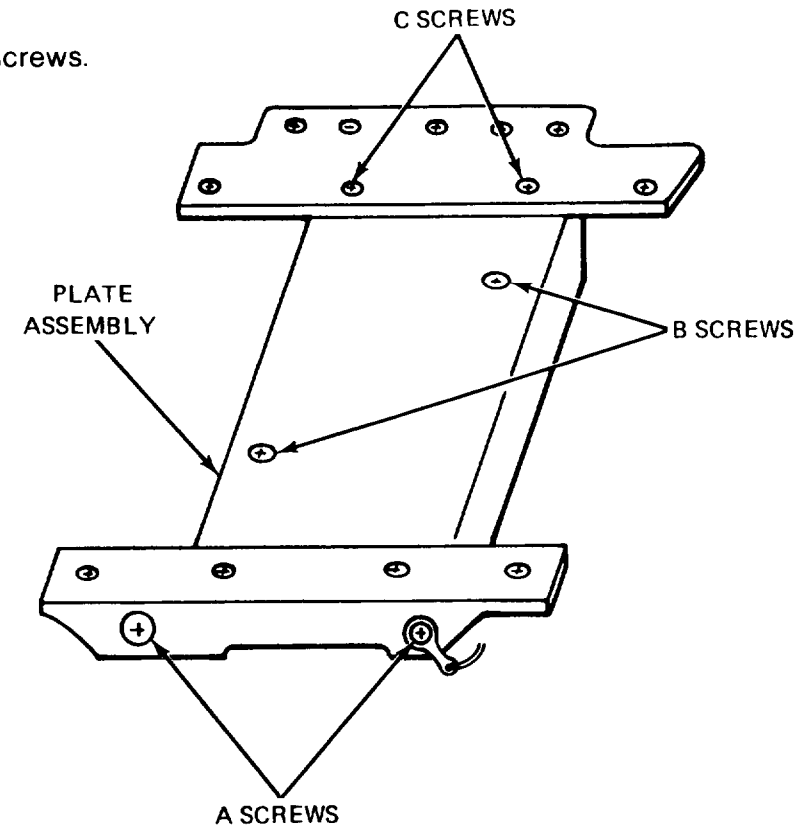


3

Remove four screws holding RFI enclosure to front panel assembly.



4 Remove two pan head A screws.

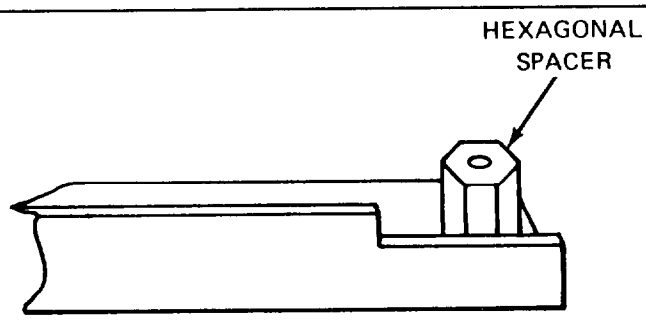


5 Remove two pan head B screws.

6 Remove two pan head C screws.

7 Remove plate assembly.

8 Remove hexagonal 1-inch spacer.



C A U T I O N

Limit rated power of soldering iron used for terminals to a maximum of 37-1/2 watts.

9 Unscrew four nuts and lockwashers fastening RFI enclosure to RFI filter.

10 Remove remaining screw attaching RFI enclosure to fan mounting plate.

C A U T I O N

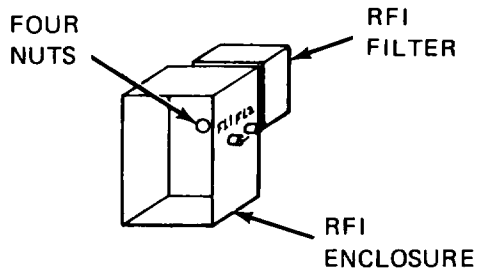
Limit rated power of soldering iron used for terminals to a maximum of 37-1/2 watts.

11 Tag and unsolder two wires to FL1 and FL2, inside terminals.

12 Tag and unsolder two remaining wires to terminals J and K on RFI filter, then remove RFI filter.

c. RFI Filter Installation:

1 Insert RFI filter into RFI enclosure and secure with four nuts and lockwashers.



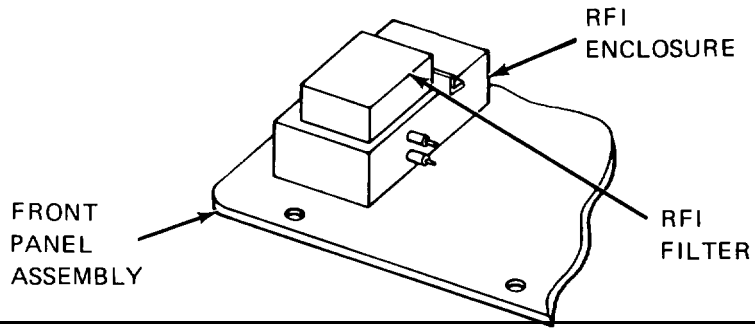
CAUTION

Limit rated power of soldering iron used for terminals to a maximum of 37-1/2 watts.

2 Solder two previously tagged wires going to terminals J and K on RFI filter and remove

3 Solder two wires going to FL1 and FL2 inside terminals and remove tags.

4 Maneuver RFI filter/enclosure assembly into position on front panel assembly.



5 Install four front panel screws into RFI enclosure.

CAUTION

Limit rated power of soldering iron used for terminals to a maximum of 37-1/2 watts.

6 Solder two wires to RFI enclosure terminals marked FL1 and FL2 and remove tags.

7 Install hexagonal 1-inch spacer removed by step 8 of paragraph 4-45 b.

8 Install plate assembly and screws removed by steps 4 through 7 of paragraph 4-45 b.

9 Perform the installation procedures of paragraphs 4-44 c and 4-39 c; respectively.

10 Perform the testing procedures provided in section IV of this chapter.

11 Perform the installation procedures of paragraph 4-38 c. after successful completion of

CHOKE ASSEMBLY REMOVAL AND INSTALLATION

4-46. This paragraph provides you with instructions for removal and installation of the choke assembly.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Choke Assembly

b. Choke Assembly Removal:

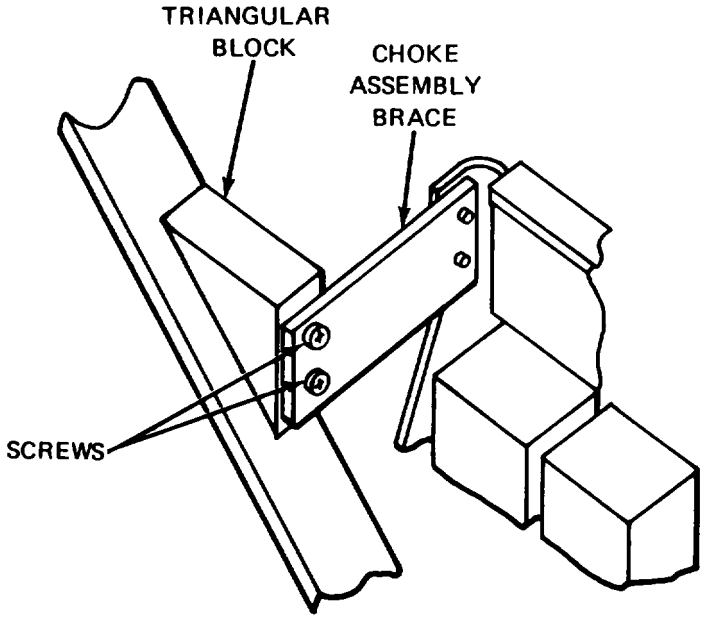
1 Perform the removal procedures of paragraph 4-38 b and 4-39 b.

CAUTION

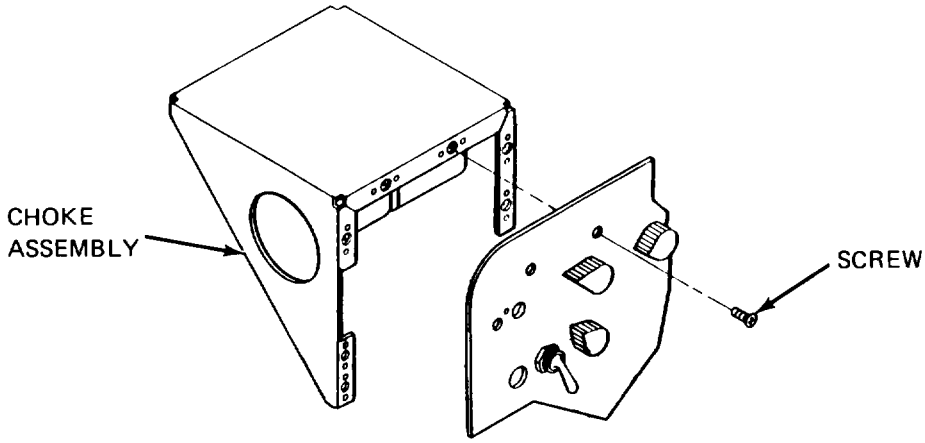
Limit rated power of soldering iron used for choke assembly to a maximum of 37-1/2 watts.

2 Tag and unsolder eight wires to choke assembly.

3 Remove two pan head screws fastening choke assembly brace to triangular block.



4 Remove seven screws and lift choke assembly free from front panel.



c. Choke Assemblv Installation

1 Position the choke assembly on the front panel assembly and secure using seven screws.

2 Install screws removed by step 3 of paragraph 4-46 b.

CAUTION

Limit rated power of soldering iron used for choke assembly to a maximum of 37-1/2 watts.

3 Solder eight wires, disconnected during removal procedure of paragraph 4-46 b. to choke

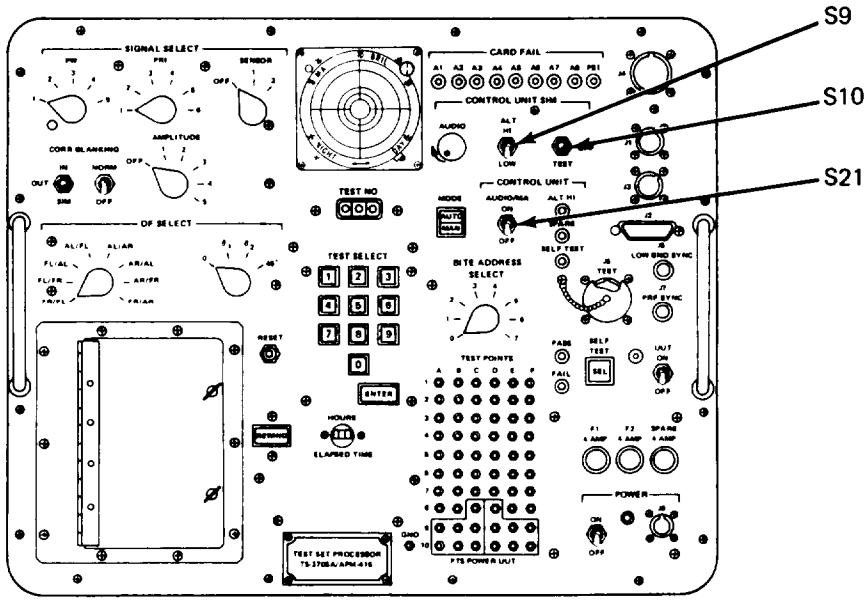
4 Perform the installation procedures provided in paragraph 4-39 c.

5 Perform the testing procedures provided in section IV of this chapter.

6 Perform the installation procedures of paragraph 4-38 c. after successful completion of

TOGGLE SWITCHES S9, S1O, AND S21 REMOVAL AND INSTALLATION

4-47. This paragraph provides you with instructions for removal and installation of toggle switches S9, S10, and S21.



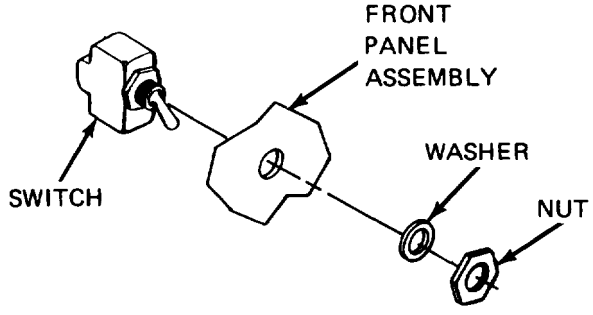
a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Toggle Switches S9 and S21
3. Toggle Switch S10

b. Toggle Switches S9, S10, and S21 Removal:

1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. and 4-43 b. respectively.

2. Turn nut counterclockwise until nut is free from switch. Remove washer. Carefully pull switch away from rear of front panel assembly until switch is free.



CAUTION

Limit rated power of soldering iron used for switch terminals to a maximum of 37-1/2 watts.

3 Position switch to allow unsoldering of terminals. Tag and unsolder all wires connected to the toggle switch.

c. Toggle Switches S9, S10, and S21 Installation:

CAUTION

Limit rated power of soldering iron used for switch terminals to a maximum of 37-1/2 watts.

1 Position switch at rear of front panel to allow soldering of terminals. Solder all wires disconnected during removal procedure of paragraph 4-47 b and remove tags.

2 Position the switch in the front panel assembly. Position the washer and nut on the switch until the nut contacts the threads. Turn nut clockwise until the switch is secured to the front panel assembly.

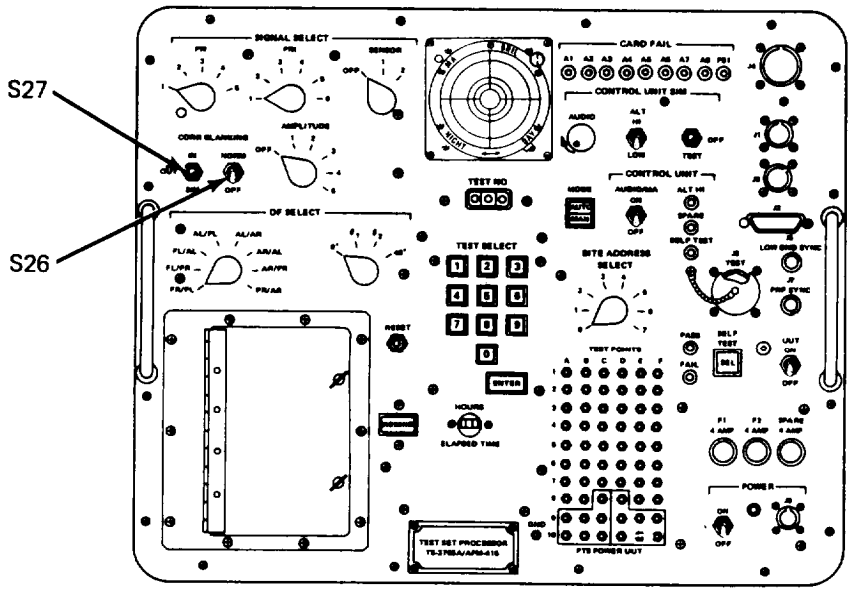
3 Perform the installation procedures provided in paragraph 4-43 c and 4-39 c.

4 Perform the testing procedures provided in section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38 c. after successful completion of

TOGGLE SWITCHES S26 and S27 REMOVAL AND INSTALLATION

4-48. This paragraph provides you with instructions for removal and installation of toggle switches S26 and S27.



a. Tools and Material:

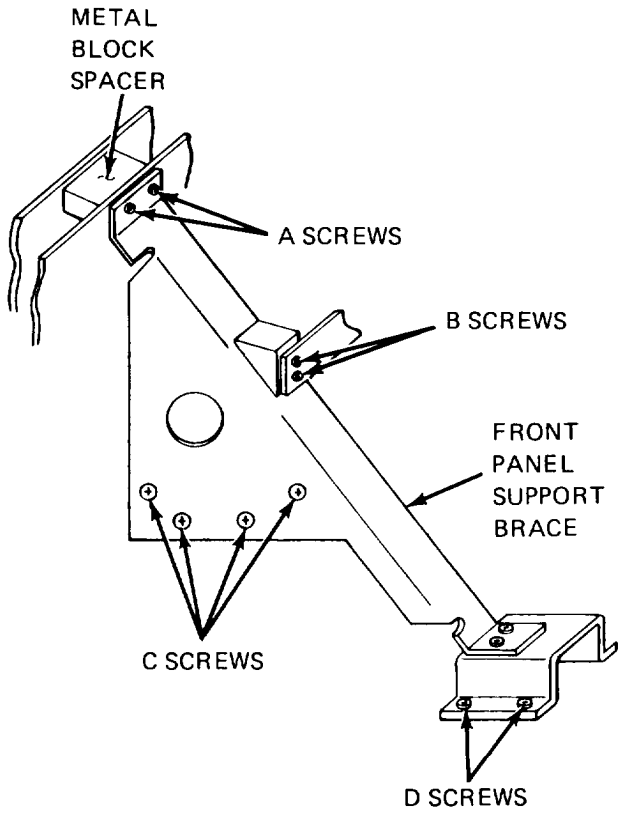
1. Tool Kit, Electronics Equipment TK-105/G
2. Toggle Switch S26
3. Toggle Switch S27

b. Toggle Switches S26 and S27 Removal:

1. Perform the removal procedures of paragraphs 4-38 b, 4-39 b 4-43 b, and 4-44 b, respectively.
2. Remove two pan head A screws and metal block spacer.
3. Remove two pan head B screws.
4. Remove four flathead C screws.

5 Remove four D screws.

6 Lift out front panel support brace.



CAUTION

Limit rated power of soldering iron used for switch terminals to a maximum of 37-1/2 watts.

7 Tag and unsolder all wires connected to the toggle switch.

8 Perform step 2 of paragraph 4-47 b.

c. Toggle Switches S26 and S27 Installation:

1. Perform step 2 of paragraph 4-47 c

CAUTION

Limit rated power of soldering iron used for switch terminals to a maximum of 37-1/2 watts.

2. Solder all wires disconnected during removal procedure of paragraph 4-48 b and remove

3. Maneuver front panel support brace into position and install A, B, C, and D screws removed by steps 2 through 5 of paragraph 4-48 b.

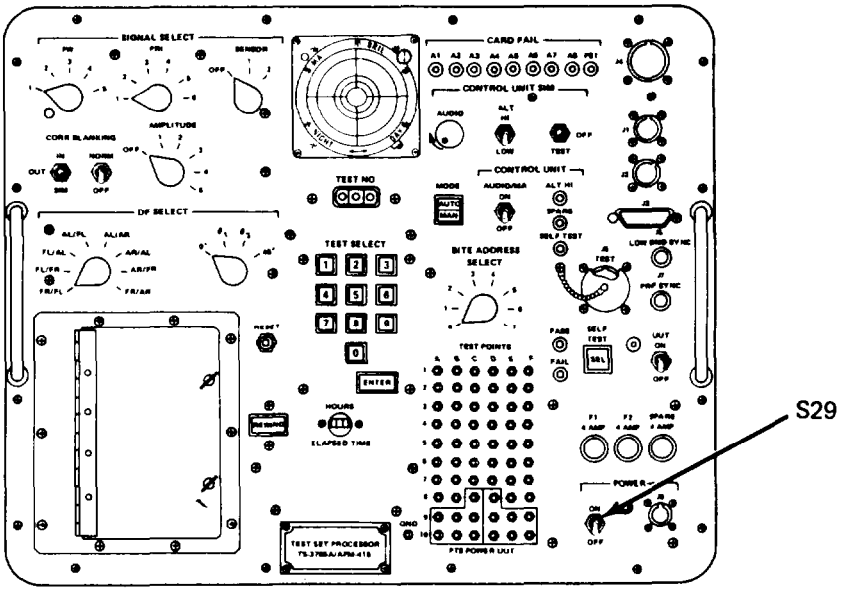
4. Perform the installation procedures provided in paragraphs 4-44 c, 4-43 c, and 4-39 c;

5. Perform the testing procedure provided in section IV of this chapter.

6. Perform the installation procedures of paragraph 4-38 c, after successful completion of step 5.

TOGGLE SWITCH S29 REMOVAL AND INSTALLATION

4-49. This paragraph provides you with instructions for removal and installation of toggle switch S29.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Toggle Switch S29

b. Toggle Switch S29 Removal:

1. Perform the removal procedures of paragraphs 4-38 b 4-39 b, 4-43 b, 4-44 b, 4-41 b, and 4-45 b, steps 3 through 8, respectively.

CAUTION

Limit rated power of soldering iron used for switch terminals to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires connected to toggle switch S29.

3. Perform step 2 of paragraph 4-47 b.

c. Toggle Switch S29 Installation:

1	Perform step 2 of paragraph 4-47 c.

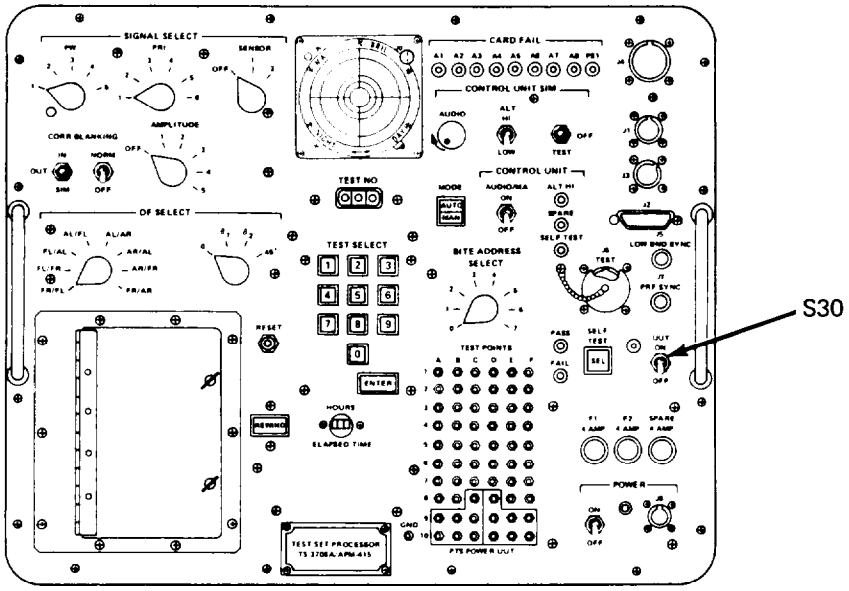
CAUTION

Limit rated power of soldering iron used for switch terminals to a maximum of 37-1/2 watts.

2	Solder all wires disconnected during removal procedure of paragraph 4-49 b and remove
3	Perform the installation procedure of paragraph 4-45 c, steps 4 through 9.
4	Perform the installation procedures provided in paragraphs 4-41 c, 4-44 c, and 4-39 c;
5	Perform the testing procedure provided in section IV of this chapter.
6	Perform the installation procedures of paragraph 4-38 c, after successful completion of

TOGGLE SWITCH S30 REMOVAL AND INSTALLATION

4-50. This paragraph provides you with instructions for removal and installation of toggle switch S30.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Toggle Switch S30

b. Toggle Switch S30 Removal:

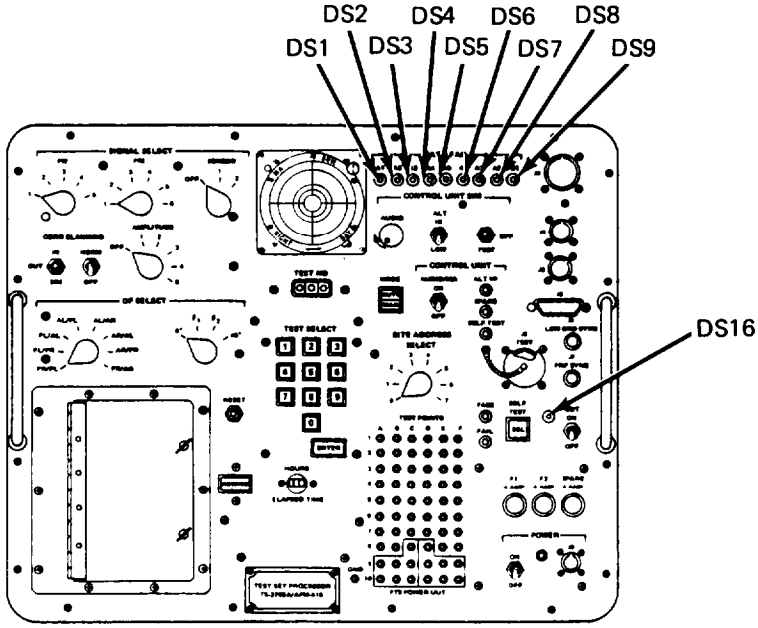
1. Perform the removal procedures of paragraphs 4-38 b and 4-39 b, respectively.
2. Perform step 2 of paragraph 4-47 b.
3. Tag and disconnect all wires connected to toggle switch S30.

c. Toggle Switch S30 Installation:

1. Reconnect wires disconnected during removal procedure of paragraph 4-50 b.
2. Perform step 2 of paragraph 4-47 c.
3. Perform the installation procedure of paragraph 4-39 c.
4. Perform the testing procedure provided in section IV of this chapter.
5. Perform the installation procedures of paragraph 4-38 c. after successful completion of

INDICATOR LAMPS DS1 THRU DS9 AND DS16 REMOVAL AND INSTALLATION

4-51. This paragraph provides you with instructions for removal and installation of indicator lamps DS1 thru DS9 and DS16.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. indicator Lamps DS1 thru DS9
3. Indicator Lamp DS16

b. Indicator Lamps DS1 thru DS9 and DS16 Removal:

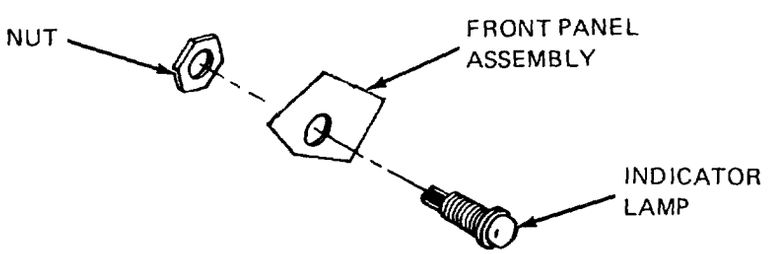
1. Perform the removal procedures of paragraphs 4-38 b and 4-39 b, respectively.

CAUTION

Limit rated power of soldering iron used for indicator lamps to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires connected to indicator lamp,

3. Turn nut counterclockwise until nut is free from indicator lamp. Pull indicator lamp forward from front of front panel assembly until indicator lamp is free.



c. Indicator Lamps DS1 thru DS9, and DS16 Installation:

1. Position indicator lamp in front panel assembly. Position nut on indicator lamp until it contacts the threads. Turn nut clockwise until the indicator lamp is secured to the front panel assembly.

CAUTION

Limit rated power of soldering iron used for indicator lamps to a maximum of 37-1/2 watts.

2 Solder all wires disconnected during removal procedure of paragraph 4-51 b and remove

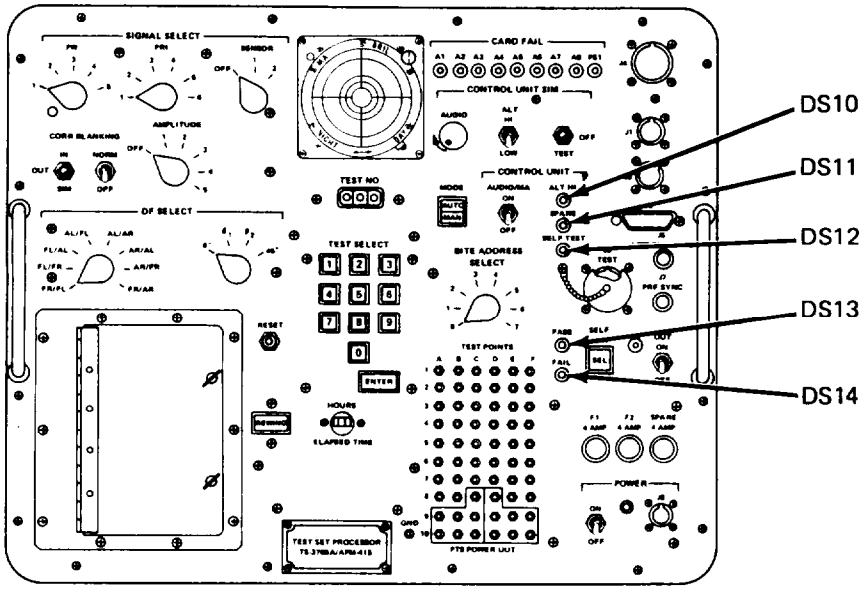
3 Perform the installation procedures provided in paragraph 4-39 c.

4 Perform the testing procedures provided in section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38 c, after successful completion of step

INDICATOR LAMPS DS10 THRU DS14 REMOVAL AND INSTALLATION

4-52. This paragraph provides you with instructions for removal and installation of indicator lamps DS10 thru DS14.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Indicator Lamps DS10 thru DS13

3 Indicator Lamp DS14

b. Indicator Lamps DS10 thru DS14 Removal:

1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-43 b. 4-44 b. and 4-41 b. respectively.

CAUTION

Limit rated power of soldering iron used for indicator lamps to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires connected to indicator lamp.

3. Perform step 3 of paragraph 4-51 b.

c. Indicator Lamps DS10 thru DS14 Installation:

1. Perform step 1 of paragraph 4-51 c.

CAUTION

Limit rated power of soldering iron used for indicator lamps to a maximum of 37-1/2 watts.

2. Solder all wires disconnected during removal procedures of paragraph

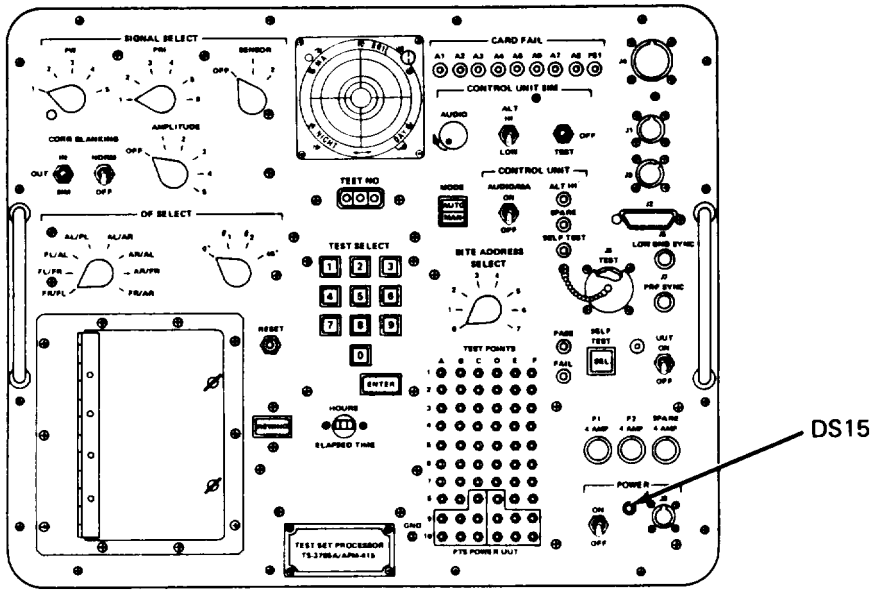
3. Perform installation procedures provided in paragraphs 4-41 c. 4-44 c. 4-43 c.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 4.

INDICATOR LAMP DS15 REMOVAL AND INSTALLATION

4-53. This paragraph provides you with instructions for removal and installation of indicator lamp DS15.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Indicator Lamp DS15

b. Indicator Lamp DS15 Removal:

1 Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-43 b. 4-44 b. 4-41 b. and 4-45 b. steps 3 through 8, respectively.

CAUTION

Limit rated power of soldering iron used for indicator lamps to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires connected to indicator lamp DS15.

3 Perform step 3 of paragraph 4-51 b.

c. Indicator Lamp DS15 Installation:

1. Perform step 1 of paragraph 4-51 c.

CAUTION

Limit rated power of soldering iron used for indicator lamps to a maximum of 37-1/2 watts.

2. Solder all wiires disconnected during removal procedures of paragraph 4-53 b and remove tags.

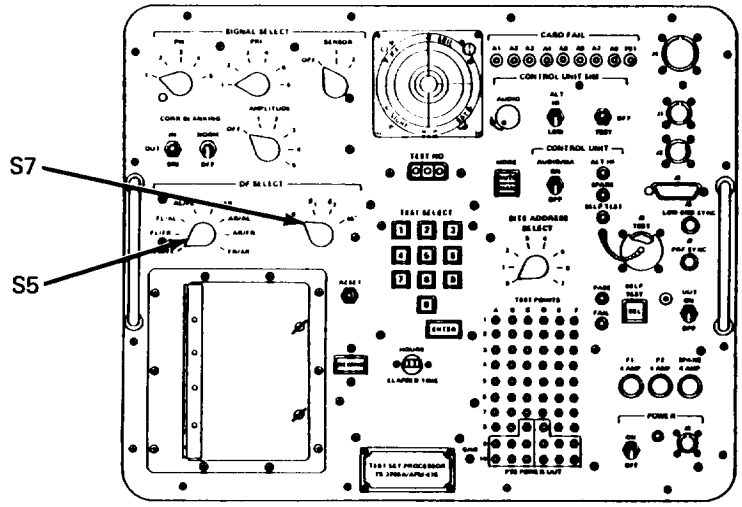
3. Perform installation procedures provided in paragraphs 4-45 c, steps 4 through 9, 4-41 c, 4-44 c, 4-43 c and 4-39 c, respectively.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 4.

ROTARY SWITCHES S5 AND S7 REMOVAL AND INSTALLATION

4-54. This paragraph provides you with instructions for removal and installation of rotary switches S5 and S7.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Rotary Switch S5
3. Rotary Switch S7

b. Rotary Switches S5 and S7 Removal:

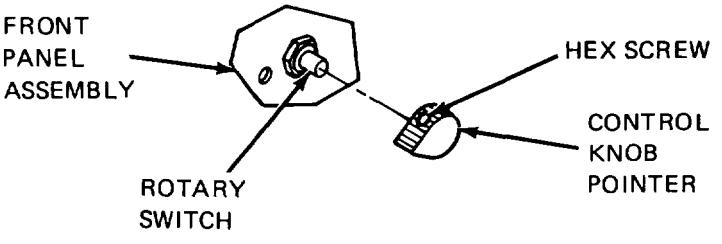
1. Perform the removal procedures of paragraphs 4-38 b, 4-39 b, and 4-42 b, steps 2 and 3, respectively.

CAUTION

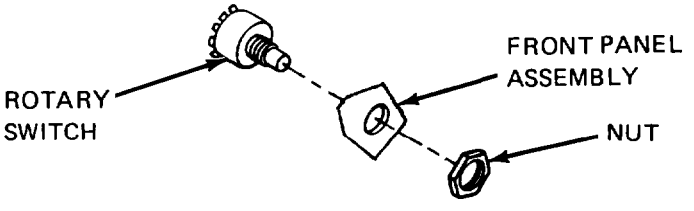
Limit rated power of soldering iron used for rotary switches to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires connected to rotary switch.

3. Loosen hex screw by turning hex screw counterclockwise. Remove switch control knob pointer from rotary switch.



4. Turn nut counterclockwise until nut is free from rotary switch. Pull rotary switch backward from rear of front panel assembly until rotary switch is free.



c. Rotary Switches S5 and S7 Installation:

1. Position rotary switch in front panel assembly. Position nut on rotary switch until it contacts the threads. Turn nut clockwise until the switch is secured to the front panel assembly.

2. Position control knob pointer on switch and secure using hex screw.

CAUTION

Limit rated power of soldering iron used for rotary switches to a maximum of 37-1/2 watts.

3. Solder all wires disconnected during removal procedures of paragraph 4-54 b and remove tags.

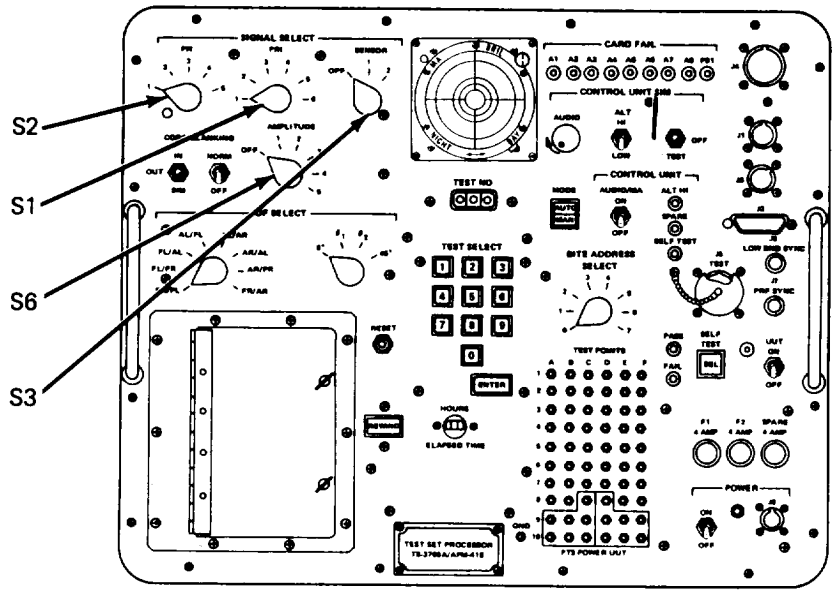
4. Perform the installation procedures provided in paragraphs 4-42 b, steps 2 and 3, and 4-39 c.

5. Perform the testing procedures provided in section IV of this chapter.

6. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 5.

ROTARY SWITCHES S1 THRU S3 AND S6 REMOVAL AND INSTALLATION

4-55. This paragraph provides you with instructions for removal and installation of rotary switches S1 thru S3 and S6.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Rotary Switches S1 and S6
3. Rotary Switch S2
4. Rotary Switch S3

b. Rotary Switches S1 thru S3 and S6 Removal:

1. Perform the removal procedures of paragraphs 4-38 b, 4-39 b, and 4-46 b, respectively.

CAUTION

Limit rated power of soldering iron used for rotary switches to a maximum of 37-1/2 watts.

2. perform the removal procedures provided in steps 2 through 4 of paragraph 4-54 b.

c. Rotary Switches S1 thru S3 and S6 Installation:

1. Perform the installation procedures of steps 1 through 3 of paragraph 4-54 c.

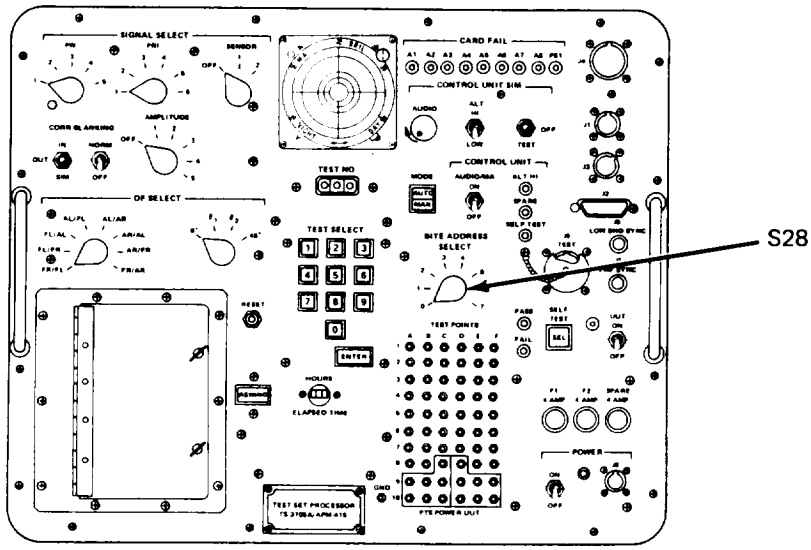
2. Perform the installation procedures provided in paragraphs 4-46 c and 4-39 c.

3. Perform the testing procedures provided in section IV of this chapter.

4. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 3.

ROTARY SWITCH S28 REMOVAL AND INSTALLATION

4-56. This paragraph provides you with instructions for removal and installation of rotary switch S28,



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Rotary Switch S28

b. Rotary Switch S28 removal

1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. and 4-44 b. respectively.

CAUTION

Limit rated power of soldering iron used for rotary switches to a maximum of 37-1/2 watts.

2. Perform the removal procedures provided in steps 2 through 4 of paragraph 4-54 b.

c. Rotary Switch S28 Installation:

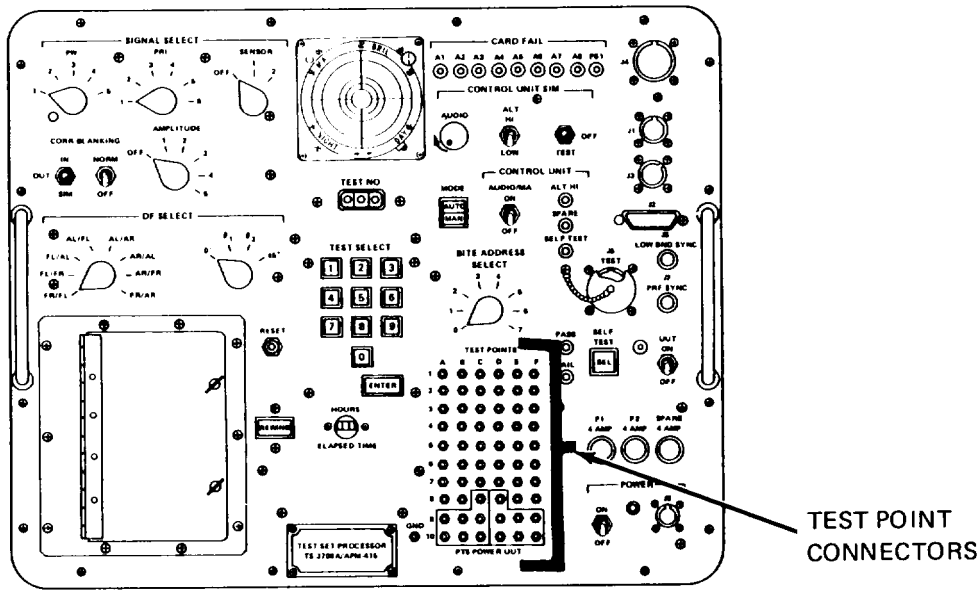
1. Perform the installation procedures of steps 1 through 3 of paragraph 4-54 c.

2. Perform the installation procedures provided in paragraphs 4-44 c and 4-39 c.

3. Perform the testing procedures provided in section IV of this chapter.

4. Perform the installation procedures of paragraph 4-38 c. after successful completion of step 3.

4-57. This paragraph provides you with instructions for removal and installation of test point connectors.



a. Tools and Material:

1. Tool Kit, Electronic Equipment TK-105/G
2. Black Test Point Connector
3. White Test Point Connector
4. Blue Test Point Connector

b. Test Point Connector Removal:

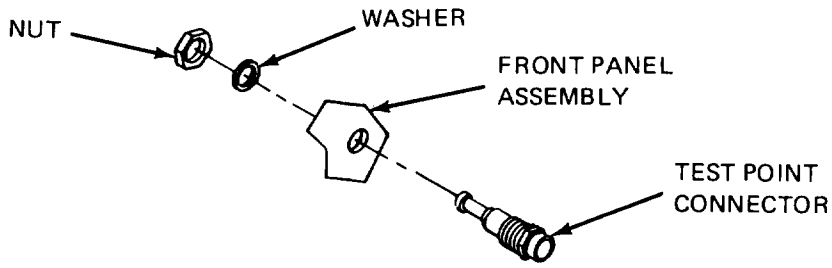
1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-44 b. and 4-45 b. steps 4 through 7, respectively.

CAUTION

Limit rated power of soldering iron used for test point connectors to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires connected to test point connector.

3 Turn nut counterclockwise until nut is free from test point connector. Pull test point connector forward from front of front panel assembly until test point connector is free.



c. Test Point Connector Installation:

1 Position test point connector in front panel assembly. Position washer and nut on test point connector until the nut contacts the threads. Turn nut clockwise until the test point connector is secured to the front panel assembly.

CAUTION

Limit rated power of soldering iron used for test point connectors to a maximum of 37-1/2 watts.

2 Solder all wires disconnected during removal procedures of paragraph 4-57 b and remove tags.

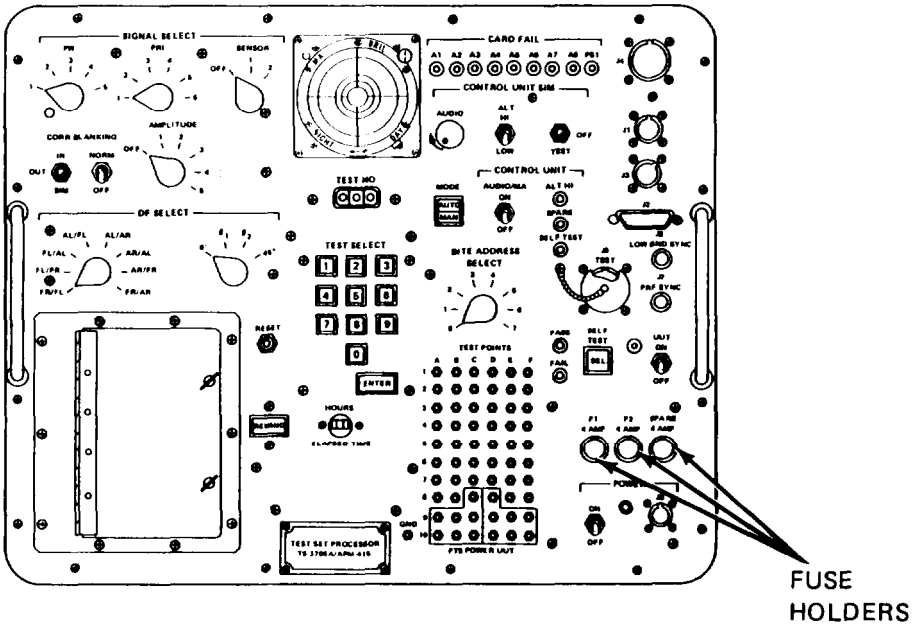
3 Perform the installation procedures provided in paragraphs 4-45 b, step 9, 4-44 c, and 4-39 c, respectively.

4 Perform the test procedures provided in section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38 c, after successful completion of step 4.

FUSE HOLDER REMOVAL AND INSTALLATION

4-58. This paragraph provides you with instructions for removal and installation of fuse holders.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Fuse Holder

b. Fuse Holder Removal:

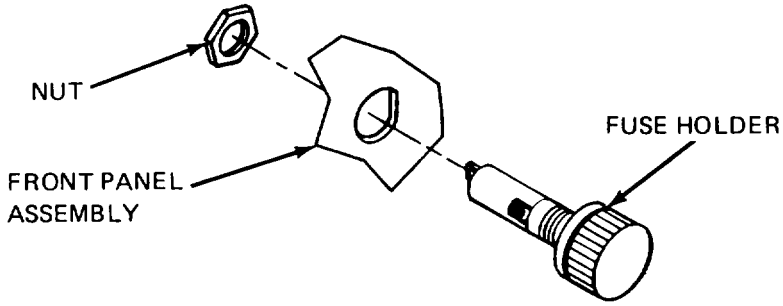
1 Perform the removal procedures of paragraphs 4-38 b 4-39 b. 4-43 b. 4-44 b. 4-41 b. and 4-45 b. steps 3 through 10, respectively.

CAUTION

Limit rated power of soldering iron used for fuse holders to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires connected to fuse holder.

3 Turn nut counterclockwise until nut is free from fuse holder. Pull fuse holder forward from front of front panel assembly until free.



c. Fuse Holder Installation:

1 Position fuse holder in front panel assembly. Position nut over fuse holder and turn nut clockwise until fuse holder is secured to the front panel assembly.

CAUTION

Limit rated power of soldering iron used for fuse holders to a maximum of 37-1/2 watts.

2 Solder all wires disconnected during removal procedures of paragraph 4-58 b and remove tags.

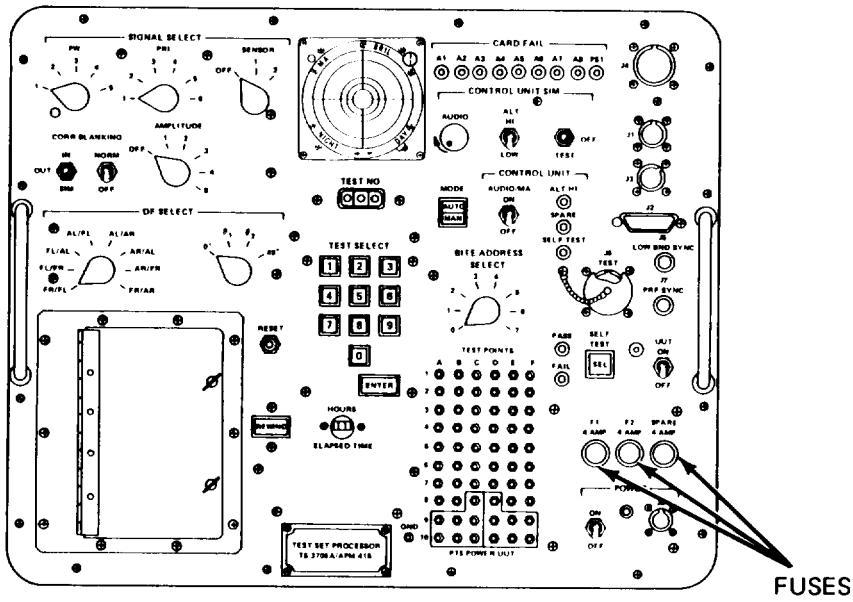
3 Perform the installation procedures provided in paragraphs 4-45 c, steps 4 through 9, 4-41 c, 4-44 c, 4-43 c, and 4-39 c, respectively.

4 Perform the testing procedures provided in section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38 c, after successful completion of step 4.

FUSE REMOVAL AND INSTALLATION

4-59. This paragraph provides you with instructions for removal and installation of fuses.



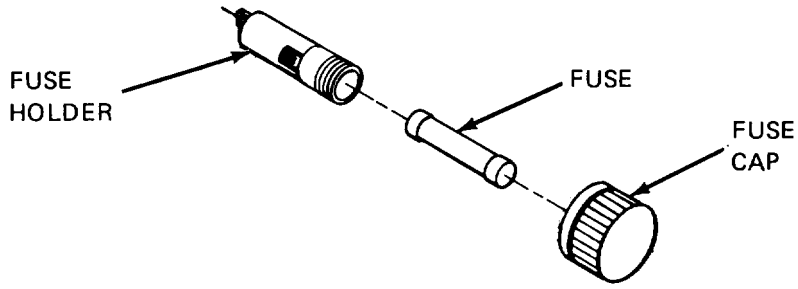
a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Fuse

b. Fuse Removal:

1. Set PTS main POWER switch to OFF.

2. Unscrew fuse cap from fuse holder. Pull fuse free from fuse holder.

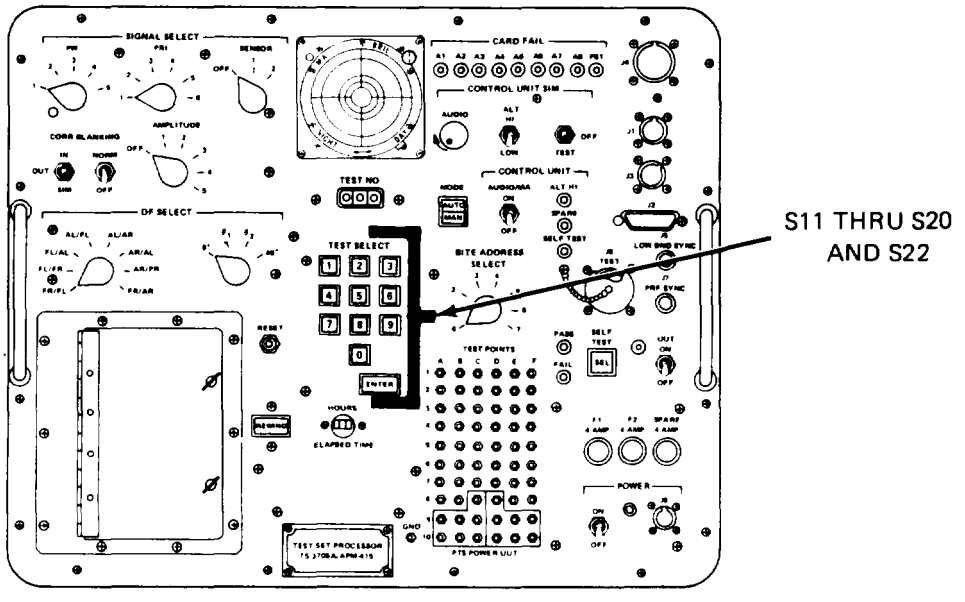


c. Fuse Installation:

1	Set PTS main POWER switch to OFF.
2	Position fuse in fuse holder.
3	Screw fuse cap clockwise onto fuse holder.
4	Perform the testing procedures provided in section IV of this chapter.
5	Perform the installation procedures of paragraph 4-38 c. after successful completion of step 4.

PUSHBUTTON SWITCHES S11 THRU S20 AND S22 REMOVAL AND INSTALLATION

4-60. This paragraph provides you with instructions for removal and installation of pushbutton switches S11 thru S20, and S22.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Pushbutton Switches S11 thru S20 and S22

b. Pushbutton Switches S11 thru S20 and S22 Removal:

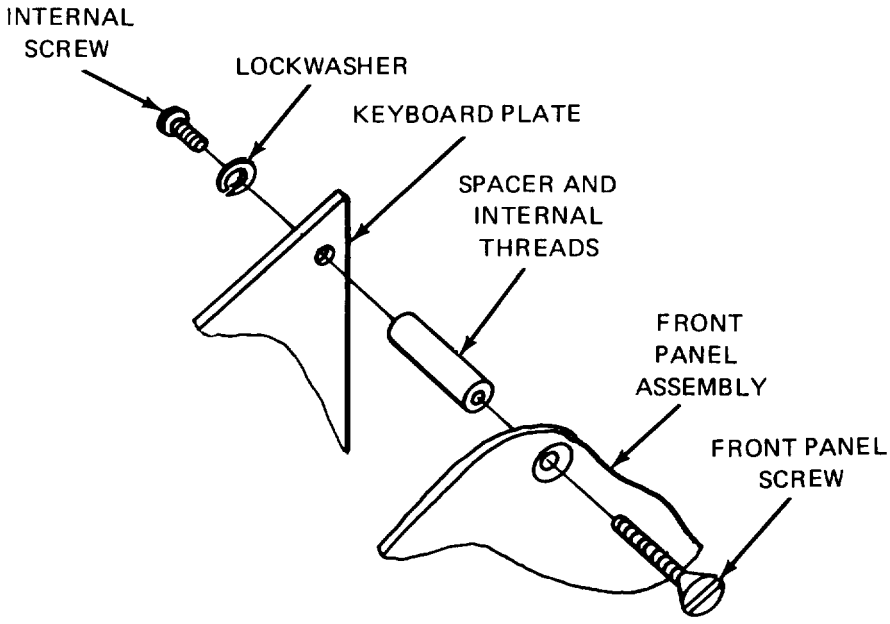
1 Perform the removal procedures of paragraphs 4-38 b, 4-39 b, 4-44 b, and 4-45 b, steps 4 through 7, respectively.

CAUTION

Limit rated power of soldering iron used for pushbutton switches to a maximum of 37-1/2 watts.

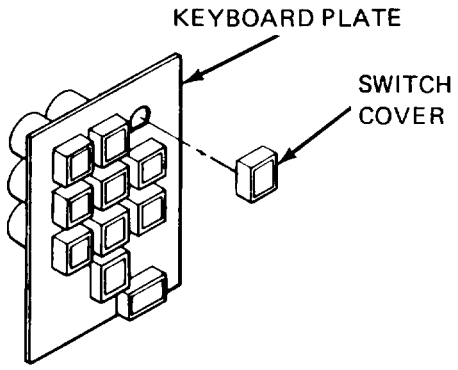
2 Tag and unsolder all wires connected to pushbutton switch.

3 Remove four internal screws and four lockwashers securing keyboard plate to threaded spacer. Pull keyboard plate from spacer and swing toward wiring side, taking care not to damage existing wiring.



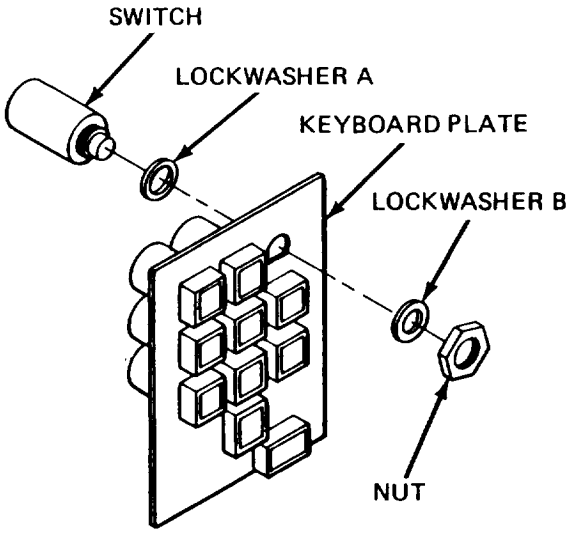
4

Grasp switch cover firmly between your fingers and snap switch cover out from keyboard plate.



5

Turn nut counterclockwise until nut is free from switch. Remove lockwasher B. Pull switch backward from rear of keyboard plate until free. Remove lockwasher A.



c. Pushbutton Switches S11 thru S20 and S22 Installation:

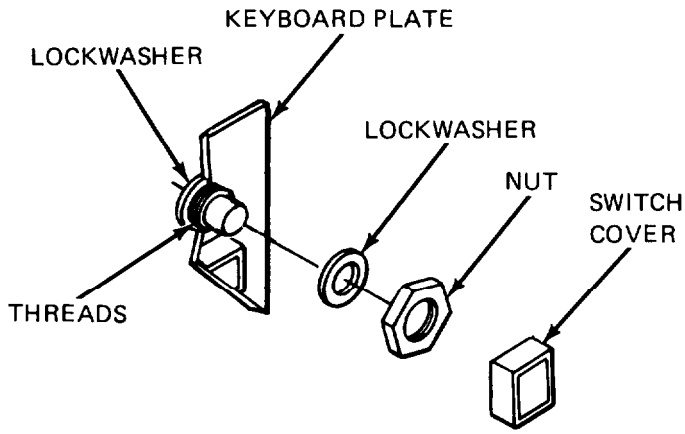
1

Position lockwasher A on switch. Position switch in keyboard plate. Position lockwasher B and nut over switch until it contacts threads. Turn nut clockwise until switch is secured to keypad.

2

Press switch cover into place on switch.

3 Position keyboard plate with four holes aligned with four internally threaded spacers. Secure with four internal screws and lockwashers.



CAUTION

Limit rated power of soldering iron used for terminals to a maximum of 37-1/2 watts.

4 Solder all wires disconnected during removal procedures of paragraph 4-60 b, and remove tags.

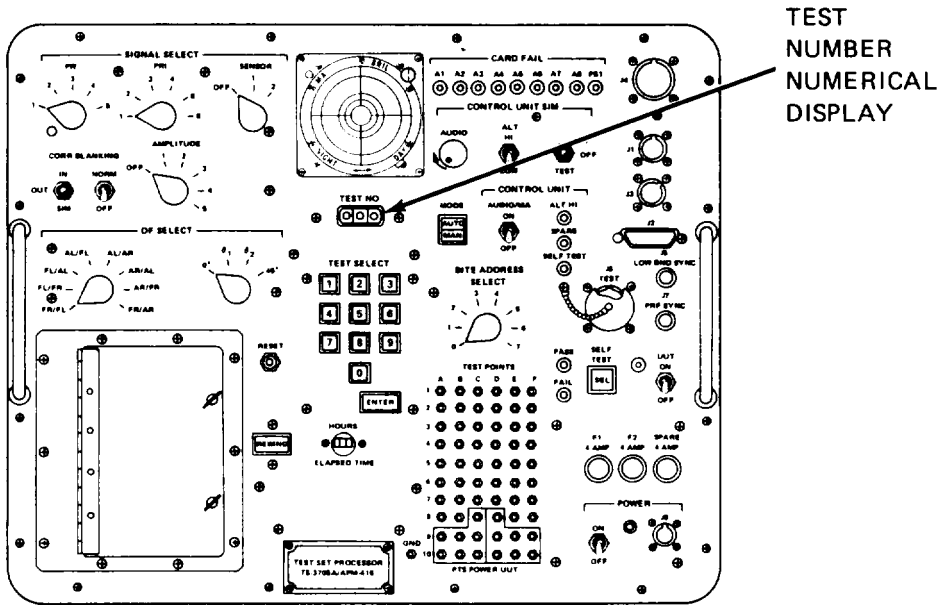
5 Perform the installation procedures provided in paragraphs 4-45 c, step 9, 4-44 c, and 4-39 c, respectively.

6 Perform the testing procedures provided in section IV of this chapter.

7 Perform the installation procedures of paragraph 4-38 c, after successful completion of step 6.

TEST NUMBER NUMERICAL DISPLAY A13 REMOVAL AND INSTALLATION

4-61. This paragraph provides you with instructions for removal and installation of the test number numerical display.



a. Tools and Material:

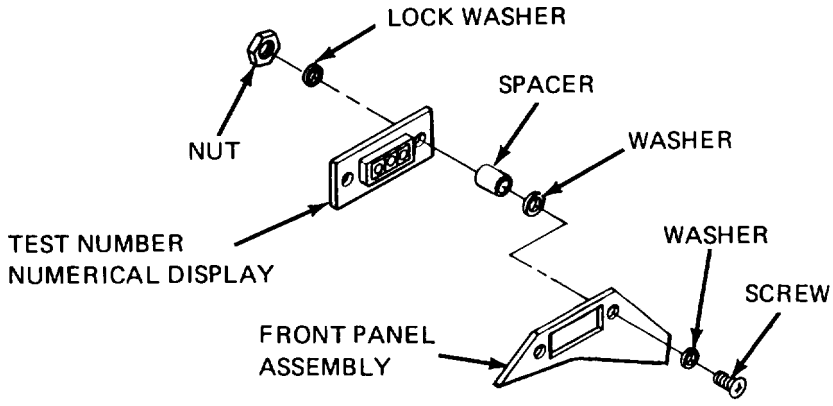
1 Tool Kit, Electronics Equipment TK-105/G

2 Test Number Numerical Display

b. Test Number Numerical Display removal:

1 Perform the removal procedures of paragraphs 4-38 b, 4-39 b, and 4-43 b, respectively.

2 Remove two nuts, two lockwashers, two screws, two washers, two spacers, and two washers. Lift test number display free from rear of front panel assembly.



CAUTION

Limit rated power of soldering iron used for numerical display to a maximum of 37-1/2 watts.

3 Tag all wires to numerical display circuit card and position to allow for unsoldering. Unsolder all wires to numerical display circuit card.

c. Test Number Numerical Displav A13 Installation:

CAUTION

Limit rated power of soldering iron used for numerical display to a maximum of 37-1/2 watts.

1 Solder all wires disconnected during removal procedures of paragraph 4-61 b. and remove tags.

2 Position the test number numerical display in the front panel assembly and secure using two screws, two washers, two spacers, two nuts and two lockwashers.

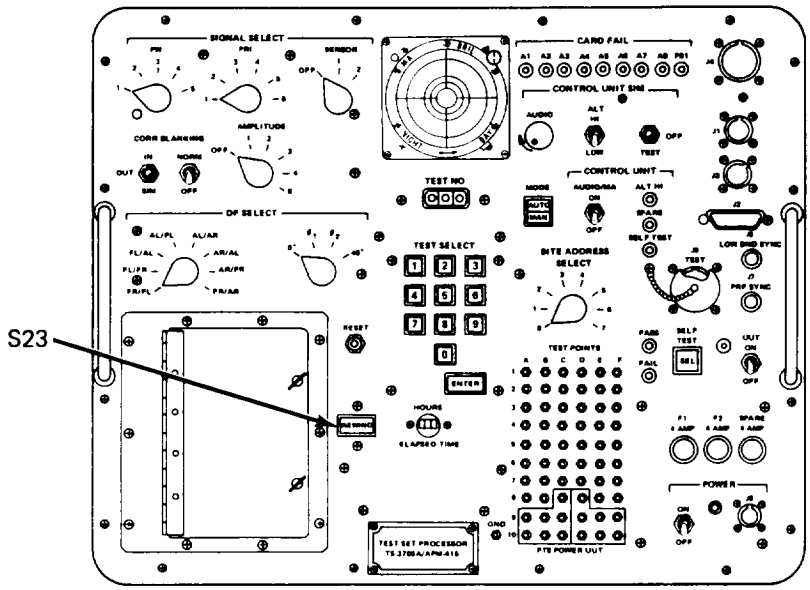
3 Perform the installation procedures provided in paragraphs 4-43 c. and 4-39 c.

4 Perform the testing procedures provided section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38 c. after successful completion of step 4.

PUSHBUTTON SWITCH S23 REMOVAL AND INSTALLATION

4-62. This paragraph provides you with instructions for removal and installation of pushbutton switch S23.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Pushbutton Switch S23

b. Pushbutton Switch S23 Removal:

1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-44 b. and 4-45 b. steps 4 through 7; respectively.

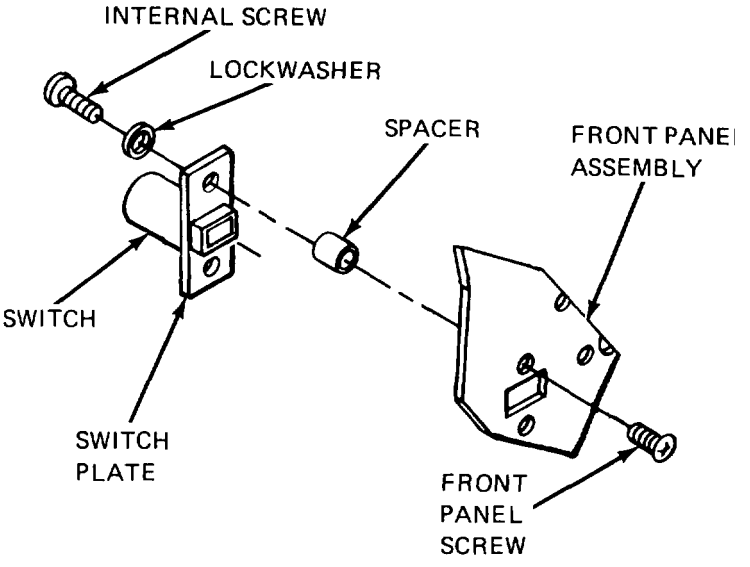
CAUTION

Limit rated power of soldering iron used for pushbutton switches to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires to pushbutton switch S23.

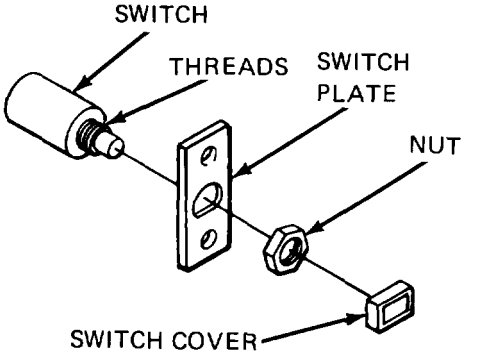
3

Remove two internal screws and two lockwashers securing switchplate to spacers. Pull switch and switch plate backward from spacers.



4

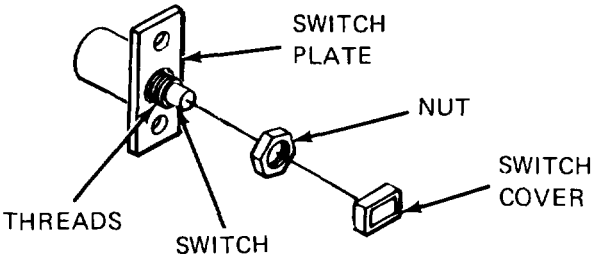
Grasp switch cover firmly between your fingers and snap switch cover out from switch.
Turn nut counterclockwise until nut is free from switch.
Pull switch free from switch plate.



c. Pushbutton Switch S23 Installation:

1

Position switch in switch plate. Position nut over switch until it contacts the threads. Turn the nut clockwise until the switch is secured to the switch plate. Press switch cover into place on switch.



2 Position switch and switch plate assembly onto spacers protruding from front panel. Secure with two screws and two lockwashers.

CAUTION

Limit rated power of soldering iron used for pushbutton switches to a maximum of 37-1/2 watts.

3 Solder all wires disconnected during removal procedures of paragraph 4-62b, and

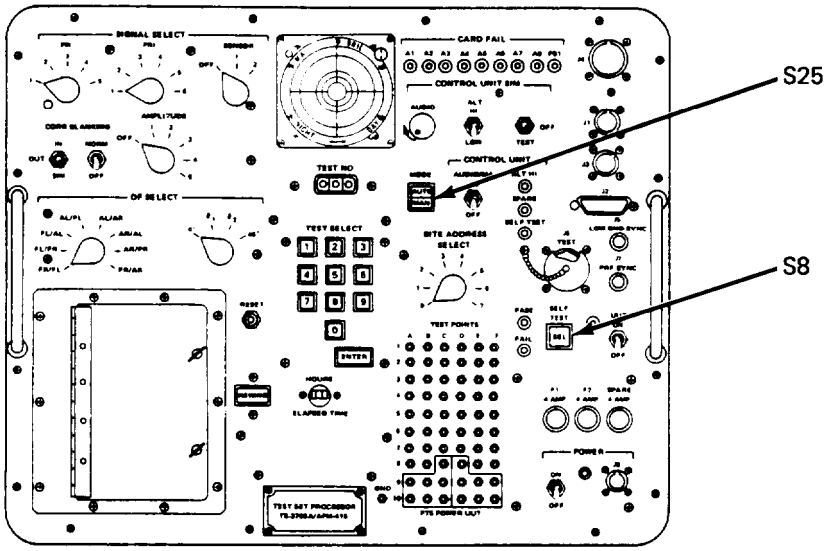
4 Perform the installation procedures provided in paragraphs 4-45 c. step 9, 4-44 c. and 4-39 c. respectively.

5 Perform the testing procedures provided in section IV of this chapter.

6 Perform the installation procedures of paragraph 4-38 c. after successful completion of step 5.

PUSHBUTTON SWITCHES S8 AND S25 REMOVAL AND INSTALLATION

4-63. This paragraph provides you with instructions for removal and installation of pushbutton switches S8 and S25.



a. Tools and Material:

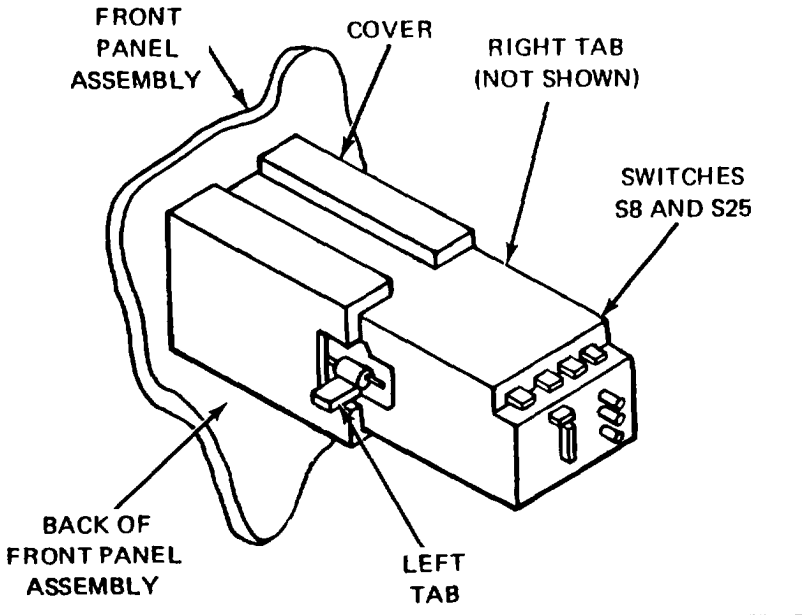
1 Tool Kit, Electronics Equipment TK-105/G

2 Pushbutton Switches S8 and S25

b. Pushbutton Switches S8 and S25 Removal:

1 Perform the removal procedures of paragraphs 4-38 b, 4-39 b, 4-43 b, 4-44 b, 4-41 b, and 4-45 b, steps 5 through 8, respectively.

2 Using pointed tool, push the left tab up and inward. Push the right tab down and inward. Slide cover away from front panel assembly and remove.



3 Push out switch from rear of front panel assembly toward front until clear.

CAUTION

Limit rated power of soldering iron used for switches to a maximum of 37-1/2 watts.

4 Tag and unsolder all wires to pushbutton switch.

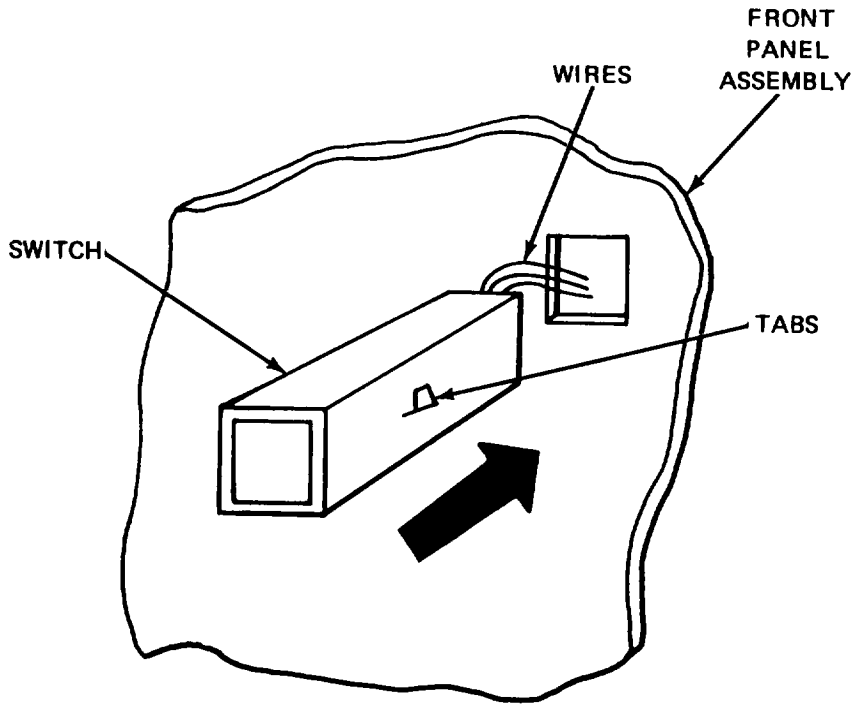
c. Pushbutton Switches S8 and S25 Installation:

CAUTION

Limit rated power of soldering iron used for switches to a maximum of 37-1/2 watts.

1 Solder all wires disconnected during removal procedure of paragraph 4-63 b. and remove

2 With tabs in and oriented to the left and right, push switch into front panel assembly.



3 Install cover as shown for step 2 of paragraph 4-63 b. Using a pointed tool, pull both left and right tabs outward, securing switch to front panel assembly.

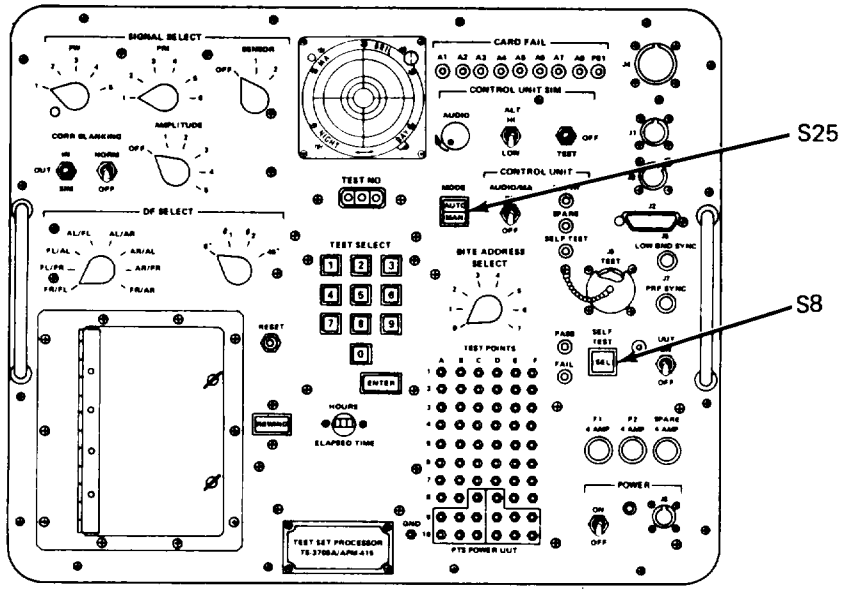
4 Perform the installation procedures provided in paragraphs 4-41 c. 4-44 c. 4-43 c. and 4-39 c. respectively.

5 Perform the testing procedures provided in section IV of this chapter.

6 Perform the installation procedures of paragraph 4-38 c, after successful completion of

PUSHBUTTON SWITCHES S8 AND S25 LAMP REMOVAL AND INSTALLATION

4-64. This paragraph provides you with instructions for removal and installation of pushbutton switches S8 and S25 indicator lamps.



a. Tools and Material:

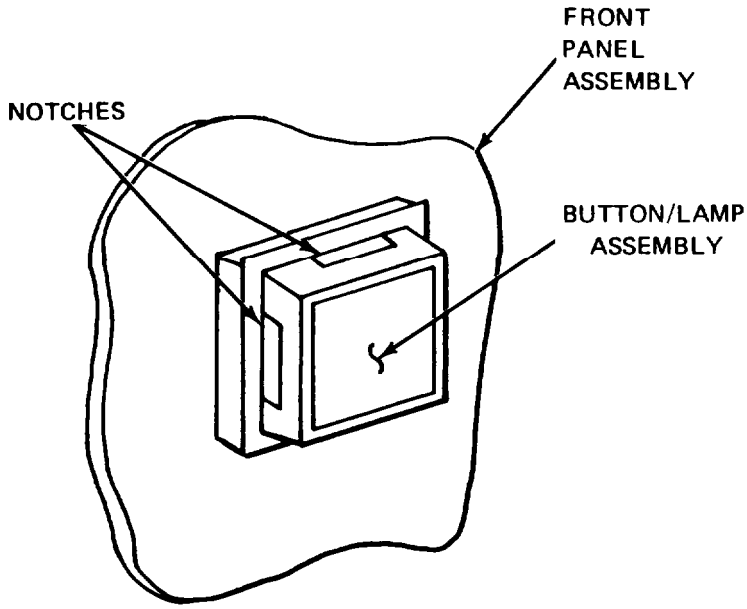
1 Tool Kit, Electronics Equipment TK-105G

2 Pushbutton Switches S8 and S25 Indicator Lamps

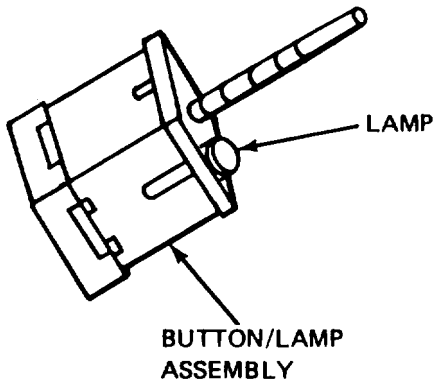
b. Pushbutton Switches S8 and S25 Lamp Removal:

1 Perform the removal procedure of paragraph 4-38 b.

2 Using fingernails of both index fingers, pry button/lamp assembly forward from front panel assembly.



3 Using thumbnail, remove defective lamp.



c. Pushbutton Switches S8 and S25 Lamp Installation:

1 Insert lamp into button/lamp assembly, removed by step 3 of paragraph 4-64 b.

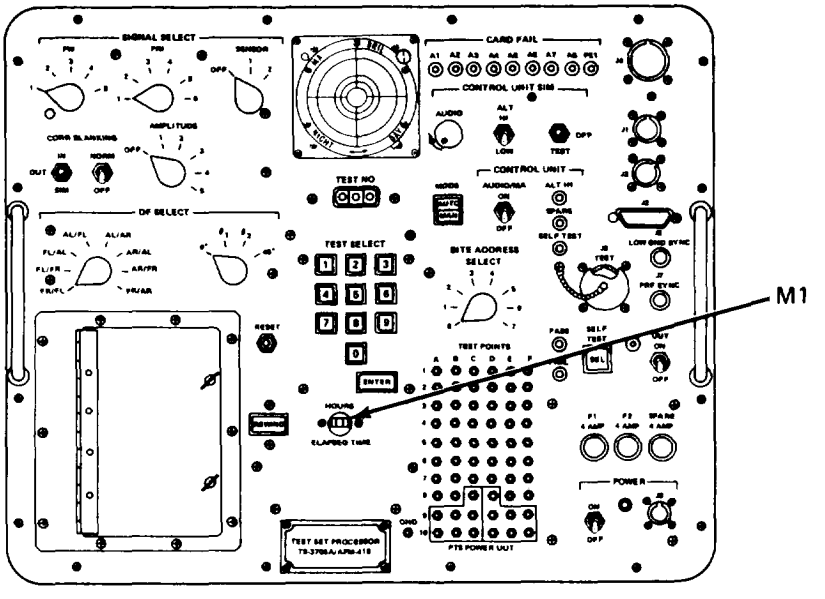
2 Insert button/lamp assembly, removed by step 2 of paragraph 4-64 b. into front panel.

3 Perform the testing procedures provided in section IV of this chapter.

4 Perform the installation procedures of paragraph 4-38 c. after successful completion of

ELAPSE TIME INDICATOR M1 REMOVAL AND INSTALLATION

4-65. This paragraph provides you with instructions for removal and installation of elapse time indicator M1.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Elapse Time Indicator M1

b. Elapse Time Indicator M1 Removal:

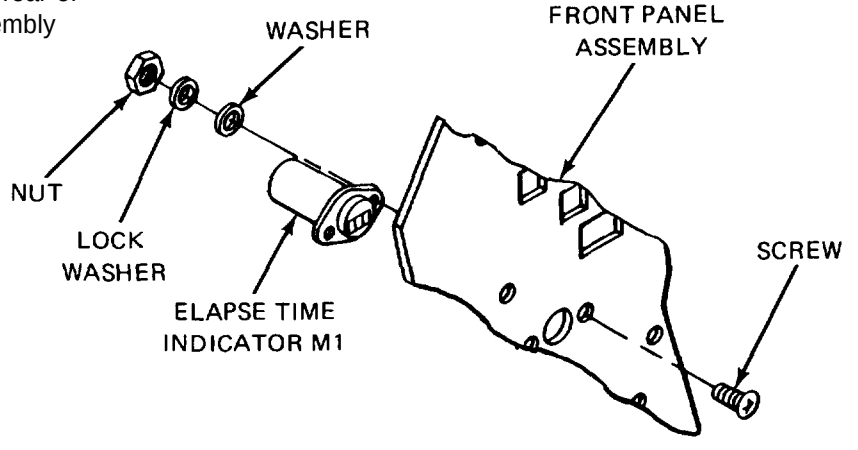
1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-44 b. and 4-45 b. steps 4 through 7, respectively.

CAUTION

Limit rated power of soldering iron used for elapse time indicator to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires to elapse time indicator M1.

3. Remove two screws, two nuts, two washers, and two lockwashers. Push the elapse time indicator backward, from the rear of the front panel assembly until free.



c. Elapse Time Indicator M1 Installation:

1. Position elapse time indicator M1 in the front panel assembly and secure using two screws, two nuts, two washers, and two lockwashers.

CAUTION

Limit rated power of soldering iron used for elapse time indicator to a maximum of 37-1/2 watts.

2. Solder all wires disconnected during removal procedures of paragraph 4-65 b and remove tags.

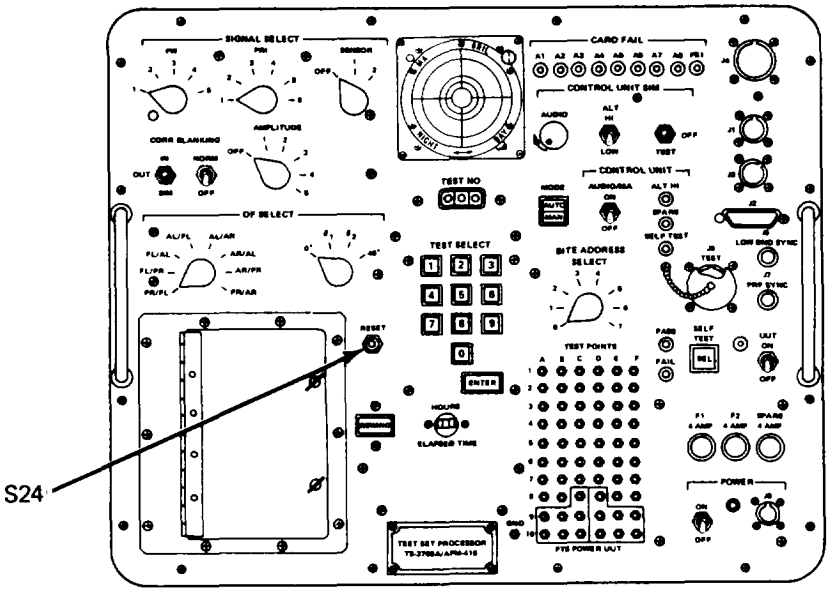
3. Perform the installation procedures provided in paragraphs 4-45 c step 9, 4-44 c, and 4-39 c, respectively.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedures of paragraph 4-38 c, after successful completion of step 4.

PUSHBUTTON SWITCH S24 REMOVAL AND INSTALLATION

4-66. This paragraph provides you with instructions for removal and installation of pushbutton switch S24.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Pushbutton Switch S24

b. Pushbutton Switch S24 Removal:

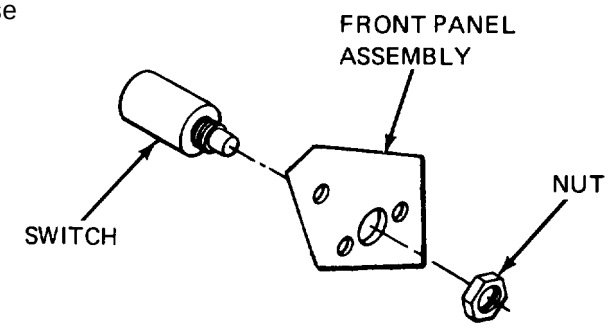
1. Perform the removal procedures of paragraphs 4-38 b. 4-39 b. 4-44 b. and 4-45 b. steps 4 through 7, respectively.

CAUTION

Limit rated power of soldering iron used for pushbutton switches to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires to pushbutton switch S24.

3. Turn nut counterclockwise until nut is free from switch. Pull switch backward from rear of front panel assembly until free.



c. Pushbutton Switch S24 Installation:

1. Position switch S24 in the front panel assembly. Position the nut over switch S24 until it contacts the threads. Turn nut clockwise until switch S24 is secured to the front panel assembly.

CAUTION

Limit rated power of soldering iron used for pushbutton switches to a maximum of 37-1/2 watts.

2. Solder all wires disconnected during removal procedures of paragraph 4-66 b and remove

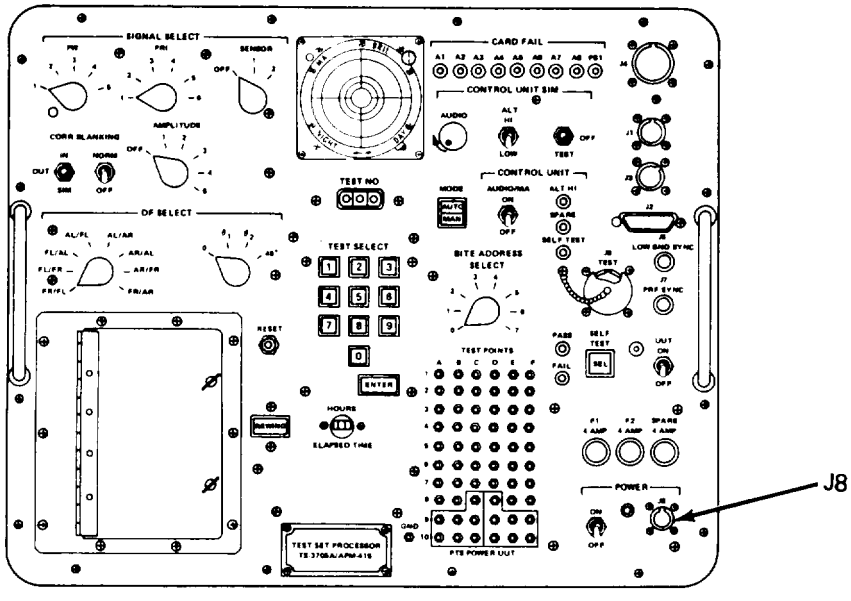
3. Perform the installation procedures provided in paragraphs 4-45c step 9, 4-44c, and 4-39c, respectively.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedures of paragraph 4-38c, after successful completion of step 4.

POWER CONNECTOR J8 REMOVAL AND INSTALLATION

4-67. This paragraph provides you with instructions for removal and installation of power connector J8.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Power Connector J8

b. Power Connector J8 Removal:

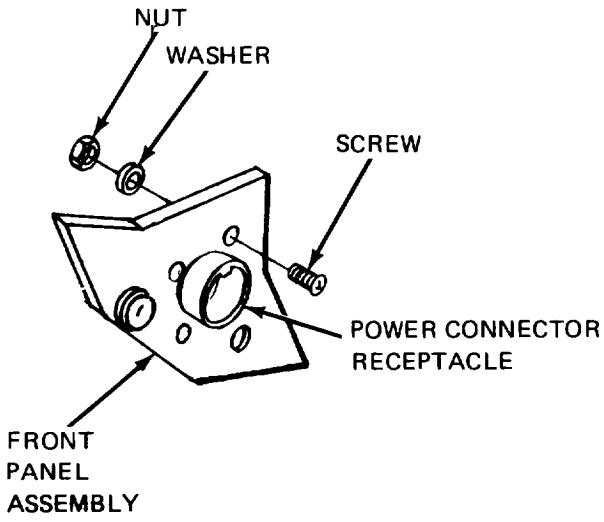
1. Perform the removal procedures of paragraphs 4-38b, 4-39b, 4-43b, 4-44b, 4-41 b, and 4-45b, steps 2 through 9; respectively.

CAUTION

Limit rated power of soldering iron used for power connector to a maximum of 37-1/2 watts.

2. Tag and unsolder all wires to power connector J8.

3. Remove four screws, four washers, and four nuts. Remove terminal lug. Pull power connector receptacle backward from rear of front panel assembly until free.



c. Power Connector J8 Installation:

1. Position power connector J8 in the front panel assembly. Position terminal lug and secure using four screws, four washers, and four nuts.

CAUTION

Limit rated power of soldering iron used for power connector to a maximum of 37-1/2 watts.

2 Solder all wires disconnected during removal procedures of paragraph 4-67b and remove tags.

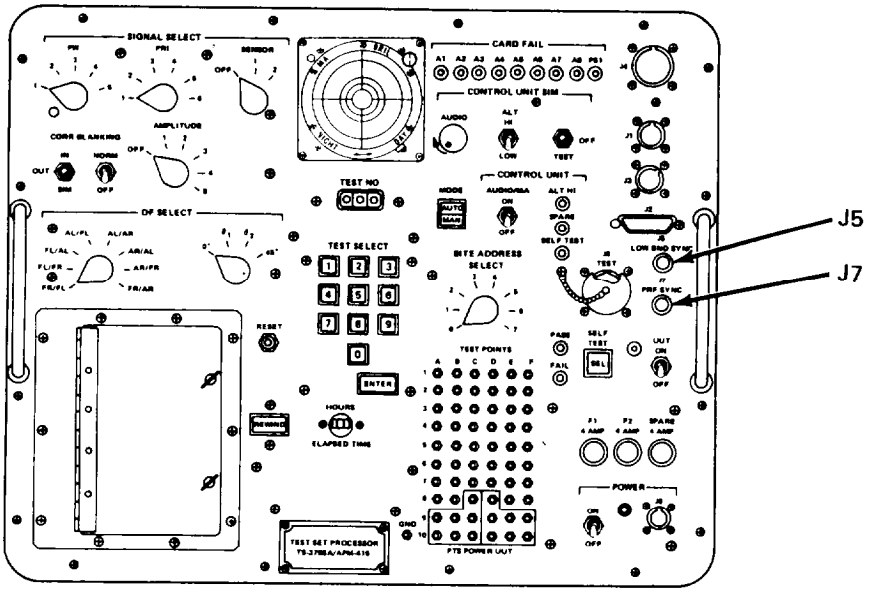
3 Perform the installation procedures provided in paragraphs 4-45c, steps 4 through 9, 4-41c, 4-44c, 4-43c, and 4-39c, respectively.

4 Perform the installation procedures of paragraph 4-38c, after successful completion of

5 Perform the testing procedures provided in Section IV of this chapter.

COAXIAL RF CONNECTORS J5 AND J7 REMOVAL AND INSTALLATION

4-68. This paragraph provides you with instructions for removal and installation of coaxial rf connectors J5 and J7.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Coaxial RF Connectors J5 and J7

b. Coaxial RF Connectors J5 and J7 Removal:

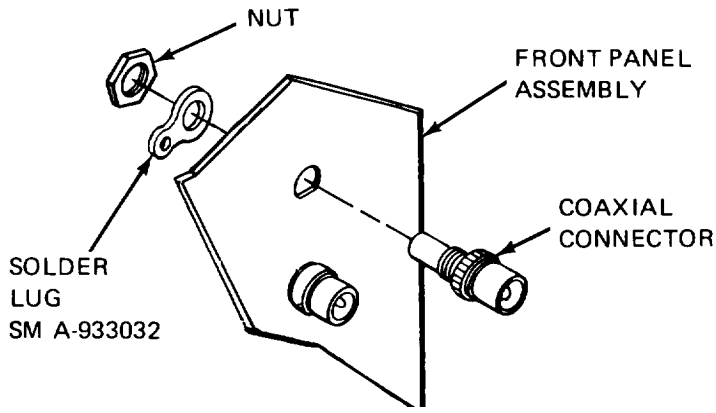
1. Perform the removal procedures of paragraphs 4-38b and 4-39b, respectively.

CAUTION

Limit rated power of soldering iron used for coaxial rf connectors to a maximum of 37-1/2 watts.

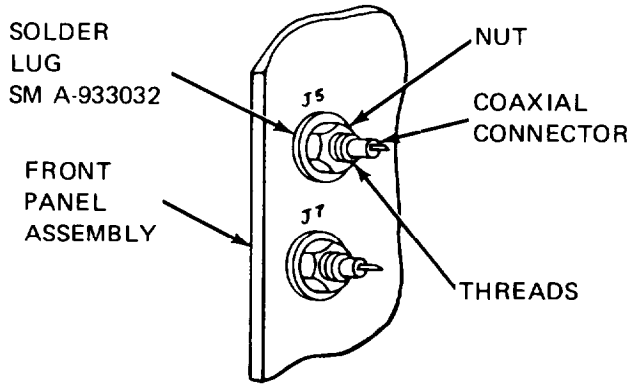
2. Tag and unsolder wire to coaxial rf connector.

3. Turn nut counterclockwise until nut is free from coaxial rf connector. Remove solder lug. Pull coaxial rf connector and coaxial cable forward from front of front panel assembly until free.



c. Coaxial RF Connectors J5 and J7 Installation:

1. Position coaxial rf connector through front panel . assembly. Slide solder lug and nut over coaxial connector until nut contacts coaxial connector threads. Turn nut clockwise until coaxial connector is secured to front panel assembly.



CAUTION

Limit rated power of soldering iron used for coaxial rf connectors to a maximum of 37-1/2 watts.

2 Solder wire disconnected during removal procedure of paragraph 4-68b and remove tag.

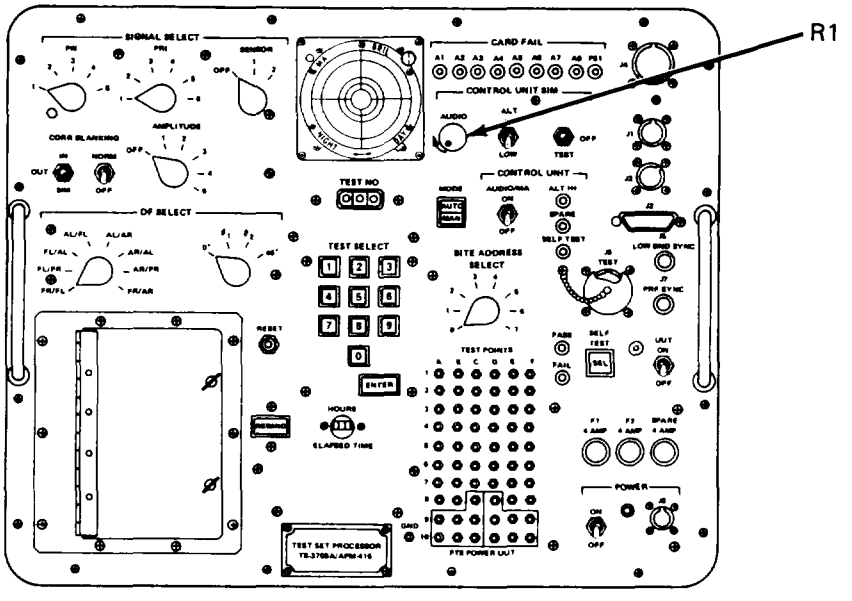
3 Perform the installation procedure provided in paragraph 4-39c.

4 Perform the testing procedures provided in section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38c, after successful completion of

VARIABLE RESISTOR R1 REMOVAL AND INSTALLATION

4-69. This paragraph provides you with instructions for removal and installation of variable resistor R1.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Variable Resistor R1

b. Variable Resistor R1 Removal:

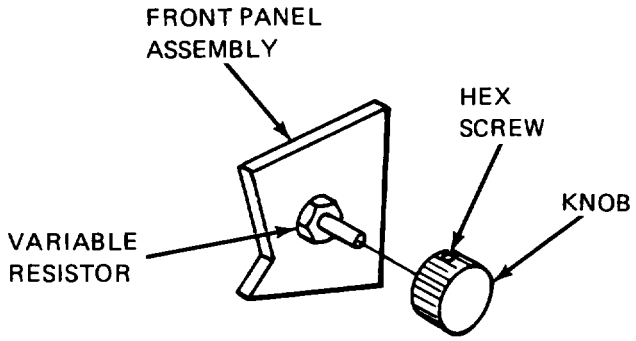
1 Perform the removal procedures of paragraphs 4-38b, 4-39b, and 4-43b,

CAUTION

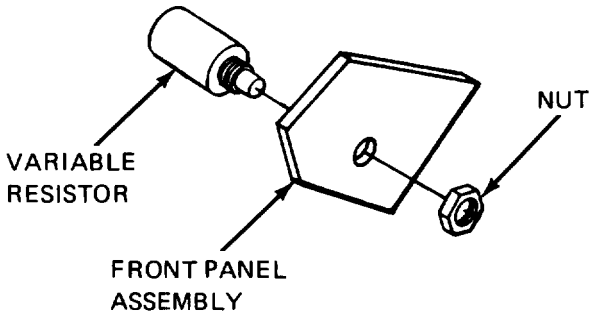
Limit rated power of soldering iron used for variable resistor to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires to variable resistor R1.

3 Loosen hex screw by turning hex screw counterclockwise. Remove knob from variable resistor.



4 Turn nut counterclockwise until nut is free from variable resistor. Pull variable resistor backward, from rear of front panel assembly until free.



c. Variable Resistor R1 Installation:

1. Position the variable resistor in the front panel assembly. Position the nut over the variable resistor until it contacts the threads, Turn nut clockwise until variable resistor is secured to the front panel assembly.

2. Rotate variable resistor shaft fully counterclockwise. Position white dot of knob at approximate 7 o'clock position and secure using hex screw.

CAUTION

Limit rated power of soldering iron used for variable resistor to a maximum of 37-1/2 watts.

3. Solder all wires disconnected during removal procedure of paragraph 4-69b and remove tags.

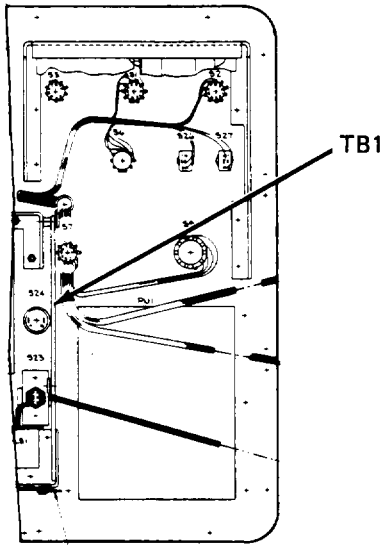
4. Perform the installation procedures provided in paragraphs 4-43c and 4-39gc.

5. Perform the testing procedures provided in section IV of this chapter.

6. Perform the installation procedures of paragraph 4-38c, after successful completion of step 5.

TERMINAL BOARD TB1 REMOVAL AND INSTALLATION

4-70. This paragraph provides you with instructions for removal and installation of terminal board TB1.



a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Terminal Board TB1

b. Terminal Board TB1 Removal:

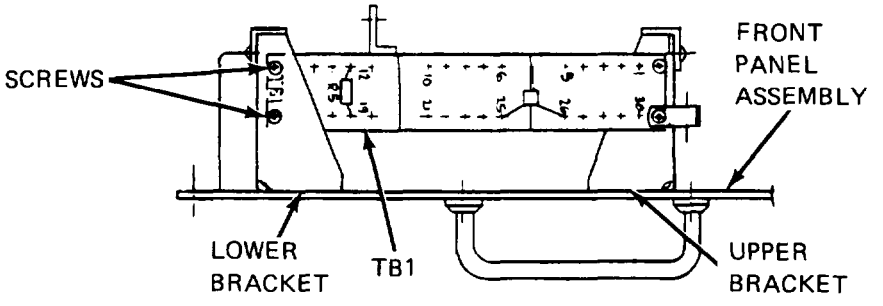
1 Perform the removal procedures provided in paragraphs 4-38b, 4-39b, 4-44b, 4-45b, steps 4 through 7, and 4-42b, respectively.

CAUTION

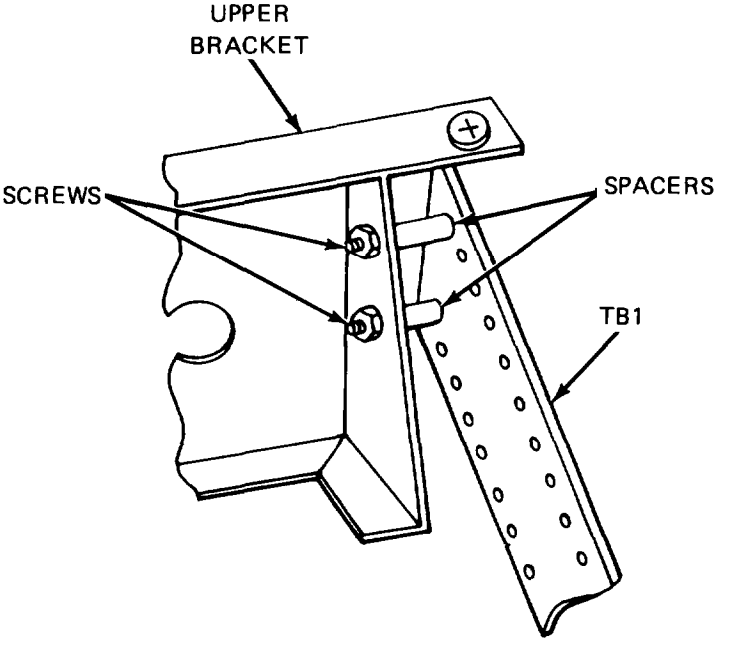
Limit rated power of soldering iron used for terminal board to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires to terminal board TB1.

3 Remove two screws, with nuts, washers, and lockwashers, securing terminal board TB1 to lower bracket.



4 Remove two screws with nuts, washers, lockwashers, and spacers, securing terminal board TB1 to upper bracket.



c. Terminal Board TB1 Installation:

1 Position terminal board TB1 near its normal position. Secure to upper bracket using two screws with nuts, washers, lockwashers, and spacers.

2 Secure terminal board TB1 to lower bracket using two screws, with nuts, washers, and lockwashers.

CAUTION

Limit rated power of soldering iron used for terminal board to a maximum of 37-1/2 watts.

3 Solder all wires disconnected during removal procedure of paragraph 4-70b

4 Perform the installation procedures provided in paragraphs 4-42c, 4-45c, step 9, 4-44c, and 4-39c, respectively.

5 Perform the testing procedures provided in section IV of this chapter.

6 Perform the installation procedures of paragraph 4-38c, after successful completion of step 5.

PERMANENT MAGNET LOUDSPEAKER LS1 REMOVAL AND INSTALLATION

4-71. This paragraph provides you with instructions for removal and installation of permanent magnet loudspeaker LS1.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Permanent Magnet Loudspeaker LS1

b. Permanent Magnet Loudspeaker LS1 Removal:

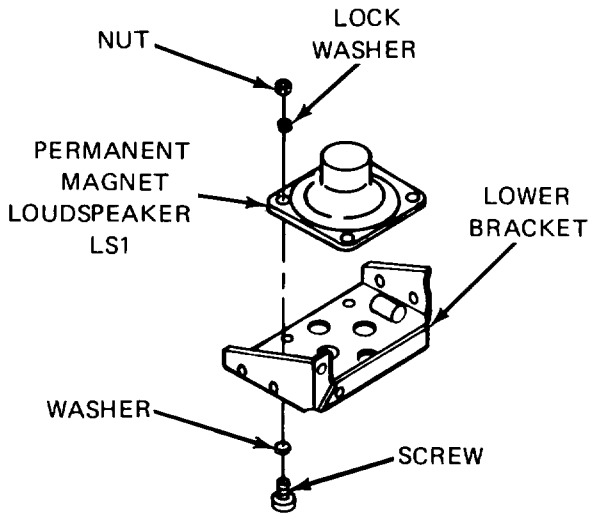
1 Perform the removal procedures provided in paragraphs 4-38b, 4-39b 4-44b, and 4-45b, steps 4 through 7, respectively.

CAUTION

Limit rated power of soldering iron used for loudspeaker to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires to permanent magnet loudspeaker LS1.

3 Remove four screws, four washers, four lockwashers, and four nuts securing permanent magnet loudspeaker LS1 to lower bracket.



4 Lift loudspeaker free from lower bracket.

c. Permanent Magnet Loudspeaker LS1 Installation:

1 Position permanent magnet loudspeaker LS1 on the lower bracket and secure using four screws, four washers, four lockwashers, and four nuts.

CAUTION

Limit rated power of soldering iron used for loudspeaker to a maximum of 37-1/2 watts.

2 Solder all wires disconnected during removal procedure of paragrah 4-71 b

3 Perform the installation procedures provided in paragraphs 4-45c, step 9, 4-44c, and 4-39c, respectively.

4 Perform the testing procedures provided in section IV of this chapter.

5 Perform the installation procedures of paragraph 4-38c, after successful completion of step 4.

TERMINAL BOARD TB2 REMOVAL AND INSTALLATION

4-72. This paragraph provides you with instructions for removal and installation of terminal board TB2.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Terminal Board TB2

b. Terminal Board TB2 Removal:

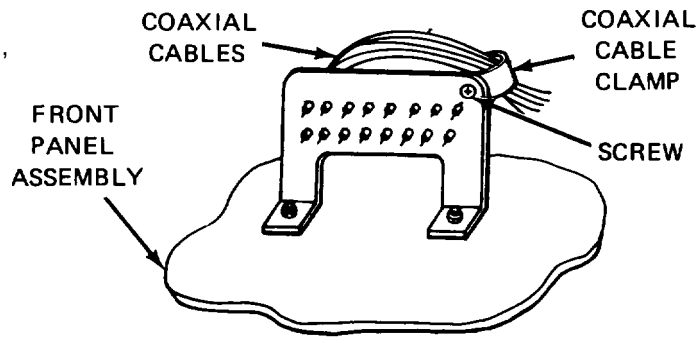
1 Perform the removal procedures provided in paragraphs 4-38b and 4-39b, respectively.

CAUTION

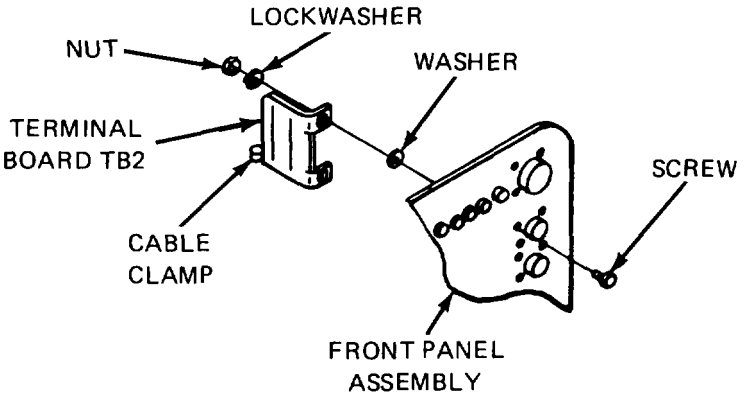
Limit rated power of soldering iron used for terminal board to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires connected to terminal board TB2.

3 Remove screw, nut, lockwasher, and coaxial cable clamp.



4 Remove two screws, two lockwashers, two washers, and two nuts. Pull terminal board TB2 free from front panel assembly.



c. Terminal Board TB2 Installation:

1 Position terminal board TB2 on the front panel assembly. Secure using two screws, two washers, two lockwashers, and two nuts.

2 Install coaxial cable clamp removed by step 3 of paragraph 4-72b, using screw, nut, and lockwasher.

CAUTION

Limit rated power of soldering iron used for terminal board to a maximum of 37-1/2 watts.

3 Solder all wires disconnected during removal procedure of paragraph 4-72b and remove tags.

4 Perform the installation procedures provided in paragraph 4-39c.

5 Perform the testing procedures provided in section IV of this chapter.

6 Perform the installation procedures of paragraph 4-38c, after successful completion of step 5.

FAN REMOVAL AND INSTALLATION

4-73. This paragraph provides you with instructions for removal and installation of the cooling fan.

a. Tools and Material:

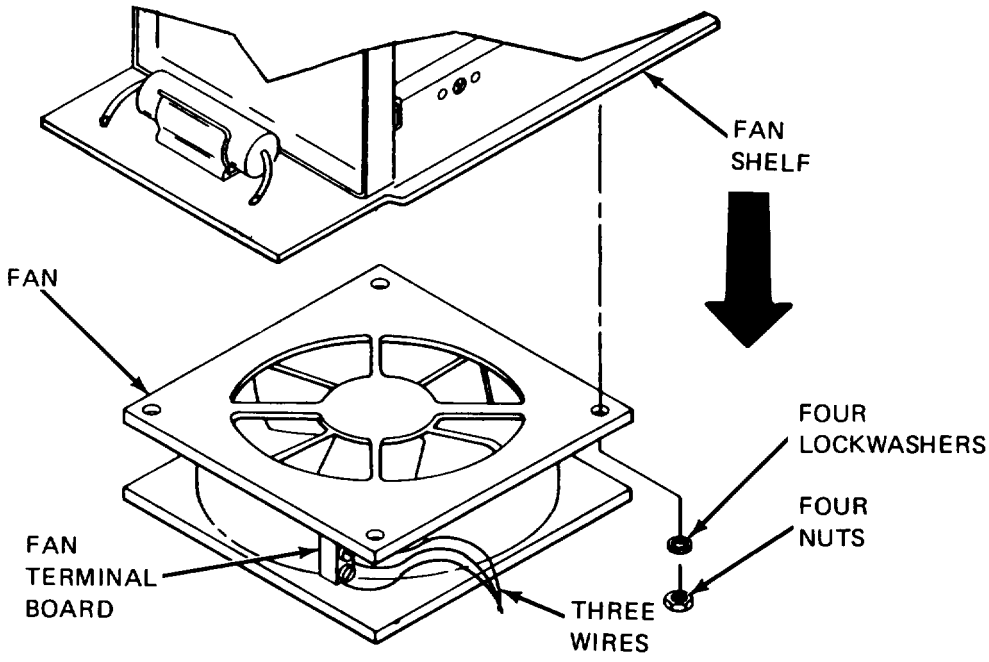
1 Tool Kit, Electronics Equipment TK-105/G

2 Fan

b. Fan Removal:

1 Perform the removal procedures in paragraphs 4-38b and 4-39b, respectively.

2 Remove four nuts, with lockwashers, fastening fan to fan shelf.



3 Tag and disconnect three wires from the fan terminal board.

4 Remove fan.

c. Fan Installation:

1. Connect three wires to fan terminal board and remove tags.
2. Position fan on fan shelf. Secure fan using four nuts with lockwashers.
3. Perform the installation procedures provided in paragraph 4-39c.
4. Perform the testing procedures provided in section IV of this chapter.
5. Perform the installation procedures of paragraph 4-38c, after successful completion of step 4.

DIODE CR17 AND FIXED RESISTOR R2 REMOVAL AND INSTALLATION

4-74. This paragraph provides you with instructions for removal and installation of diode CR17 and fixed resistor R2.

a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Semiconductor Diode CR17
3. Fixed Resistor R2

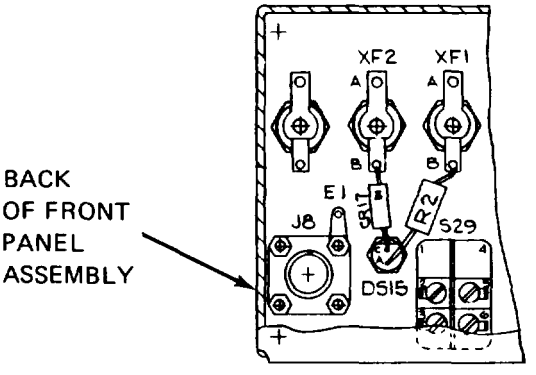
b. Diode CR17 and Fixed Resistor R2 Removal:

1. Perform the removal procedures of paragraphs 4-38b, 4-39b, 4-43b, 4-44b, 4-41b, and steps 4 through 7 of paragraph 4-45b, respectively.

CAUTION

Limit rated power of soldering iron used for diode and resistor to a maximum of 37-1/2 watts.

2 Unsolder defective diode or resistor and remove.



c. Diode CR17 and Fixed Resistor R2 Installation:

CAUTION

Limit rated power of soldering iron used for diode and resistor to a maximum of 37-1/2 watts.

1 Solder replacement diode or resistor in proper position and trim excess leads.

2 Perform the installation procedures provided in paragraphs 4-45c, steps 4 through 9, 4-41c, 4-44c, 4-43c, and 4-39c, respectively.

3 Perform the testing procedures provided in section IV of this chapter.

4 Perform the installation procedures of paragraph 4-38c, after successful completion of step 3.

FIXED RESISTOR R3 REMOVAL AND INSTALLATION

4-75. This paragraph provides you with instructions for removal and installation of fixed resistor R3.

a. Tools and Material:

1 Tool Kit, Electronics Equipment TK-105/G

2 Fixed Resistor R3

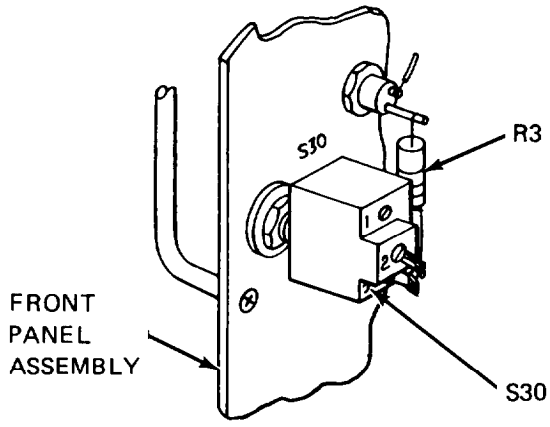
b. Fixed Resistor R3 Removal:

1 Perform the removal procedures of paragraphs 4-38b and 4-39b, respectively.

CAUTION

Limit rated power of soldering iron used for resistor to a maximum of 37-1/2 watts.

2 Unsolder R3 leads and remove R3.



c. Fixed Resistor R3 Installation

CAUTION

Limit rated power of soldering iron used for resistor to a maximum of 37-1/2 watts.

1. Solder replacement fixed resistor R3 in proper position and trim excess leads.
2. Perform the installation procedures provided in paragraph 4-39c.
3. Perform the testing procedures provided in section IV of this chapter.
4. Perform the installation procedures of paragraph 4-38c, after successful completion of step 3.

FIXED RESISTOR R4 REMOVAL AND INSTALLATION

4-76. This paragraph provides you with instructions for removal and installation of fixed resistor R4.

a. Tools and Material

1. Tool Kit, Electronics Equipment TK-105/G
2. Fixed Resistor R3
3. Thermal Conductive Paste

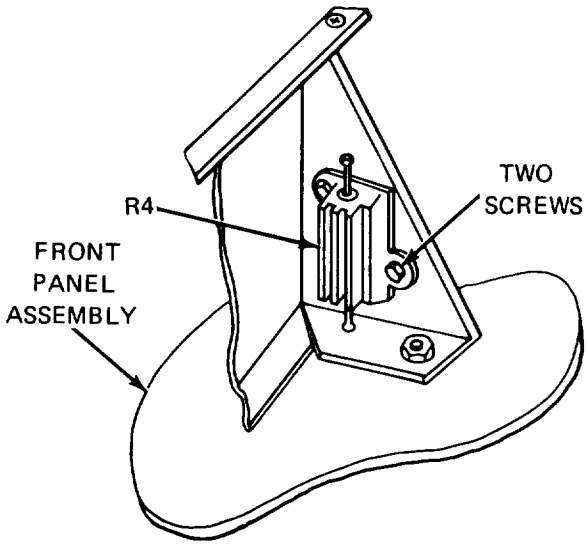
b. Fixed Resistor R4 Removal:

1. Perform the removal procedures of paragraphs 4-38b, 4-39b, 4-44b, and 4-45b, steps 4 through 7, respectively.

CAUTION

Limit rated power of soldering iron used for resistor to a maximum of 37-1/2 watts.

2 Tag and unsolder all wires to resistor R4 terminals.



3 Remove two screws, with nuts and lockwashers. Remove resistor R4.

c. Fixed Resistor R4 Installation:

1 Apply thin coating of thermal conductive paste to base of resistor R4.

2 PositIon resistor R4 and secure with two screws, lockwashers, and nuts.

CAUTION

Limit rated power of soldering iron used for resistor to a maximum of 37-1/2 watts.

3. Solder all wires and remove tags.

4. Perform installation procedures provided in paragraphs 4-45c, step 9, 4-44c, and 4-39c, respectively.

5. Perform the testing procedures provided in Section IV of this chapter.

6. Perform the installation procedures of paragraph 4-38c, after successful completion of step 5.

FIXED CAPACITOR C1 REMOVAL AND INSTALLATION

4-77. This paragraph provides you with instructions for removal and installation of fixed capacitor C1.

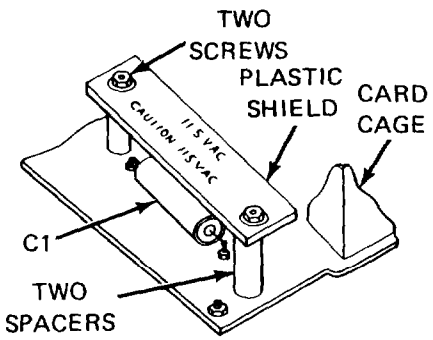
a. Tools and Material

1. Tool Kit, Electronic Equipment TK-105/G
2. Fixed Capacitor C1

b. Fixed Capacitor C1 Removal

1. Perform the removal procedures of paragraphs 4-38b, 4-39b, and 4-41b, respectively.

2 Remove plastic shield secured with two screws, lockwashers, and nuts.



CAUTION

Limit rated power of soldering iron used for capacitor to a maximum of 37-1/2 watts.

3 Tag and unsolder capacitor C1 leads and remove.

c. Fixed Capacitor C1 Installation:

CAUTION

Limit rated power of soldering iron used for capacitor to a maximum of 37-1/2 watts.

1 Position capacitor C1 and solder leads. Trim excess leads and remove tags.

2 Perform the installation procedures provided in paragraphs 441c and 4-39c, respectively.

3 Perform testing procedures provided in section IV of this chapter.

4 Perform the installation procedures of paragraph 4-38c, after successful completion of step 3.

FIXED CAPACITOR C2 AND RESISTOR R5 REMOVAL AND INSTALLATION

4-78. This paragraph provides you with instructions for removal and installation of fixed capacitor C2 and fixed resistor R5.

a. Tools and Material:

1. Tool Kit, Electronic Equipment TK-105/G
2. Fixed Resistor R5
3. Fixed Capacitor C2

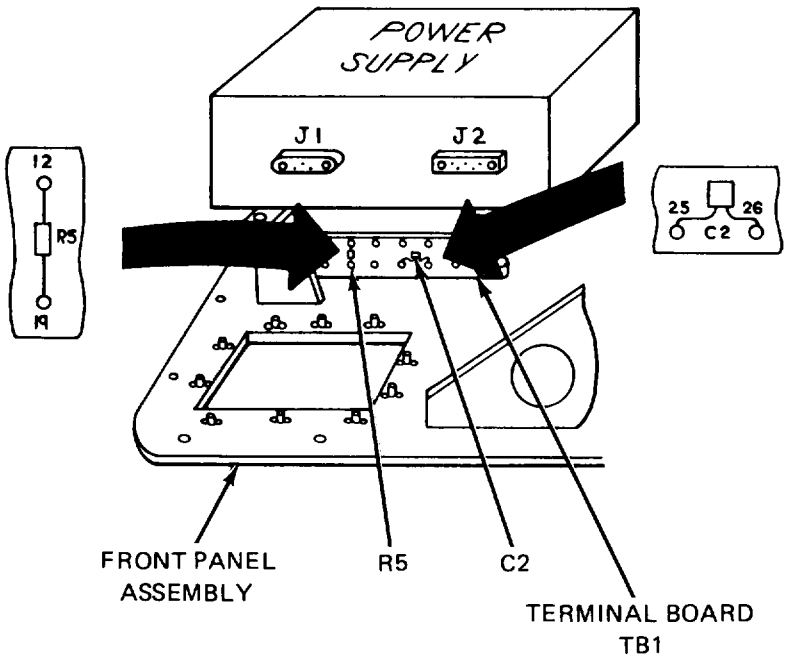
b. Fixed Capacitor C2 or Resistor R5 Removal:

1. Perform the removal procedures of paragraphs 4-38b, 4-39b, and 4-42b, respectively.

CAUTION

Limit rated power of soldering iron used for resistor or capacitor to a maximum of 37-1/2watts.

2. Unsolder defective capacitor C2 or resistor R5 and remove.



c. Fixed Capacitor C2 or Resistor R5 Installation:

CAUTION

Limit rated power of soldering iron used for resistor or capacitor to a maximum of 37-1/2 watts.

1. Solder replacement capacitor C2 or resistor R5 in proper position and trim excess leads.
2. Perform the installation procedures provided in paragraphs 4-42c and 4-39c,
3. Perform the testing procedures provided in section IV of this chapter.
4. Perform the installation procedures of paragraph 4-38c, after successful completion of step 3.

CONNECTOR P15 REMOVAL AND INSTALLATION

4-79. This paragraph provides you with instructions for removal and installation of connector P15.

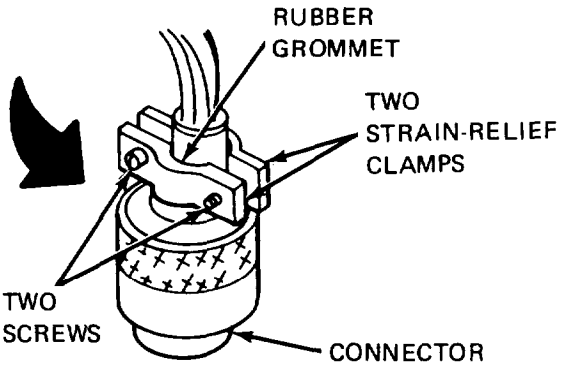
a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Connector P15

b. Connector P15 Removal:

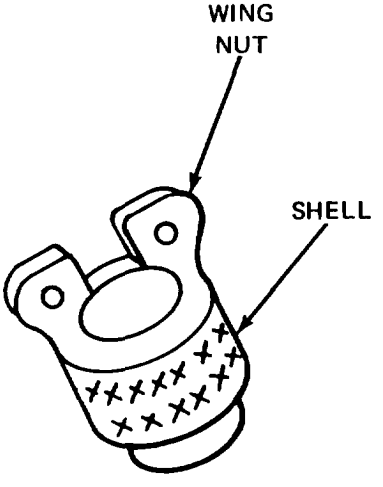
1. Perform the removal procedures provided in paragraphs 4-38b and 4-39b, respectively.

2 Remove two screws and two strain-relief clamps from connector.



3 Push back rubber grommet wire protector.

4 Reconnect P15 and J1. Gently turn wing nut until free, then disconnect P15 and J1.



CAUTION

Limit rated power of soldering iron used for connector pins to a maximum of 37-1/2 watts.

5 Slide back shrink tubing type insulation from each wire. Tag and unsolder all wires to connector P15.

c. Connector P15 Installation:

CAUTION

Limit rated power of soldering iron used for connector pins to a maximum of 37-1/2 watts.

1. Solder all wires to connector P15. Slide shrink tubing type insulation back over each wire and then remove tags.

2. Reconnect P15 and J1. Gently tighten wing nut, then disconnect P15 and J1.

3. Slide rubber grommet into place.

4. Install two strain-relief clamps using two screws.

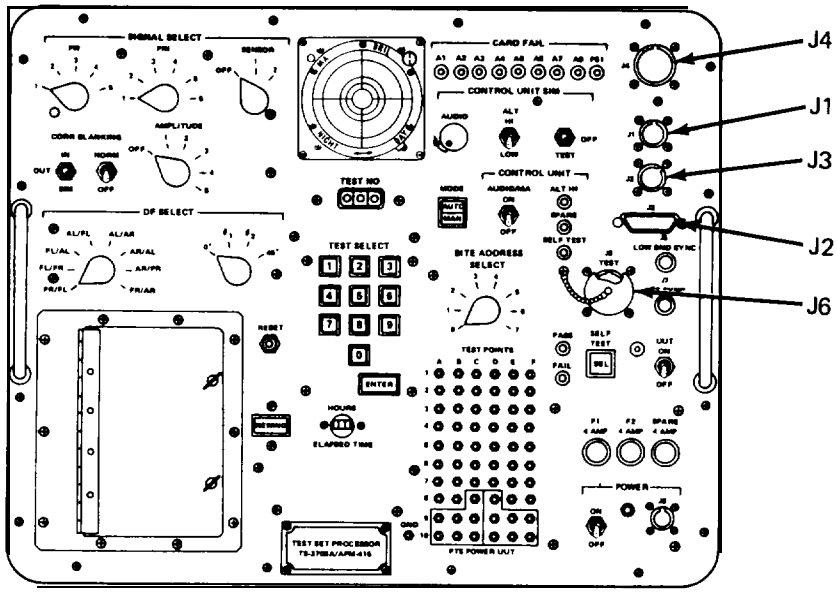
5. Perform the installation procedures provided in paragraph 4-39c.

6. Perform the testing procedures provided in section IV of this chapter.

7. Perform the installation procedures of paragraph 4-38c, after successful completion of step 6.

CONNECTORS J1, J2, J3, J4, AND J6 PIN REPLACEMENT

4-80. This paragraph provides you with instructions for pin replacement for connectors J1, J2, J3, J4, and J6.



a. Tools and Material:

1. Tool Kit, Electronics Equipment TK-105/G
2. Connector pins
3. Extraction/Insulation Tools

b. Connector J4 Pin Replacement:

1. Using normal shop practices, replace damaged pin(s) of connector J4.
2. Perform the installation procedure in paragraph 4-39c.
3. Perform the testing procedures provided in section IV of this chapter.
4. Perform the installation procedure in paragraph 4-38c, after successful completion of step 3.

c. Connectors J1, J2, J3 and J6 Pin Replacement

1. Perform the removal procedure in paragraph 4-41 b.

2. Using normal shop practices, replace damaged pin(s) of connector(s) J1, J2, J3 or J6.

3. Perform the installation procedure in paragraph 4-41c and 4-39c.

4. Perform the testing procedures provided in section IV of this chapter.

5. Perform the installation procedure in paragraph 4-38c, after successful completion of step 4.

SECTION VII
DESTRUCTION OF ARMY ELECTRONICS MATERIAL

SECTION CONTENTS — PAGE

GENERAL INSTRUCTIONS

4-81. If you receive orders to destroy the processor test set, do a thorough job. Don't leave anything intact if it may possibly be of use to the enemy. The following paragraph lists the preferred methods of destruction. However, if you don't have the right materials available, use anything you can find to do the job; brush fires, stones, clubs, etc. DESTROY everything you can.

METHODS OF DESTRUCTION

4-82. Here are the best ways to destroy the processor test set; use them if you can.

- SMASH - using a hammer, a sledgehammer, or a club, break up or distort these items:
  - PTS front panel
  - Connectors on PTS front panel and cables
  - Processor test set case
- CUT - using axes or knives, cut all cables into small pieces.
- BURN - Soak cable pieces, the PTS, and the technical manual with gasoline or fuel oil. Ignite by throwing torches, grenades, or by direct fire.
- CRUSH - Run over the PTS and the processor test set case with a vehicle, preferably with a tracked vehicle.
- SCATTER - Remove as many parts as you can cut or wrench out of the PTS. Scatter these parts as widely as possible.

PRIORITIES

4-83. If time is short, destroy the following items of the PTS in priority order:

- Circuit card A1
- Magnetic Cassette tapes MTC5079654 and MTC5079655
- Circuit card A2
- Circuit cards A3 thru A5 and A7 thru A9
- PTS front panel
- Cables W1 thru W5 and power adapter cable
- Processor test set case

SECTION VIII
ADMINISTRATIVE STORAGE

SECTION CONTENTS

ADMINISTRATIVE STORAGE PROCEDURES

4-84. When storage is only for a short term (1 to 45 days), the processor test set should be placed indoors in a safe area where it will be protected from damage or adverse environmental factors such as water or extreme dust.

INTERMEDIATE AND LONG TERM STORAGE

4-85. For intermediate (46 to 180 days) or long term storage (180 days or more), it is recommended that the PTS and all major items (refer to paragraph 1-8, section II, chapter 1) be stored in the processor test set case. Under these conditions, the processor test set will be complete when removed for use.

APPENDIX A
REFERENCES

A-1 SCOPE

The following is a list of all forms, technical bulletins, and technical manuals referenced in this manual.

A-2 PAMPHLETS

Consolidated Index of Army Publications and Blank Forms . . . . . DA Pam 310-1

A-3 FORMS AND RECORDS

Discrepancy in Shipment Report (DISREP) SF-361
Report of Discrepancy (ROD) SF-364
Quality Deficiency Report SF-368
Recommended Changes to Publications and Blank Forms . . . . . DA Form 2028
Recommended Changes to Equipment Technical Manuals . . . . . DA Form 2028-2
Equipment Inspection and Maintenance Worksheet . . . . . DA Form 2404

A-4 SUPPLY BULLETINS

Painting and Preservation of Supplies Available for Field
Use for Electronics Command Equipment SB11-573
Preservation, Packaging, Packing and Marking Materials,
Supplies, and Equipment Used by Army SB38-100

A-5 TECHNICAL BULLETINS

Field Instructions for Painting and Preserving Electronics Command Equipment
Including Camouflage Pattern Painting of Electrical Equipment Shelters . . . . . TB 43-0118

A-6 TECHNICAL MANUALS

Aviation Unit Maintenance (AVUM) Manual, Radar Signal Detecting Set
AN/APR-39(V)1 (NSN 5841-01-023-7112) . . . . . TM 11-5841-283-12
Aviation Unit Maintenance (AVUM) Manual, Radar Signal Detecting Set
AN/APR-39(V)2 (NSN 5841-01-054-8540) . . . . . TM 11-5841-288-12
Direct Support and General Support Maintenance Manual, Aviation
Intermediate Maintenance (AVIM) Digital Processor CM-480A/APR-39(V)
(NSN 5841-01-054-8541) and Detecting Set Control C-10412A/APR-39(V)
(NSN 5841-01-149-4094) . . . . . TM 11-5841-288-34-1
Direct Support and General Support Maintenance Manual, Aviation
Intermediate Maintenance (AVIM), Digital Processor CM-480A/APR-39(V)
(NSN 5841-01-054-8541) and Detecting Set Control C-10412A/APR-39(V)
(NSN 5841-01-149-4094) (CLASSIFIED SUPPLEMENT) . . . . . TM 11-5841-288-34-2

APPENDIX A (Continued)

Repair Parts and Special Tools List (Including Depot Maintenance Parts) for Test Set, Processor AN/APM-415A (NSN 6625-01-147-4741) . . . . . TM 11-6625-2940-24P
Repair Parts and Special Tools List (Including Depot Maintenance Parts) for Digital Processor CM-480A/APR-39(V) (NSN 5841-01-054-8541) and Detecting Set Control C-10412A/APR-39(V) (NSN 5841-01-149-4094) . . . TM 11-5841-288-24P
The Army Maintenance Management System (TAMMS) . . . . . DA PAM 738-750
Administrative Storage of Equipment . . . . . TM 740-90-1
Destruction of Army Electronics Materiel TM750-244-2

APPENDIX B
MAINTENANCE ALLOCATION CHART FOR PROCESSOR TEST SET AN/APM-415A

SECTION I

INTRODUCTION

B-1 Maintenance Allocation Chart

a. This Maintenance Allocation Chart (MAC) assigns maintenance functions in accordance with the Three Levels of Maintenance concept for Army aviation. These maintenance levels (categories) -Aviation Unit Maintenance (AVUM), Aviation Intermediate Maintenance (AVIM), and Depot Maintenance - are depicted on the MAC as:

AVUM, which corresponds to an 0 Code in the Repair Parts and Special Tools List (RPSTL)

AVIM, which corresponds to an F Code in the Repair Parts and Special Tools List (RPSTL)

DEPOT, which corresponds to a D Code in the Repair Parts and Special Tools List (RPSTL)

b. The maintenance to be performed below depot and in the field is described as follows:

(1) Aviation Unit Maintenance (AVUM) activities will be staffed and equipped to perform high frequency “On-Aircraft” maintenance tasks required to retain or return aircraft systems to a serviceable condition. The maintenance capability of the AVUM will be governed by the Maintenance Allocation Chart (MAC) and limited by the amount and complexity of ground support equipment (GSE), facilities required, authorized manning strength, and critical skills available. The range and quantity of authorized spare modules/components will be consistent with the mobility requirements dictated by the air mobility concept. (Assignments of maintenance tasks to divisional company size aviation units will consider the overall maintenance capability of the division, the requirement to conserve personnel and equipment resources, and air mobility requirements.)

(a) Company Size Aviation Units: Perform those tasks which consist primarily of preventive maintenance and maintenance repair and replacement functions associated with sustaining a high level of aircraft operational readiness. Perform maintenance inspections and servicing to include preflight, daily, intermediate, periodic (or phased), and special inspections as authorized by the MAC or higher headquarters. Identify the cause of equipment/system malfunctions using applicable technical manual troubleshooting instructions, built-in test equipment (BITE), installed aircraft instruments, or test, measurement, and diagnostic equipment (TMDE). Replace worn or damaged modules/components that do not require complex adjustments or system alinement and which can be removed/installed with available skills, tools, and ground support equipment. Perform operational and continuity checks and make minor repairs to the electrical system. Inspect, service and make operational, capacity, and pressure checks to hydraulic systems. Perform servicing, functional adjustments, and minor repair/replacement to the flight control, propulsion, power train, and fuel systems. Accomplish air frame repair that does not require extensive disassembly, jigging, or alinement. The manufacture of air frame parts will be limited to those items which can be fabricated with tools and equipment found in current air mobile tool and shop sets. Evacuate unserviceable modules/components and end items beyond the repair capability of AVUM to the supporting AVIM.

(b) Less than Company Size Aviation Units: Aviation elements organic to brigade, group, battalion headquarters, and detachment size units are normally small and have less than ten aircraft assigned. Maintenance tasks performed by these units will be those which can be accomplished by the aircraft crew chief or assigned aircraft repair person and will normally be limited to preventive maintenance, inspections, servicing, spot painting, stop drilling, application of nonstress patches, minor adjustments, module/component fault diagnosis, and replacement of selected modules/components. Repair functions will normally be accomplished by the supporting AVIM unit.

(2) Aviation Intermediate Maintenance (AVIM) provides mobile, responsive “One-Stop” maintenance support. (Maintenance functions which are not conducive to sustaining air mobility will be assigned to depot maintenance). AVIM may perform all maintenance functions authorized to be done at AVUM. Repair of equipment for return to user will emphasize support or operational readiness requirements. Authorized maintenance includes replacement and repair of modules/components and end items which can be accomplished efficiently with available skills, tools, and equipment. AVIM establishes the Direct Exchange (DX) program for AVUM units by repairing selected items for return to stock when such repairs cannot be accomplished at the AVUM level. The AVIM level inspects, troubleshoots, performs diagnostic tests, repairs, adjusts, calibrates, and alines aircraft system modules/components. AVIM units will have capability to determine the serviceability of specified modules/components removed prior to the expiration of the Time Between Overhaul (TBO) or finite life. Module/component disassembly and repair will support the DX program and will normally be limited to tasks requiring cleaning and the replacement of seals, fittings, and items of common hardware. Air frame repair and fabrication of parts will be limited to those maintenance tasks which can be performed with available tools and test equipment. Unserviceable reparable modules/components and end items which are beyond the capability of AVIM to repair will be evacuated to Depot Maintenance. AVIM will perform aircraft weight and balance inspections and other special inspections which exceed AVUM capability.

Provides quick response maintenance support, including aircraft recovery and air evacuation, on-the-job training, and technical assistance through the use of mobile maintenance contact teams. Maintains authorized operational readiness float aircraft. Provides collection and classification services for serviceable/unserviceable material. Operates a cannibalization activity in accordance with AR 710-2. (The aircraft maintenance company within the maintenance battalion of a division will perform AVIM functions consistent with air mobility requirements and conservation of personnel and equipment resources. Additional intermediate maintenance support will be provided by the supporting nondivisional AVIM unit.)

B-2 Use of the Maintenance Allocation Chart

NOTE

Nomenclatures used throughout the MAC are approved item names. Those terms/nomenclatures expressed in parentheses are generic in nature and are not to be considered as official terminology.

a. The Maintenance Allocation Chart assigns maintenance functions to the lowest category of maintenance based on past experience and the following considerations.

(1) Skills available.

(2) Work time required.

(3) Tools and test equipment required and/or available.

b. Only the lowest category of maintenance authorized to perform a maintenance function is indicated. If the lowest maintenance category cannot perform all tasks of any single maintenance function (e.g., test, repair), then the higher maintenance level(s) that can accomplish additional tasks will also be indicated.

c. A maintenance function assigned to a maintenance category will automatically be authorized to be performed at any higher maintenance category.

d. A maintenance function that cannot be performed at the assigned category of maintenance for any reason may be evacuated to the next higher maintenance category. Higher maintenance categories will perform the maintenance functions of lower maintenance categories when required or directed by the commander that has the authority to direct such tasking.

e. The assignment of a maintenance function will not be construed as authorization to carry the related repair parts or spares in stock. Information to requisition or otherwise secure the necessary repair parts will be as specified in the associated Repair Parts and Special Tools List (RPSTL).

f. Normally there will be no deviation from the assigned level of maintenance. In cases of operational necessity, maintenance functions assigned to a maintenance level may, on a one-time basis and at the request of the lower maintenance level, be specifically authorized by the maintenance officer of the level of maintenance to which the function is assigned.

The special tools, equipment, etc. required by the lower level of maintenance to perform this function will be furnished by the maintenance level to which the function is assigned. This transfer of a maintenance function to a lower maintenance level does not relieve the higher maintenance level of the responsibility for the function. The higher level of maintenance will provide technical supervision and inspection of the function being performed at the lower level.

g. Changes to the Maintenance Allocation Chart will be based on continuing evaluation and analysis by responsible technical personnel and on reports received from field activities.

B-3 Maintenance functions.

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination (e.g., by sight, sound, or feel).

b. Test. To verify serviceability by measuring the mechanical, pneumatic, hydraulic, or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (includes decontaminate, when required), to preserve, to drain, to paint, or to replenish fuel, lubricants, chemical fluids, or gases.

d. Adjust. To maintain or regulate, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to specified parameters.

e. Aline. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test, measuring, and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Remove/install. To remove and install the same item when required to perform service or other maintenance functions. Install may be the act of emplacing, seating, or fixing into position a spare, repair part, or module (component or assembly) in a manner to allow the proper functioning of an equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services[1], including fault location/troubleshooting[2], removal/installation, and disassembly/assembly[3] procedures, and maintenance actions[4] to identify troubles and restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) prescribed to restore an item to a completely serviceable/operational condition as required by maintenance standards in appropriate technical publications (i.e., DMWR). Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours/miles, etc.) considered in classifying Army equipment/components.

---

[1]Services - inspect, test, service, adjust, aline, calibrate, and/or replace.

[2]Fault locate/troubleshoot - The process of investigating and detecting the cause of equipment malfunctioning; the act of isolating a fault within a system or unit under test (UUT).

[3]Disassemble/assemble - encompasses the step-by-step taking apart (or breakdown) of a spare/functional group coded item to the level of its least componency identified as maintenance significant (i.e., assigned an SMR code) for the category of maintenance under consideration.

[4]Actions - welding, grinding, riveting, straightening, facing, remachining and/or resurfacing.

SECTION II
MAINTENANCE ALLOCATION CHART
FOR
PROCESSOR TEST SET AN/APM-415A

(1) GROUP NUMBER	(2) COMPONENT/ ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY AVUM	AVIM	DEPOT	(5) TOOLS AND EQPT	(6) REMARKS
0	PROCESSOR TEST SET AN/APM-415A (C5079441)	INSPECT		0.6			
		TEST			1.2	1,2,3,4, 6,15,16,19	
		REPAIR			1.2	1,2,3,4, 6,15,16,19	
01	PROCESSOR TEST SET TS-3706A/APM-415 (C5079444)	TEST		0.9		1,2,3,4, 6,15,16,19	
		TEST			1.2	1,2,3,4, 6,15,16,19	
		REPLACE		0.3		1,3	
		REPAIR		0.9		1,3,17	A
		REPAIR			1.2	1,3,17	
0101	CKT CD, COMPUTER/DMA (C5079449) A2	TEST			1.2	2,4,8	
		REPLACE		0.3		1	
		REPAIR			3.0	1,2,3,4, 8,9,20	
0102	CKT CD, VIDEO GENERATOR (C5079455) A7	TEST			1.2	2,4,6,10	C
		REPLACE		0.3		1	
		REPAIR			3.0	1,2,3,4, 6,10	C
0103	CKT CD, DISPLAY/ PROTECT (C5079481) A8	TEST			1.2	2,4,6,7,11	C
		REPLACE		0.3		1	
		REPAIR			2.7	1,2,3,4, 6,7,11	C
0104	CKT CD, ANALOG SIGNAL INTERFACE (C5079482) A9	TEST			0.3	2,4,6,7,12	C
		REPLACE		0.3		1	
		REPAIR			2.7	1,2,3,4. 6,7,12	C

SECTION II (Continued)

(1) GROUP NUMBER	(2) COMPONENT/ ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY AVUM	AVIM	DEPOT	(5) TOOLS AND EQPT	(6) REMARKS
0105	CKT CD, MEMORY/ POWER STROBE (C5079704) A1	TEST			0.9	2,4,8,9, 18	
		REPLACE			0.3	1	
		REPAIR			3.0	1,2,3,4, 8,9,18	
0106	CKT CD, ANALOG CONTROL INTERFACE (C5079462) A4	TEST			0.4	2,4,6,7, 13	C
		REPLACE		0.1		1	
		REPAIR			1.1	1,2,3,4, 6,7,13	C
0107	CKT CD, DIGITAL SIGNAL PROCESSOR (C5079456) A3	TEST			0.4	2,4,5,6,7	C
		REPLACE		0.1		1	
		REPAIR			1.3	1,2,3,4, 5,6,7	C
0108	CKT CD, COMPUTER INTERFACE (C5079483) A5	TEST			0.4	2,4,6,14	C
		REPLACE		0.1		1	
		REPAIR			1.0	1,2,3,4, 6,14	C
0109	FRONT PANEL ASSEMBLY (C5079457)	REPAIR		1.8		3,17	
0110	TRANSPORT, MAG TAPE, CASSETTE (C5079461)	TEST			0.3	1,3	
		REPLACE		0.1		1,3,21	
		REPAIR			0.1	1,3,21	
0111	POWER SUPPLY, LV (C5079518)	TEST			0.3	2	
		ADJUST			0.1	1,2	
		REPLACE		0.3		1,3	
		REPAIR			0.3	2	
0112	INDICATOR, RADAR SIGNAL IP-1150/APR-39(V) (SM-C-877040)	TEST			0.3		B
		REPLACE		0.9		1,3	
		REPAIR			0.5		B
0113	CARD CAGE, BACKPLANE PRINTED WIRING BOARD (C5079484)	TEST			2.0	2	
		REPLACE		0.3		1,3	
		REPAIR			0.5	1,2,3,17	
02	TEST ADAPTER ASSY MX-9975/APM-415 (C5079650)	TEST			0.5	2	
		REPLACE		0.3			
		REPAIR			0.9	1,2,3,17	

SECTION II (Continued)

(1) GROUP NUMBER	(2) COMPONENT/ ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY			(5) TOOLS AND EQPT	(6) REMARKS
			AVUM	AVIM	DEPOT		
03	CASE, TEST SET CY-7712A/APM-415 (C5079443)	REPLACE REPAIR		0.2 0.3		1,3 1,3	
04	CABLE, PROCESSOR TEST SET (C5079588) W2	TEST REPLACE REPAIR		 0.1	0.1 0.2	2 1,2,3,17	
05	CABLE, PROCESSOR TEST SET (C5079591) W5	TEST REPLACE REPAIR		 0.1	0.1 0.2	2 1,2,3,17	

SECTION III
TOOLS AND TEST EQUIPMENT REQUIREMENTS
FOR
PROCESSOR TEST SET - AN/APM-415A

TOOL OR TEST EQUIPMENT REF. CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL NATO STOCK NUMBER	TOTAL NUMBER
1	AVIM, DEPOT	TOOL KIT, ELECTRONIC EQUIPMENT TK-101/G	5181-00-64-5178	
2	AVIM, DEPOT	FLUKE DIGITAL MULTIMETER MODEL 8000A (OR EQUIVALENT)	6625-00-322-8715	
3	AVIM, DEPOT	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	5180-00-610-8177	
4	AVIM, DEPOT	OSCILLOSCOPE OS-261/U TEKTRONIX MODEL 475 (OR EQUIVALENT)	6625-00-127-0079	
5	DEPOT	DIGITAL SIG PROCESSOR TEST SET SM-D-933140		
6	AVIM, DEPOT	POWER SUPPLY MODEL 4050 POWER DESIGN INC.	7021-01-041-0116	
7	DEPOT	PULSE GENERATOR HP8013B		
8	DEPOT	GENRAD 1792B TEST SET OR GENRAD 1795 TEST SET WITH INTERFACE • UNIVERSAL TEST FIXTURE 313826-000 • DISK CARTRIDGE 1792-9672 • DISK CARTRIDGE 313842-000 • DISK CARTRIDGE 313487-000 • LOAD BOARD 313827-000 • LOAD BOARD 313833-000		

SECTION III (Continued)

TOOL OR TEST EQUIPMENT REF. CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL NATO STOCK NUMBER	TOTAL NUMBER
9	DEPOT	PROM PROGRAMMER C5079673 • UV PROM ERASER SPECTRONICS MODEL PC-1100 • DATA I/O -29A UNIVERSAL PROGRAMMER 990-0029-010 • UNIPAK 950-0099-003K • PROGRAMMER-100 313626-000 • PTS OPERATIONAL CASSETTE TAPE MTC5079741-1 • TEST PATTERN CASSETTE TAPE MTC5079741-2		
10	DEPOT	VIDEO GENERATOR TEST SET SM-D-933139		
11	DEPOT	DISPLAY PROTECT TEST SET SM-D-933143		
12	DEPOT	ANLG SIG INTR TEST SET SM-D-933142		
13	DEPOT	ANLG CONTROL INTR TEST SET SM-D-933144		
14	DEPOT	COMPUTER INTR TEST SET SM-D-933141		
15	AVIM, DEPOT	DIGITAL PROCESSOR CM-480A/ APR-39(V) (C5079442)	5841-01-054-8541	
16	AVIM, DEPOT	DETECTING SET CONTROL C-10412A/APR-39(V) (C5079440)	5841-01-149-4094	

SECTION III (Continued)

TOOL OR TEST EQUIPMENT REF. CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL NATO STOCK NUMBER	TOTAL NUMBER
17	AVIM, DEPOT	USE WITH REPAIR OR REPLACING CONNECTOR		
		INSTALLING & REMOVAL TOOL, CONNECTOR ELECTRICAL CONTACT (SIZE 20 CONTACT) MS18278-1	5120-00-230-3770	
		CRIMPING TOOL, TERMINAL, HAND, M22520/2-01		
		CRIMPING TOOL, TERMINAL, HAND, M22520/2-03		
		CRIMPING TOOL, TERMINAL, HAND, M22520/2-06		
		CRIMPING TOOL, TERMINAL, HAND, M22520/2-08		
		CRIMPING TOOL, TERMINAL, HAND, M22520/2-09		
		TOOL, CONTACT, CONNECTOR, ASSEMBLY & DISASSEMBLY MS27495R22M	5120-00-146-6558	
		TOOL HAND CRIMP, MINIATURE, CLASS 1, MS3198-1	5120-00-833-4190	
		TOOL, INSERTION, CONTACT, CONNECTOR, MS3323-22	5120-00-177-7028	
		TOOL, REMOVAL, SOCKETS, CONTACT MS3344-23	5120-00-177-7029	
18	AVIM, DEPOT	PROCESSOR TEST SET AN/APM-415A	5120-00-177-4741	
		• CARD PULLER C5079575		
		• PUT DIAGNOSTIC PROGRAM CASSETTE TAPE MTC5079655		
		• MEMORY VERIFICATION PROGRAM CASSETTE TAPE MTC5079654		

SECTION III (Continued)

TOOL OR TEST EQUIPMENT REF. CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL NATO STOCK NUMBER	TOTAL NUMBER
18 (CONT)		• TEST ADAPTER MX-9975/APM-415 • PTS TS-3706A/APM-415 • FIVE TEST CABLES C5079649 C5079588 C5079589 C5079590 C5079591 • POWER ADAPTER SM-C-933053		
19	AVIM	COUNTER, ELECTRONIC HP5328A, AN/USM-459	6625-01-061-8928	
20	DEPOT	PUNCH PAPER TAPE READER 901-1951 • PAPER TAPE MTC5079732		
21	AVIM, DEPOT	TORQUE SCREWDRIVER		

SECTION IV
REMARKS
PROCESSOR TEST SET AN/APR-415A

REFERENCE CODE	REMARKS
A.	REPAIR CONSISTS OF REPLACING DEFECTIVE LAMPS, CABLES, HINGES, PRESSURE VALVE, OPERATED FUSES AND REPLACING DEFECTIVE MAJOR ASSEMBLIES
B.	REFER TO TM 11-5841-283-20, RADAR SIGNAL DETECTING SET, AN/APR-39(V)1.
C.	THE FOLLOWING QUANTITIES OF POWER SUPPLY, MODEL 4050, POWER DESIGN INC., ARE NEEDED FOR THE FOLLOWING CIRCUIT CARD TEST SET.

GROUP NO.	CKT CD	TEST SET	REQUIRED QTY. OF POWER SUPPLY
0102	VIDEO GENERATOR (C5079455)A7	VIDEO GENERATOR TEST SET	(5)
0103	DISPLAY/PROTECT (C5079481) A8	DISPLAY/PROTECT TEST SET	(4)
0104	ANALOG SIGNAL INTERFACE (C5079482) A9	ANALOG SIGNAL INTERFACE TEST SET	(7)
0106	ANALOG CONTROL INTERFACE (C5079462) A4	ANALOG CONTROL INTERFACE TEST SET	(1)
0107	DIGITAL SIGNAL PROCESSOR (C5079456) A3	DIGITAL SIGNAL PROCESSOR TEST SET	(1)
0108	COMPUTER INTERFACE (C5079483) A5	COMPUTER INTERFACE TEST SET	(4)

APPENDIX C
COMPONENTS OF END ITEM AND BASIC ISSUE ITEMS LISTS

SECTION I
INTRODUCTION

C-1. Scope

This appendix lists components of end item and Basic issue items for the (AN/APM-415A) to help you inventory items required for safe and efficient operation.

C-2. General

The components of End Item and Basic Issue Items Lists are divided into the following sections:

a. Section II. Components of End Item. This listing is for informational purposes only, and is not authority to requisition replacements. These items are part of the end item, but are removed and separately packaged for transportation or shipment. As part of the end item, these items must be with the end item whenever it is issued or transferred between property accounts. Illustrations are furnished to assist you in identifying the items.

b. Section III. Basic Issue Items. These are the minimum essential items required to place the (AN/APM-415A) in operation, to operate it, and to perform emergency repairs. Although shipped separately, packaged BII must be with the (AN/APM-415A) during operation and whenever it is transferred between property accounts. The illustrations will assist you with hard to identify items. This manual is your authority to request/requisition replacement BII, based on TOE/MTOE authorization of the end item.

C-3. Explanation of Columns

The following provides an explanation of columns found in the tabular listings:

a. Column (1) - ILLUSTRATION NUMBER. This column indicates the number of the illustrations in which the item is shown.

b. Column (2) - National Stock Number (NSN). Indicates the National Stock Number assigned to the item and will be used for requisitioning purposes.

c. Column (3) - DESCRIPTION. Indicates the Federal item name and, if required, a minimum description to identify and locate the item. The last line for each item indicates the FSCM (in parentheses) followed by the part number. If item needed differs for different models of this equipment, the model is shown under the "USABLE ON" heading on this column. These codes are identified as:

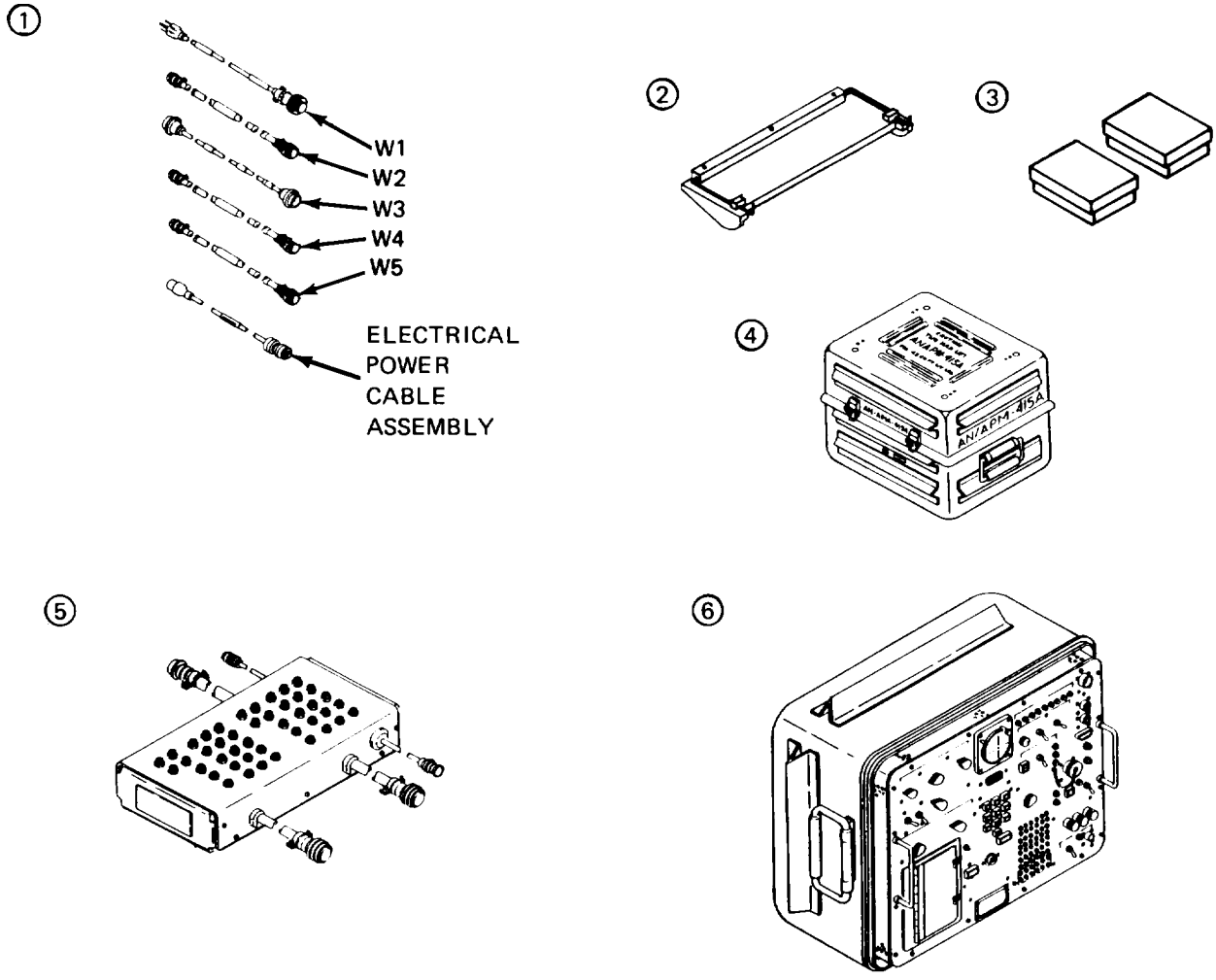
CODE	USE ON
EVU	AN/APM-415A

d. Colunm (4) - Unit of Measure (U/M). Indicates the measure used in performing the actual operational/maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr).

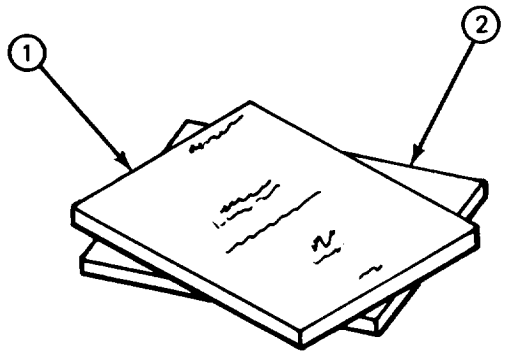
e. Column (5) - Quantity Required (QTY REQ). Indicates the quantity of the item authorized to be used with/on the equipment.

SECTION II

COMPONENTS OF END ITEM



(1) ILLUSTRATION NUMBER	(2) NSN	(3) DESCRIPTION FSCM & PART NUMBER	USABLE ON CODE	(4) U/M	(5) QTY REQ
1	TBD	CABLES W1 CABLE LNE CORD (59757) C5079649	EVU	ea.	1
		W2 CABLE, PROCESSOR TEST SET (59757) C5079588	EVU	ea.	1
		W3 CABLE, TEST SET CONTROL (57957) C5079589	EVU	ea.	1
		W4 CABLE, PROCESSOR TEST SET (57957) C5079590	EVU	ea.	1
		W5 CABLE, PROCESSOR TEST SET (57957) C5079591	EVU	ea.	1
		CABLE ASSY POWER, ELECTRICAL (57957) SM-C-933053	EVU	ea.	1
2	TBD	CARD EXTRACTOR ASSY (57957) C5079575	EVU	ea.	1
3	TBD	CASSETTE TAPE BOX ASSY (57957) C5079579 PTS DIAGNOSTIC (57957) C5079658 PTS SELF TEST	EVU	ea.	2
4	6625-01-147-4750	CASE, TEST SET CY-7712A/APM-415 (57957) C5079443	EVU	ea.	1
5		TEST ADAPTER ASSY MX-9975A/APM-415 (57957) C5079650	EVU	ea.	1
6	6625-01-147-4742	TEST SET, PROCESSOR TS-3706A/APM-415 (57957) C5079444	EVU	ea.	1



SECTION III
BASIC ISSUE ITEMS

(1) ILLUS NUMBER	(2) NATIONAL STOCK NUMBER	(3) DESCRIPTION FSCM AND PART NUMBER	USABLE ON CODE	(4) U/M	(5) QTY REQ
1	TBD	TM 11-6625-2940-14 Operator's Organizational and General Support Maintenance Manual	EVU	ea.	1
2	TBD	TM 11-6625-2940-14HR Hand Receipt Manual	EVU	ea.	1

APPENDIX D
EXPENDABLE SUPPLIES AND MATERIALS LIST

SECTION I

INTRODUCTION

SCOPE

D-1 This appendix lists expendable supplies and materials you will need to operate and maintain the Processor Test Set AN/APM-415A. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

EXPLANATION OF COLUMNS

D-2 Column (1) - ITEM NUMBER. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., 'Use cleaning compound, item 5, App. D').

Column (2) - LEVEL. This column identifies the lowest level of maintenance that requires the listed item.

(enter as applicable)

AVUM - Aviation Unit Maintenance
AVIM - Aviation Intermediate Maintenance

Column (3) - NATIONAL STOCK NUMBER. This is the National stock number assigned to the item; use it to request or requisition the item.

Column (4) - DESCRIPTION. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parentheses followed by the part number.

Column (5) - Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

SECTION II
EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NUMBER	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION	(5) U/M
1	AVUM/ AVIM	6810-00-543-7415	ALCOHOL, ISOPROPYL, GALLON CAN	GL
2	AVUM/ AVIM	8305-00-267-3015	CHEESECLOTH, CCCC 440-TY2-CL2, 36 IN. WIDE	FT
3	AVUM/ AVIM	6850-00-033-8851	TRICHLOROTRIFLUOROETHANE	5 GL CAN

GLOSSARY

The following special words and terms are used in this manual.

SPECIAL WORD/TERM	DEFINITION
A/D BITE	Analog to digital BITE command.
AL	Aft left.
AR	Aft right.
AUDSW	Audio switch.
AUXBAND1 thru AUXBAND5	Auxiliary band outputs 1 through 5.
BADDOSW thru BADD2SW	BITE address switch outputs 0 through 2.
BITADDO thru BITADD2	BITE address lines 0 through 2.
BLANKING$	External blanking.
CRUSEL	Communication register unit select.
CUIS	Control unit current source.
DBIN	Data bit in.
DMA	DIRECT Memory Access.
D1IN1,2,4,8	Display 1 input bits 1,2,4, and 8.
D21N1,2,4,8	Display 2 input bits 1,2,4, and 8.
D31N1,2,4,8	Display 3 input bits 1,2,4, and 8.
EMDAT00 through EMDAT15	External memory data bus, 16 lines.
EXTCS$	External chip select.
EXTEMADRV$	External memory address drive.
EXTEMDDRV$	External memory data drive.
EXTPW	External pulse width.
EXTREAD$	External read.
EXTWE$	External write.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
EXTWRITECS$	External write chip select.
FL	Forward left.
FR	Forward right.
LBVIDEN$	Low band video enable.
MA	Missile alert.
MEMDATDRV$	Memory data drive.
MPCRUINZ	Maintenance panel communications register unit input.
MPLOADZ	Maintenance panel load.
MPRSTZ	Maintenance panel reset.
NEGK	Negative K-axis drive.
NEGM	Negative M-axis drive.
PADDBUS00 thru PADDBUS14	Processor Test Set address bus, 15 lines.
PALCHBIT	Processor Test Set aft left channel bit.
PALMSEL$	Processor Test Set aft left main band select.
PALSSEL$	Processor Test Set aft left side band select.
PAM P05$, PAMP15$	Processor Test Set signal select amplitude.
PARCHBIT	Processor Test Set aft right channel bit.
PARMSEL$	Processor Test Set aft right main band select.
PARSSEL$	Processor Test Set aft right side band select.
PATMACLK	Processor Test Set automatic mode clock.
PAUDMA	Processor Test Set audio/ma signal.
PAUTOMODE	Processor Test Set auto mode.
PAUTO$	Processor Test Set auto mode enable.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
PA1 FAIL$ thru PA8FAIL$	Processor Test Set assembly fail, assemblies 1 through 8.
PBITE$	Processor Test Set BITE.
PBITFL$	Processor Test Set BITE fail.
PBITGO$	Processor Test Set BITE go.
PBLANK$	Processor Test Set blank.
PBLANKEN$	Processor Test Set blank enable.
PBLNKPULS	Processor Test Set blank pulse.
PBNDMRK1, PBNDMRK2	Processor Test Set band marks, 1 and 2.
PBNDSEL$	Processor Test Set band select.
PBVFVcc	Processor Test Set buffer Vcc.
PBUSY	Processor Test Set busy.
PCADD03, PCADD09 thru PCADD14	Processor Test Set control address lines 03, and 09 through 14.
PCASSDATA	Processor Test Set cassette data.
PCASSLOAD	Processor Test Set cassette load.
PCHANTEST	Processor Test Set channel test.
PCHIPSEL$	Processor Test set chip select.
PCLK$	Processor Test Set clocks.
PCORR$	Processor Test Set correlation.
PCORREN$	Processor Test Set correlation enable.
PCRUIN$	Processor Test Set communications register unit input.
PCWAUTO$	Processor Test Set control word auto.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
PCWCLR$	Processor Test Set control word clear.
PCWEN$	Processor Test Set control word enable.
PCWST$	Processor Test Set control word self test.
PCWTS$	Processor Test Set control word test strobe.
PCW1$	Processor Test Set control word 1.
PDATBUS00 thru PDATBUS15	Processor Test Set data bus, 16 lines.
PDBIN	Processor Test Set data bus input.
PDGAUD$	Processor Test Set digital audio.
PDIGSIGIN	Processor Test Set digital signal input.
PDSPLAL	Processor Test Set display aft left.
PDSPLAR	Processor Test Set display aft right.
PDSPLFL	Processor Test Set display forward left.
PDSPLFR	Processor Test Set display forward right.
PEMADRV$	Processor Test Set external memory address drive.
PEMDAT00-15	Processor Test Set external memory data bus, 16 lines.
PEMPDRV$	Processor Test Set external memory data drive.
PEOT	Processor Test Set end of tape.
PEXTCS$	Processor Test Set external chip select.
PEXTEMADR$	Processor Test Set external test connector external memory address drive.
PEXTEMDDR$	Processor Test Set external test connector external memory data drive.
PEXTREAD	Processor Test Set external test connector read.
PEXTWE$	Processor Test Set external test connector write enable.
PFLCHBIT	Processor Test Set forward left channel bit.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
PFLMSEL$	Processor Test Set forward left main band select.
PFLSSEL$	Processor Test Set forward left side band select.
PFRCHBIT	Processor Test Set forward right channel bit.
PFRMSEL$	Processor Test Set forward right main band select.
PFRSSEL$	Processor Test Set forward right side band select.
PFWD	Processor Test Set forward.
PGAP	Processor Test Set gap.
PGENSYNCH	Processor Test Set generated synch.
PHIALT$	Processor Test Set high altitude.
PHIALTLD$	Processor Test Set high altitude load.
PHINOIS$	Processor Test Set high noise.
PHOLD$	Processor Test Set hold.
PHOLDA	Processor Test Set hold A.
PINTMEM	Processor Test Set interrupt memory.
PKBRINT$	Processor Test Set keyboard interrupt.
PKYBRD	Processor Test Set keyboard read.
PLOAD$	Processor Test Set load.
PLONOIS$	Processor Test Set low noise.
PMALAMP	Processor Test Set missile alert lamp.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
PMEMDATDRV$	Processor Test Set memory data drive.
PMEMEN$	Processor Test Set memory enable.
PMPCRUINZ	Processor Test Set maintenance panel communication register unit input.
PMPLOADZ	Processor Test Set maintenance panel load.
PMPRSTZ	Processor Test Set maintenance panel reset.
PNEGTRIG$	Processor Test Set negative trigger.
PN12VPTS	Processor Test Set negative 12 V dc.
PN5VPTS	Processor Test Set negative 5 V dc.
POSK	Positive K-axis drive.
POSM	Positive M-axis drive.
PPOSTRIG$	Processor Test Set positive trigger.
PPRETRIG	Processor Test Set pretrigger.
PPRFAIL$	Processor Test Set power fail.
PPSSTRB$	Processor Test Set power supply strobe.
PPWRFAIL	Processor Test Set power fail.
PP15VPTS	Processor Test Set positive 15 V dc.
PP26VPTS	Processor Test Set positive 26 V dc.
PQA-PQD	Processor Test Set power check code (4-bits).
PREADY	Processor Test Set ready.
PRESET$	Processor Test Set reset.
PREV	Processor Test Set reverse.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
PRIBITE1 thru PRIBITE6	Priority Built In Test 1 thru 6
PSB0DB$, PSB5DB$, PSB6DB$	Processor Test Set angle select code, 3 bits.
PSLFTST$	Processor Test Set self test.
PSPARE$	Processor Test Set spare.
PSPARELD$	Processor Test Set spare load.
PSPARINT1$	Processor Test Set spare interrupt 1.
PSPKRA	Processor Test Set speaker A wire.
PSPKRB	Processor Test Set speaker B wire.
PSR$	Processor Test Set system reset.
PSRADD	Processor Test Set serial address.
PSRDAT	Processor Test Set serial data.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
PST	Processor TestSet self test.
PSTLD$	Processor TestSet self testload.
PS8MHZCL$	Processor TestSet 8 MHz clock.
PTGTSEP	Processor TestSet target separate.
PTSCRUCLK	Processor Test Set communication register unit clock.
PTSCRUIN	Processor Test Set communication register unit input
PTSCRUOUT	Processor Test Set communication register unit output
PTSINT$	Processor Test Set interrupt
PUT	Processor Under Test
PUNBLKDR	Processor Test Set unblank drive.
PUPA00Z thru PUPA14Z	Processor Test Set CPU address bus, 15 lines.
PUPCRUCLKZ	Processor Test Set CPU communication register unit clock.
PUPCRUOTZ	Processor Test Set CPU communication register unit output.
PUPEDCYZ	Processor Test Set CPU end cycle.
PUPIAQZ	Processor Test Set CPU instruction acquisition.
PUPMEMENZ	Processor Test Set CPU memory enable.
PUPRSTZ	Processor Test Set CPU reset
PUPTFAIL	Processor Test Set unit test power fail.
PVIDPULS	Processor Test Set video pulse.
PVSTRB$	Processor Test Set video strobe.
PWE$	Processor Test Set write enable.
PWMODE$	Pulse width mode.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
P1MHZCLK	Processor TestSet 1 MHz clock.
P125KHZ	Processor TestSet 125 kHz.
P26.5VPTS	Positive 26.5Vdc, Processor TestSet.
SERDATINH	Serial data inputhigh.
SERDATINL	Serial data input low.
SIMVID	Simulated video.
SRSWITCH$	System reset switch.
STAFT	Self test aft.
STFWD	Self test forward.
SWSEL1, SWSEL2	Switch select 1 and 2.
S12$-S16$	Switch S1, lines 2 through 6.
S1o1$, S103$	Switch S10, lines 1 and 3.
S21$ thru S24$	Switch S2, lines 1 through 4.
S32$, S33$	Switch S3, lines 2 and 3.
S51$thru S53$	Switch S5, lines 1 through 3.
S61$thru S65$	Switch S6, lines 1 through 5.
S72$thru S74$	Switch S7, lines 2 through 4.
S91$	Switch S9, line 1.
TIPROC	Test current, Processor.
TN15VPROC	Test negative 15 V dc, Processor.
TN6VPROC	Test negative 6 V dc, Processor.
T15VPROC	Test 15 V dc, Processor.
T5VPROC	Test 5 V dc, Processor.
T6VPROC	Test 6 V dc, Processor.
T26VPROC	Test 26 V dc, Processor.
UPA00Zthru UPA14Z	CPU address bus, 15 lines.

GLOSSARY (Continued)

SPECIAL WORD/TERM	DEFINITION
UPCRUCKZ	CPU communications register unit clock.
UPIAQZ	CPU instruction acquisition.
X1 thru X4	Keypad matrix, X-axis.
Y1 thru Y3	Keypad matrix, Y-axis.

INDEX

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

Subject | Page

D (Continued)

INDEX (Continued)

Subject — Page

D (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM (PRINT YOUR UNIT'S COMPLETE ADDRESS)
Commander
Stateside Army Depot
ATTN: AMSTA-US
Stateside, N.J. 07703

DATE SENT
10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-6625-2940-14	23 Jan 74	Processor Test Set AN/APM-415A

BE EXACT PIN-POINT WHERE IT IS			
PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO
2-25	2-28		
3-10	3-3		3-1
5-6	5-8		
		F03	

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°.

REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.

Item 5, Function column. Change "2 db" to "3db."

REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.

Add new step f.1 to read, "Replace cover plate removed in step e.1, above."

REASON: To replace the cover plate.

Zone C 3. On J1-2, change "+24 VDC to "+5 VDC."

REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

SIGN HERE
SSG I. M. DeSpiritof

DA, FORM 1 JUL 79 2028-2 PREVIOUS EDITIONS ARE OBSOLETE.

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

TEAR ALONG PERFORATED LINE

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

SAMPLE

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-6625-2940-14	15 January 1986	Processor Test Set AN/APM-415A

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARAGRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S. IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

FOLD BACK ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

TEAR ALONG PERFORATED LINE

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-6625-2940-14	15 January 1986	Processor Test Set AN/APM-415A

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARAGRAPH	FIGURE NO	TABLE NO

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S. IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

FOLD ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

TEAR ALONG PERFORATED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-6625-2940-14	15 January 1986	Processor Test Set AN/APM-415A

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARAGRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S. IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

TEAR ALONG PERFORATED LINE

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

U.S. MAIL

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

By Order of the Secretary of the Army:

JOHN A. WICKHAM JR.
General, United States Army
Chief of Staff

Official:

MILDRED E. HEDBERG
Brigadier General, United States Army
The Adjutant General

DISTRIBUTION:
S0392 - 10 COPIES, 100 COPIES TO BE STOCKED AT USAAGPC-St. Louis.

*U.S. GOVERNMENT PRINTING OFFICE 1990–261–872/20607.